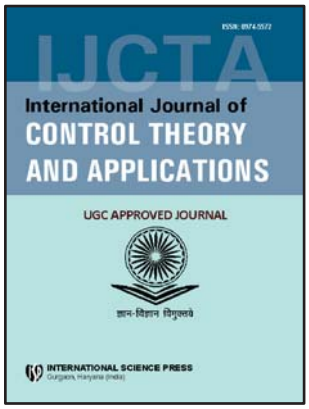

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A Design of Encoding and Decoding by using Standard Basis Code with Multiplexer using AND Operation for an on-Chip Communication Network

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Abstract: In the rapid growth of the computational complexity, more and more processing elements (PEs) are integrated onto a single chip, and Network on Chip (NoC) has been proposed to address the scalability, reliability issues of on chip communication. However, conventional packet switched NoC suffer from nondeterministic transmission latency and limited opportunities for parallel data transfer, since multiple flows cannot get through a link at the same time. To resolve these problems, the Code Division Multiple Access technique as an effective method for implementing high performance on-chip communication was applied to NoC. To reduce the delay of the NoC, we implement the multiplexer using AND operation in the encoder and decoder. In the transmitter module, source data from various sender is individually encoded with an orthogonal code of a standard basis by using multiplexer, this different coded data is mixed into one. After that, through the on chip communication infrastructure the sums of data can be transmitted to their destinations. In the receiver module, by taking an XOR operation between the sums of data and the corresponding orthogonal code a sequence of chips is retrieved. Finally, original data can be reconstructed. This method achieves 56.11% less delay, 11.21% area saving and achieves maximum throughput than the existing one.

Keywords: *Integrated circuit(IC), Code division multiple access (CDMA), Globally Asynchronous Locally Synchronous (GALS), Network on chip (NoC).*

1. INTRODUCTION

The Network-on-Chip (NoC) concept has mostly used technique of difficult System-on-Chip (SoC) designs for handling the large on-Chip communication requirements [1]. A traditional Intellectual Property (IP) blocks are collide with each other to communicate over the shared bus based interconnection scheme that does not scale well to very large SoCs. To route the information between IP blocks and it results achieve a very large bandwidth, delay and power within the chip by using the packet-switching paradigm. The previously proposed CDMA NoCs based on a digital encoding and decoding method and it requires spreading codes with orthogonal codes. To this end, the standard basis code is typically used. However, the Standard Basis Code (SB) encoding and decoding method has disadvantages, which are given as follows.

1. **Data loss:** While transferring data parallel between the transmitter and receiver, data will collide and it will cause data loss and finally result in transmission delay also. The proposed system isto eliminate this data loss and the resulting transmission delay.

To address the aforementioned weakness, we proposed a Standard Basis (SB) Encoding/Decoding method, which outperforms the Standard Basis encoding/decoding method. The SB encoding/decoding method can be applied to any CDMA NoCs to improve their performance. The rest of this brief is organized as follows. In Section 2, we dis-cuss related work. In Section 3 and 4, we detail the SB encoding/decoding method and formally prove its correctness. The simulation results and comparisons between the previously proposed Standard Basis method and the newly proposed Standard Basis method are presented in Section 6. Finally, we draw the conclusions in Section 8.

2. LITERATURE REVIEW

2.1. High Performance CDMA Based Broadcast Free Photonic Multi-CoreNetwork on Chip

High Performance CDMA [1] was developed by Soumyajit Poddar, Prasun Ghosal and Hafizur Rahaman in 2016.In this technique to eliminate invalidation broadcasts in photonic multicores. Due to this encoding, invalidation takes less time and more secure, but average network latency increases. Substantial performance benefits are obtained, especially as the number of cores is scaled up. A lightweight distributed flow control scheme is also introduced. And also propose a low insertion loss topology. The proposed technique has low area overhead, although energy required is at par with state of the art.

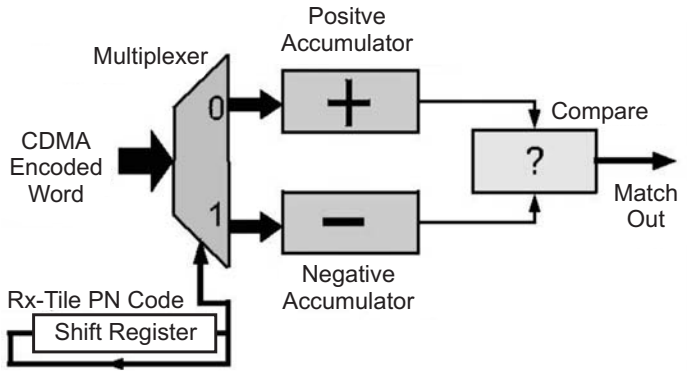


Figure 1: Block diagram of CDMA Transmitter

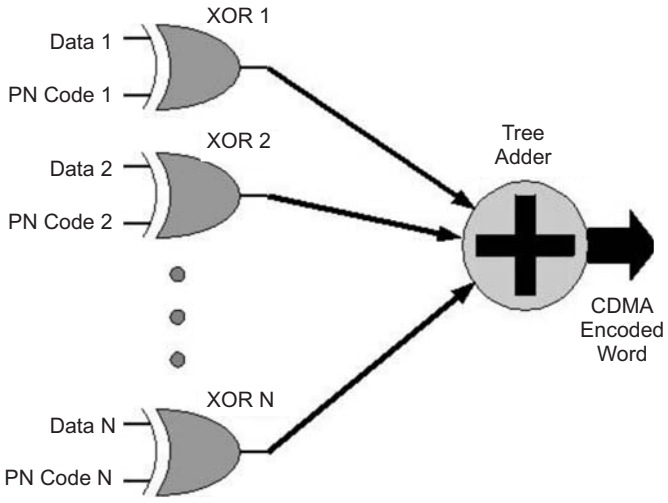


Figure 2: Block diagram of CDMA Receiver

2.2. Overloaded CDMA Interconnect for Network-on-Chip (OCNoC)

In the Overloaded CDMA Net-work On Chip (OCNoC) has central router with dynamic code assignment. In overloaded CDMA it will increase the physical layer capacity of the conventional CDMA crossbar by 100% without increasing the physical layer complexity and latency. Consequently, the OCNoC router can transmit twice the number of packets at the same transfer latency of NoCs employing the conventional CDMA codes. Dynamic code assignment enables the network router to utilize a fixed number of spreading codes regardless of the number of interconnected PEs. Two OCNoC variants were developed, Serial-OCNoC (SOCNoC) and Parallel-OCNoC (POCNoC). The OCNoC router is compared to existing CDMA-based routers in terms of latency, throughput, area, and energy dissipation. The overloaded CDMA codes reduce the packet blocking induced by dynamic code assignment, which reduces the packet transfer latency. The OCNoC routers provide up to 141% throughput improvement due to the crossbar capacity improvement, with up to 62% and 82.5% area per PE and dynamic energy dissipation reduction, respectively. The deviation in the latency of the presented OCNoC router is down to 1.7% of the mean latency, which makes the OCNoC a preferred choice for applications requiring guaranteed, high-throughput QoS.

2.3. Implementation of Network on Chip (NOC) using Globally-Asynchronous Locally-Synchronous (Gals) Scheme

Ccommunication plays a fundamental and crucial role for the development of human society in every aspect because better communications facilitate better understanding and cooperation between individuals. As in electronics field, believe that the same truth also applies to on-chip systems, which means that the quality of communication in an on-chip system prominently affects system performance. As the complexity of an on-chip system keeps growing, because of that the communication among functional hosts in the system becomes a non-trivial issue to deal with. Currently, silicon chips which contain thousands of millions of transistors with 45nm feature size are already available on market, e.g. Intel Pentium processor. As the number of system components becomes larger, current widely applied bus structures for data transfers in an on-chip system. Two main disadvantages are bus arbitration bottleneck and bandwidth limitation. The rest of this brief is organized as follows. In Section 2, we discuss related work. In Section 3 and 4, we detail the SB encoding/decoding method and formally prove its correctness.

2.4. Encoding and Decoding using Standard Basis Code with Star Network-on-Chip (NOC) Topology

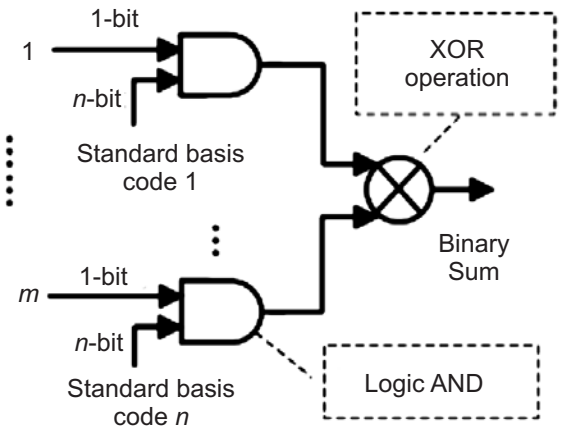


Figure 3: Encoding Process

In transmitter side, source data from varies senders are individually encoded with an orthogonal code of a standard basis code by using XOR operation these coded data are mixed together. After that, through the on chip communication infrastructure the sums of data can be transmitted to their destinations. In the receiver module, by taking an AND operation between the sums of data and the corresponding orthogonal code a sequence of chips is retrieved.

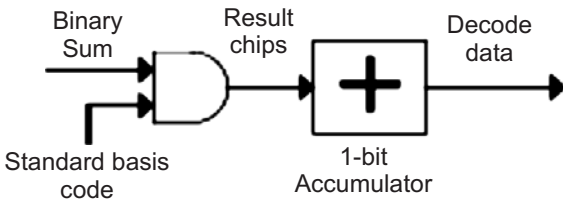


Figure 4: Decoding Process

The Figure3 shows that, a data bit from a different sender is apply into an AND gate, and it will be separated to n chip encoded data with an orthogonal code of a standard basis. Then, by using XOR operation encoded data from different senders are mixed together and a sum of binary signal is generated. That means, the sequence of binary signal from encoder is transferred to destination using one single wire. The Figure4 shows, receiver side an AND operation is taken between the sum of binary signal and the corresponding orthogonal code in chip by chip manner. After that, the result chips are sent to an accumulator. After m-chips are accumulated (m is the length of the orthogonal code), the output value of the accumulator will be the corresponding original data. There is always only one chip equal to 1 and all other chips are equal to 0 for an orthogonal code in standard basis. Hence, the maximal accumulated value in the Standard Basis accumulator is 1 and it can be stored in a 1-bit register. Therefore, in the Standard Basis decoding module, only one AND gate and an accumulator with one 1-bit register are used, resulting in less logical resources.

3. PROPOSED WORK

3.1. Code Division Multiple Access (CDMA) Network Onchip (NOC)

A new standard based encoding and decoding method to force the cost and performance of Code Division Multiple Access **(**CDMA) Network on Chip in delay, area and network throughput is proposed. In the transmitter module, source data from varies senders are individually encoded with an orthogonal code of a standard basis and by using multiplexer these coded data are mixed together. After that, through an on chip communication infrastructure the sums of data can be transmitted to their destinations. In the receiver module, by taking an XOR operation between the sums of data and the corresponding orthogonal code a sequence of chips is retrieved. Finally, original data can be reconstructed.

In this figure 5, Parallel-to-Serial (P2S) module, Serial-to-Parallel (S2P) modules, Network Interface (NI), Programmable Element (PE). A Programmable Element executes the application tasks and data's are divided by using network interface from Programmable Element into packets and reconstruct data flows by using packets from Network-on-Chip (NoC). In the sender, via a Parallel-to-Serial (P2S) module packets from Network interface are switched to a bit stream [7]. This bit is joined with some code words. By using addition module, the coded data from varies encoding modules are joined together. Then, the outputs of data's are transferred to receivers. In the receiver, using sums of data from transmitter, original data is reconstructed. Then these continuous bit streams are transmitted to packet flits by Serial to Parallel (S2P) modules. Finally, these packet flits are transferred to Network interface. Finally, these packet flits are transferred to Network interface.

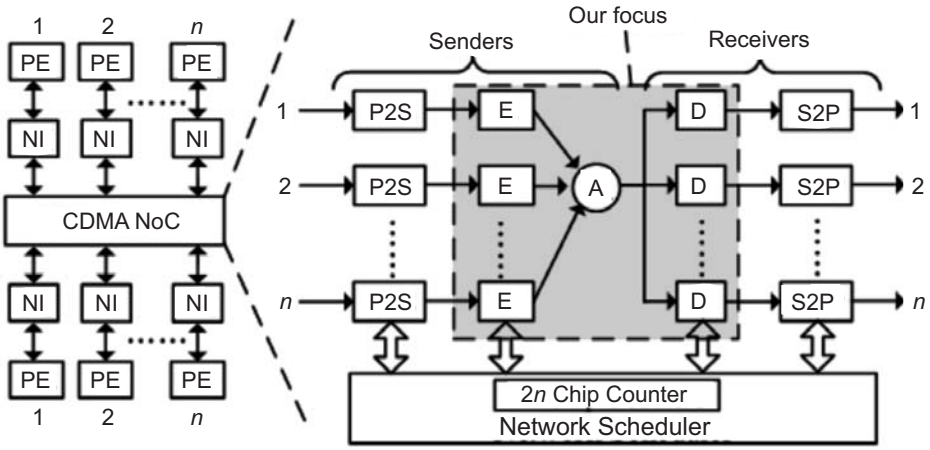


Figure 5: Structure of CDMA NoC

3.2. Standard Basis (SB) Encoding Scheme

The *n* number of inputs of data is collected from n number of sources. These n number of collected signals are given as input to the encoder in bit-by-bit manner. Consider a code word is X bit. By using PN sequence generator in this code word is generated. The input signal is separated into n bits by taking AND operation using multiplexer with X as code word. In AND operation "When both input's are '1' then output will be '1' ".

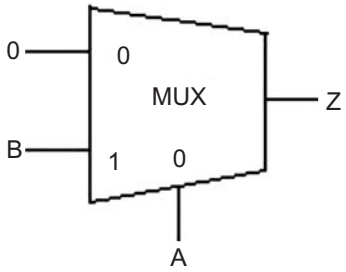


Figure 6: Mux using AND operation

Table 1
AND operation

A	*B*	*Z*
0	0	0
0	0	0
1	0	0
1	1	1

In table 1, A and B are the two inputs of AND gate and the output is Z. The principle of multiplexer is based on AND operation of input bit and code word. The diagram 6 explains, taking one of the input as 0 or 1 and the other as code word is B. In the table 1, consider A as select line and B as code word. If select line is 0, then the output will be same as input. If select line is 1, then the output will be same as code word. An original data bit from a different sender is apply into a multiplexer, and it will be separated to n chip encoded data with an orthogonal code of a standard basis. The relationship between a bit and a chip is shown in Fig. 6.

Then, by using XOR operation encoded data from different senders are mixed together and a sum of binary signal is generated. That means, the sequence of binary signal from encoder is transferred to destination using one single wire. The progressions of both the encoding schemes are depicted in Fig. 6.

3.3. Standard Basis Decoding Scheme

When the binary sum signal arrives at receivers, multiplexer operation is taken between the binary sum and the corresponding orthogonal code in chip-by-chip manner. Then, the result chips are sent to an accumulator. After m-chips are accumulated (m is the length of the orthogonal code), the output value of the accumulator will be the corresponding original data.

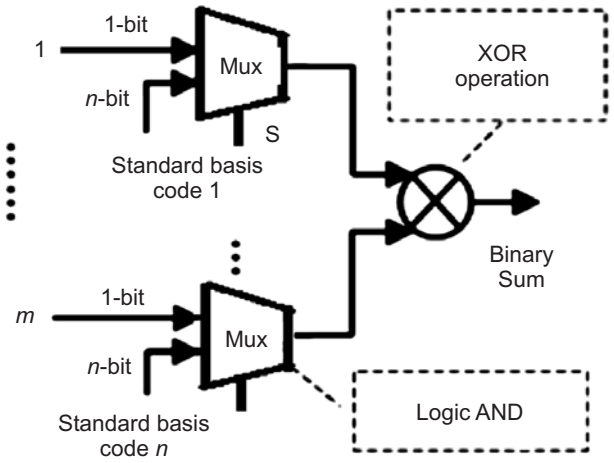


Figure 7: Standard Basis Encoding process

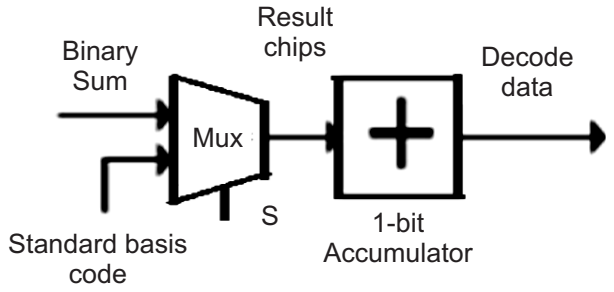


Figure 8: Standard Basis Decoding process

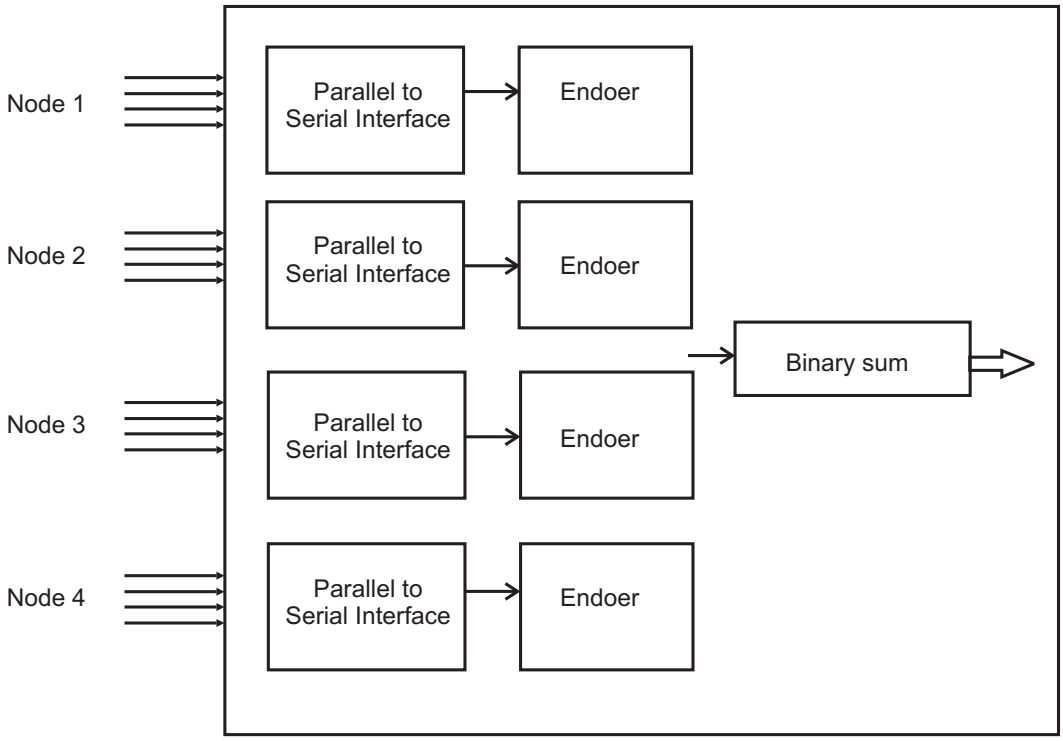
Note that there is always only one chip equal to 1 and all other chips are equal to 0 for an orthogonal code in standard basis. Hence, the maximal accumulated value in the Standard Basis accumulator is 1 and it can be stored in a 1-bit register. Therefore, in the Standard Basis decoding module, only one gate and an accumulator with one 1-bit register are used, resulting in less logical resources. The same as like that, we can perform *n* number of operations with an n number of gates. For example, in figure7consider input data is 0, standard basis spreading code word is 1 and the select line is 1. When Input has given of bits to the encoder. There multiplexer will perform AND operation and produces an outputs. The same operation will be taken in n encoders .Both of the outputs will be mixed together by taking an multiplexer XOR operation .The resulting output is in binary sum as 0 or 1.The binary output result will be given as input of decoder.

In decoder, this dummy data is converted into original user friendly format. If spreading code word of decoder is same as the spreading code of encoder then perform AND operation. The resultant output will be applied to the accumulator, which performs XOR operation and produces the result. Finally, the output is same as the input data .By using multiplexer for performing AND and XOR operation it will reduce the data transfer delay and area size. A multiplexer is a circuit that accept many input but give only one output. The technique of transmitting multiple signals over a single medium is called multiplexing. It is used for digital applications, also called digital multiplexer, is a circuit with many input only one output. By applying control signals, we can steer any input to the output. Multiplexer are used in various fields where multiple data need to be transmitted using a single line. Multiple signals can be isolated and eventually, the desire signals reach the intended recipients. By performing multiple data transfer we can achieves high timing. Mainly we used multiplexer instead of AND gate, it has very low number of gates because of that it occupies very less area and for data transferring also it takes very less timing.

3.4. Network Scheduler

In the Code Division Multiple Access Network-on-Chip (NoC), network scheduler receives the transmitting requests from senders and assigns proper spreading codes to the senders and requested receivers. Note that all-zero code word is assigned to nodes having no data to transmit/ receive. Moreover, when there are multiple senders requesting the same receiver, the scheduler will apply an arbitration scheme, for example, round-robin. The chip counters calculate how many orthogonal chips are used in one encoding/decoding operation.

Each node needs two chip counters, one for the sender and the other for the receiver. Note that packet flits from Network Interface can also be transformed to multiple bit streams in the Parallel-to-Serial(P2S) module to make tradeoffs between power/area cost and packet transfer latency, and the scheduler should provide a bit-synchronous scheme to maintain the orthogonally of the transmitted channels.



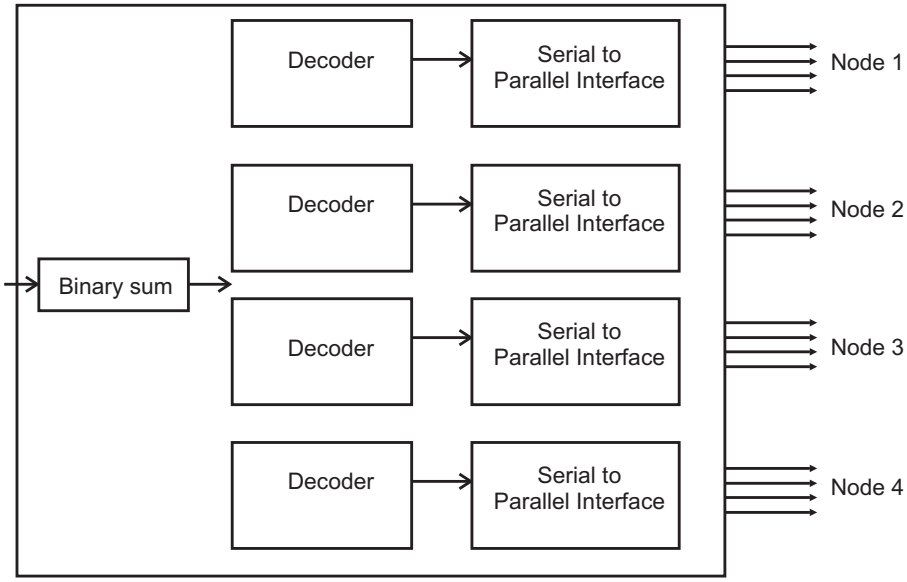


Figure 9: Block Diagram of the proposed system

Four bits of Data from many nodes are given to parallel to serial interface and encoded. The resulting output are added and then transmitted. The receiver decodes the data and sent to serial to parallel interface. Finally the decoded data is delivered to the nodes. Figure 8 has four nodes each and every nodes are primary inputs. Each packet contains Data, source node address and destination node address. For example taking node1 four bits as input bits and node 3 four bits as output bits. Those source and destination bits are kept in a packet. When Input has given of four bits from node 1 to Parallel to serial interface. The parallel to serial interface will selects one out of four bits from right to left and will transfer it to the encoder. And the encoder will perform AND operation between the received bit from parallel to serial interface and data bits. The above said operation to be performed in node with received output from this node 2 operation to be added with the node 1 output, this output to be given as an input in decoder and this has to be decoded with data bits. The result will be transferred to accumulator and this will perform XOR operation with each and every bits and it will produce single bit as output. These same operations to be performed for the remaining bits in the node1and the final output are equal to the input.

4. SIMULATION RESULTS

The simulation results for the comparison of Standard basis encoding and decoding with AND gate and Standard basis encoding and decoding multiplexer using AND operation is using Xilinx ISE Simulator as shown in figure. Area, delay analyzed and maximum throughput measured using Xilinx 14.2 as shown in Table II and Table III. A network is implemented in verilog with 6,8 and 16 nodes. Synopsys DC with a 40mm standard cell library is used to synthesize the delay and area consumption results.

4.1. CDMA Encoder/Decoder Power and Area cost

We compare the power and area cost of the two encoding/decoding methods. Here, encoder and decoder besides its chip counters are taken into consideration. Normally chip counters are implemented by using registers. There are 6, 8 and 16 nodes, the standard basis code with AND gate length is p and new standard basis code length is q respectively. In table 2 it shows, area and power consumption of encoder/decoder. From the table, we can easily find out the best performance. Power value =Maximum power achieves from the both decoder and encoder of existing method - Maximum power achieves from the both decoder and encoder of proposed method /Maximum power achieved.

The total performance achieves 11.21% area saving and 28.2% power saving.

Table 2
Comparison of Standard Basis Code with multiplexer using AND operation and Standard Basis Code with AND gate

Modules		*SB Encoding/Decoding using AND Gate*			*SB Encoding/Decoding MUX using AND Operation*		
		Area (µm2)	*Delay (ns)*	*Power (m M)*	*Area (µm2)*	*Delay (ns)*	*Power (m M)*
6 Nodes	Encoder	151	4.367	0.37	143	3.11	0.23
	Decoder	306	4.91	0.8	280.1	4.7	0.76
	Total	457	9.277	1.17	423.1	7.81	0.99
8 Nodes	Encoder	230	6.24	0.6	210	6.0	0.5
	Decoder	390	8.6	0.97	322	7.4	0.79
	Total	620	14.84	1.57	532	13.3	1.29
16 Nodes	Encoder	600.2	11.01	1.2	556	10.9	1.0
	Decoder	587.2	15.9	2.7	498	14.5	1.8
	Total	1187.2	26.91	3.9	1054	25.4	2.8

4.2. CDMA Encoder/Decoder Power and Area cost

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The total performance achieves 11.21% area saving and 28.2% power saving.

4.3. Comparison of CDMA Decoding/Decoding Delay

In table 2 shows the delay value of two methods. From the table, the standard basis code with multiplexer using AND operation achieves low delay than standard basis code Encoding/decoding method using AND gate. By using two different encoding/decoding methods we have compared the performance of Code Division Multiple Access Network on Chip. Delay value = Maximum Delay achieves from the both decoder and encoder of existing method - Maximum delay achieves from the both decoder and encoder of proposed method /Maximum delay achieved.

4.4. Comparison of CDMA Network on Chips

By using two encoding/decoding schemes we have compared the performance of CDMA Network on Chips. Besides the decoder module and encoder module, other on-chip modules, such as parallel-to-serial modules, serial-to-parallel modules and network scheduler are all included in the Network on Chips. The results of

CDMA NoC performance in delay, area cost and power consumption are given in Table II and throughput results are given in Table III. From Table II, we can find that the New Standard Basis code with multiplexer using AND operation Code Division Multiple Access Network on Chip (CDMA NoC) has lower area, delay and power cost than the existing standard basis Code Division Multiple Access Network on Chip. Since both NoCs contain the parallel-to-serial module, scheduler module, and serial-to-parallel module, the percentage of power and area saving of the new code division multiple access, is as much as the previously calculated Standard basis code. However, the SB CDMA NoC still gains 14.10% – 25.27% power saving and 18.25%– 2 4.11% area saving. Fig. 10 evaluates the maximal throughput of both NoCs .

Throughput = No of output bits X Maximum Operating Frequency.

Table 3
Comparison of Throughput results

S.No	*Modules*		*Throughput (Packets/Second)*
1.	Standard Basis code using AND gate	6 Nodes	991.871
		8 Nodes	1232.88
		16 Nodes	1538.92
2.	Standard Basis code Mux using AND operation	6 Nodes	4114.064
		8 Nodes	6995.84
		16 Nodes	10275.36

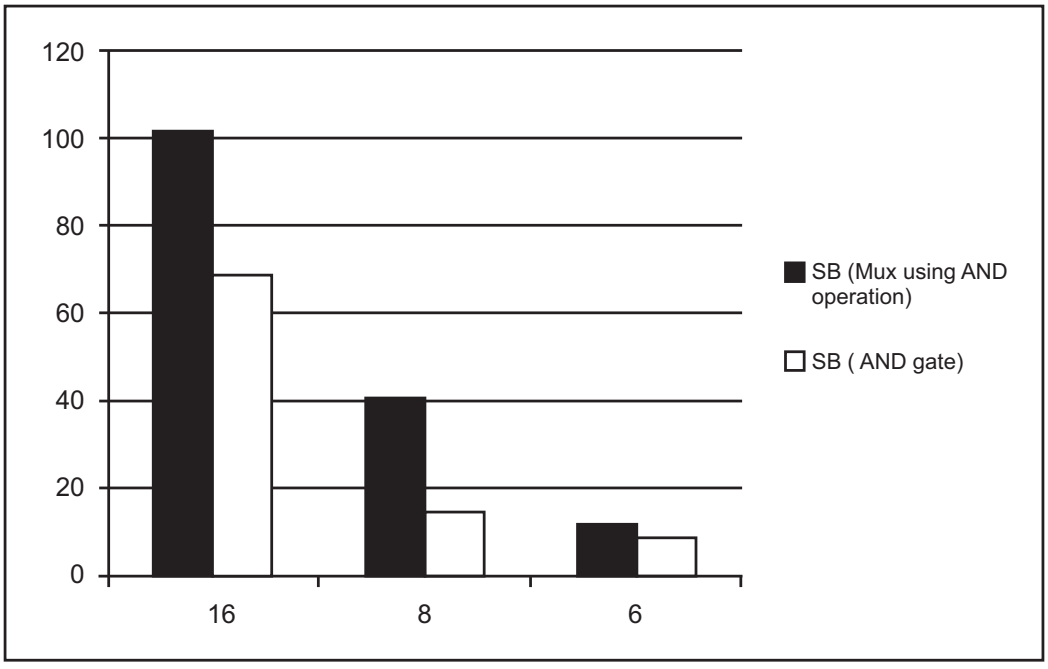

Figure 17: Maximum Throughput of CDMA NoC

5. CONCLUSION

In this paper, Standard Basis Code Multiplexer using AND operation for an on chip interconnection network has been presented. Standard basis codes are used to modulate the packet data to handle a large number of parallel data transfer. Compare to the the existing standard basis code method, the proposed standard basis code of CDMA approach provides reduction in delay, power, and area and achieves maximum throughput. A Standard Basis Code Multiplexer using AND operation for an on chip achieves very less delay than the existing method. In proposed method low number of gates is used than the existing method. So, it occupies less area than existing one. Normally multiplexer is used in many areas for data transferring. Multiplexer sends digital or analog signals at higher speed on a single line in one shared device. The Standard Basis Code Multiplexer using AND operation for an on chip interconnection network (NoC) performance is improved than the existing standard basis code method.

6. FUTURE WORK

Future work includes Design of Low Power & Reliable Networks on Chip through Joint Crosstalk Avoidance and Multiple Error Correction Coding.

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