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# A Novel Method for Compensation of Harmonics and Interharmonics in Adjustable Speed Drives

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*Abstract:* Interharmonic components are those with frequencies which are non integral multiples of the fundamental frequency of the supply. Adjustable speed drives(ASDs) are main sources of interharmonics generation in the supply system which are widely used in industries. ASDs consist of a three phase bridge rectifier using diodes, dc link and a voltage source inverter. Interharmonics have undesirable effects on other power system equipments. So it is necessary to minimize interharmonics. This paper presents a novel method for mitigation of interharmonics. In the proposedmethod, multilevel inverter is employed. A real system is simulated using PSIM. Simulation results prove the effectiveness of the proposed method.

Keywords: interharmonics, diode-clamped inverter, ASD

## **INTRODUCTION**

Increased use of power electronic converters in industrial and commercial processes has made these converters as major sources of harmonics and interharmonics. ASDs at various power levels are employed in most of the industrial applications. Fig. 1 gives the block diagram of ASD. ASD consists of a three phase bridge rectifier using diode s to convert AC input power into unregulated dc. By connecting a large capacitor across the dc link, ripples are reduced in the rectified output voltage. Then ac voltage of variable magnitude and frequency is obtained from dc voltage using a VSI [1].

When two systems operating at different frequencies are interconnected using a static frequency converter, interharmonics are generated. Static frequency converters like cycloconverters and three phase diode bridge rectifier fed voltage source inverter are sources of interharmonics. Of these, ASDs that consist of three phase diode bridge rectifier fed VSI are chief sources of interharmonics. Interharmonics can be amplified if the frequency of the interharmonic coincides with the resonance frequency of the system. Also interharmonic frequency is dependent on the load operating frequency [2],[5]. Mitigation of these interharmonics are difficult particularly minimization of extremely low frequency interharmonics[6]. Some of the impacts of interharmonics areoverheating, overstressing of capacitor banks, abnormal operation of electronic relays, telephone interference, light flicker even though its magnitude is less [1]-[4].

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Figure 1: Block diagram of ASD

Usually for ASD applications, Pulse Width Modulated (PWM) inverters are employed. Passive filtering techniques are suggested in the literature [2]. In this paper to mitigate interharmonics in the supply side, a multilevel inverter is proposed. ASD with the proposed diode clamped multilevel inverter is simulated in PSIM and the results are compared with ASD using SPWM two level inverter.

## **PROPOSED SYSTEM**

Conventional system consists of bridge rectifier using diode, dc link and PWM two level inverter. The proposed system consists of a bridge rectifier using diode, dc link and a diode-clamped multilevel inverter. Multilevel inverters are advantageous over conventional twolevel inverters that employs PWM technique. When compared to two level voltage source inverter, multilevel inverter has advantages like more efficiency and less electromagnetic interference[8]. Multilevel inverters can draw source current with low distortion and generates output voltage with low distortion [7].

## (A) Diode bridge rectifier

Three phase bridge rectifier using diode is employed as a front end converter. This rectifies input ac supply into dc. The rectified dc is fed to the inverter. Fig.2 shows the diagram of the rectifier that is employed in ASD. The rectified output has ripples and is minimized using a large capacitor in the dc link.





# A. DiodeClamped Multilevel Inverter

Multilevel inverters of different types are found in literature. Most commonly used topologies of multilevel inverter are

- 1) Diode Clamped Multilevel Inverter
- 2) Series Hbridge Multilevel Inverter
- 3) Flyingcapacitor Multilevel Inverter

Of these multilevel inverters, the most commonly used multilevel inverter is adiodeclamped multilevel inverter. Diode is used as the clamping device to achieve a stepped waveform at the output. These inverters are used for static var compensation, ASDs, interconnectinghigh voltage system. A  $3\Phi$ , 3level diodeclamped multilevel inverter is given in Fig. 3.



Figure 3 : Φ, 3 level diode clamped inverter

In diodeclampedmultilevel inverters, the diodes  $D_{a1}$ - $D_{c1}$  and  $D_{a2}$ - $D_{c2}$  used to clamp the voltage of the switch to half of the dc input voltage. The steady state voltage across each capacitor of n-level diode clamped inverteris

given by 
$$\frac{V_{dc}}{n-1}$$
.

		Table I		
Output voltage	$S_{al}$	$S_{a2}$	<i>S</i> <sub><i>a1</i></sub> ,	S <sub>a2</sub> '
V <sub>dc</sub>	1	1	0	0
0	0	1	1	0
-V <sub>dc</sub>	0	0	1	1



Figure 4: Output voltage waveform of diode-clamped three level inverter

Each phase has two complementary switches. When one of the switches of a pair is turned on, its complementary must be turned off. The possible voltage levels at the output forone phase of the inverter is listed in Table I. Each phase has two complementary switches. The pair of switches for 'a' phase are  $(S_{a_1}, S_{a_1}')$  and  $(S_{a_2}, S_{a_2}')$ . Similarly for phase b and c are  $(S_{b_1}, S_{b_1}')$ ,  $(S_{b_2}, S_{b_2}')$  and  $(S_{c_1}, S_{c_1}')$ ,  $(S_{c_2}, S_{c_2}')$  respectively.

Phase Disposition Pulse Width Modulation (PDPWM) strategy is employed for the diode clamped multilevel inverter. In this method, the carriers have same frequency, phase and amplitude but they are different in dc offset. The arrangement of the carriers are given in Fig. 5.



Figure 5

## (A) Simulation of ASD with PWM two level inverter

ASD with three phase bridge rectifier using diode, dc link and PWM two level inverter is given in Fig.6 and is simulated using PSIM. An ac choke is connected in the input side to minimize harmonics and interharmonics whose value is obtained by trial and error method. Its value is chosen to be 1mH. Increasing ac choke value beyond this value results in voltage distortion.Simulation is carried out for two different values of the drive operating frequencies.



Figure 6: ASD with two level PWM inverter

## **SIMULATION**

The parameters used for simulating the ASD system is given in Table II.

Table II				
AC Sou	rce	Induction Moto	)r	
Voltage	400V	Rated Power	40kW	
Frequency	50Hz	Rated Voltage	400V	
Resistance	8mΩ	Stator Resistance	0.394Ω	
Inductance	28µH	Stator Leakage Inductance	0.00139H	
DC Link	Rotor Resistance	0.256Ω		
Resistance	350mΩ	Rotor Leakage Inductance	0.00074H	
Inductance	0.001H	Pairs of Poles	3	
Capacitance	5000µF	Motor Operating Frequency	40Hz to 50Hz	

Rectifier input current and its spectrum obtained using FFT are shown in Fig.7 for drive operating frequency i.e.,  $f_{out} = 40$ Hz.

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Rectifier input current spectrum shows more interharmonic components inbetween fundamental frequency and fifth harmonic frequency. Fifth harmonic component is calculated which is equal to 20.13% of the fundamental current component.

Also the performance of the induction motor is analysed at this drive operating frequency of 40Hz. The input currents of the motor  $I_{\mu}$ ,  $I_{\nu}$ ,  $I_{\nu}$  along with the motor speed are given in Fig. 8.



Rectifier input current and its spectrum obtained using FFT are shown in Fig.9 for f<sub>out</sub>=45Hz.

Interharmonic component are present between fundamental and fifth order harmonic. The fifth harmonic component is found to be equal to 23.5% of the fundamental current component.

Motor performance is analysed and the input currents of the motor  $I_u$ ,  $I_v$ ,  $I_w$  along with the motor speed are given in Figure 10.

## (A) ASD with diode-clamped multilevel inverter

The proposed system of ASD with three phase bridge rectifierusin diode, dc link and diode-clamped inverter fed induction motor is simulated in PSIM. Simulation is done using the circuit shown in Fig.11.PDPWM strategy isemployed for giving triggering pulses to the devices in the diode-clamped multilevel inverter.

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Figure 10





Figure 12 gives rectifier the input current and its spectrum obtained using FFT for drive operating frequency of 40Hz.



Rectifier input current is better than that is obtained in a two level inverter. Also, rectifier input current spectrum of diode clamped inverter shows low interharmoniccurrntmagnitude between fundamental frequency and fifth harmonic. Fifth harmonic component is 15% which is less than that of the ASD with two level inverter.

Motor performance is also analysed and the corresponding results are shown in Fig.13. for the drive operating frequency of 40Hz.



Figure 13

The input current of rectifier and its spectrum obtained for a drive operating frequency of 45Hz is shown in Fig 14.

Interharmonics between fundamental component and fifth harmonics are reduced. Also the fifth harmonic component is 15% of the fundamental component.

Motor performance at a drive operating frequency of 45Hz is shown in Figure 15.



Interharmonic components in ASD employing diode-clamped MLI is compared with that of the ASD employing two level inverter and the interharmonic components magnitude are tabulated in Table III. In the table interharmonic order is specified, which can be calculated as follows.

 $InterharmonicOrder = \frac{Interharmonic frequency}{Fundamental frequency}$ 

In the table shown above, the magnitude of the supply current of ASD with diode clamped inverter is compared with that of ASD with two level inverter atthe interharmonic frequencies at the drive operating frequencies of 40Hz and 45Hz. For comparison interharmonic frequencies from 52Hz to 98Hz are considered. The magnitude of the interharmonic current is more in ASD with diode clamped inverter for interharmonic frequencies from 52Hz to 66Hz when compared to ASD with two level inverter. For interharmonic frequencies ranging from 68Hz to 98Hz, interharmonic current magnitude reduces considerably in the proposed system.

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Interhar- monic order	Interhar- monic Frequency	$f_{out}$ =40Hz		$f_{out}$ =45Hz	
		With diode- clamped MLI Current i <sub>a</sub>	With two level inverter Current i <sub>a</sub>	With diode- clamped MLI Current i <sub>a</sub>	With two level inverter Current i <sub>a</sub>
1.04	52	9.77	3.663	10.16	3.690
1.08	54	4.50	2.264	4.67	2.089
1.12	56	2.81	1.695	2.86	1.537
1.16	58	2.085	1.420	2.05	1.248
1.2	60	1.662	1.248	1.61	1.092
1.24	62	1.392	1.115	1.35	0.979
1.28	64	1.227	1.016	1.17	0.861
1.32	66	1.097	0.987	0.99	0.824
1.36	68	0.97	0.997	0.89	0.776
1.4	70	0.885	0.947	0.81	0.735
1.44	72	0.810	0.936	0.74	0.696
1.48	74	0.748	0.887	0.69	0.732
1.52	76	0.687	0.864	0.63	0.678
1.56	78	0.638	0.908	0.59	0.703
1.6	80	0.615	0.928	0.54	0.711
1.64	82	0.557	0.963	0.51	0.710
1.68	84	0.539	1.000	0.47	0.731
1.72	86	0.511	1.102	0.46	0.716
1.76	88	0.486	1.198	0.43	0.769
1.8	90	0.510	1.247	0.41	0.856
1.84	92	0.479	1.285	0.41	0.940
1.88	94	0.466	1.257	0.39	1.033
1.92	96	0.450	1.222	0.39	1.075
1.96	98	0.422	1.228	0.389	1.028

Table III

The comparison between two level inverter and diode clamped inverter for an output frequency of 40Hz is shown in Fig.16.





The comparison between two level inverter and diode clamped inverter for an output frequency of 45Hz is shown in Fig. 17.



Comparison chart 2

#### Figure 17

# CONCLUSION

In this work, the presence of interharmonicsis analysed in the input current of the rectifier employed in ASD and its effects are described. ASD with two level inverter employing PWM technique is simulated in PSIM and the results are discussed. A novel method is proposed which has a diode clamped multilevel inverter instead of two level inverter. The proposed method is simulated in PSIM and the results are compared with those obtained using two level inverter. The proposed method shows better results which has lower interharmonic magnitude and reduced fifth order harmonic.

## REFERENCES

- [1] Gary W. Chang, *Senior Member, IEEE*, and Shin-Kuan Chen, *Student Member, IEEE*, "An Analytical Approach for Characterizing Harmonic and Interharmonic Currents Generated by VSI-Fed Adjustable Speed Drives," *IEEE* Transactions on Power Delivery, vol. 20, no. 4, October 2005.
- [2] D.Uma, K.Vijayarekha, "Mitigation of Harmonics and Interharmonics in VSI-Fed Adjustable Speed," International Journal of Engineering and Technology (IJET) 2013.
- [3] A. Testa, M. F. Akram, R. Burch, G. Carpinelli, G. Chang, V. Dinavahi, C. Hatziadoniu, W. M. Grady, E. Gunther, M. Halpin, P. Lehn, Y. Liu, R. Langella, M. Lowenstein, A. Medina, T. Ortmeyer, S. Ranade, P. Ribeiro, N. Watson, J. Wikston, and W. Xu, "Interharmonics: Theory and Modeling," IEEE Transactions on Power Delivery, vol. 22, no. 4, October 2007.
- [4] *G.* W. Chang, *Senior Member, IEEE*, and S. K. Chen, *Student Member*, "Characterizing Harmonic and Interharmonic Currents Generated by the VSI-Fed AdjustableSpeedDrives," *IEEE*, International Conference on Power System Technology, November 2004.
- [5] Dahai Zhang, WilsunXu, *Fellow, IEEE*, and Yutian Liu, *Senior Member, IEEE*, "On the Phase Sequence Characteristics of Interharmonics," *IEEE* Transactions on Power Delivery, vol. 20, no. 4, October 2005.

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- [6] Seyed Reza Hadian Amrei, Dian GuoXu, "Harmonics and Interharmonics Generation in General VSI/CSI Inverters: A New Approach," Senior Member, IEEE, and Y. Q. Lang.
- [7] SurinKhomfoi and Leon M. Tolbert,"Chapter 31 Multilevel Power Converters," The University of Tennessee.
- [8] José Rodríguez, Senior Member, IEEE, Jih-Sheng Lai, Senior Member, IEEE, and Fang Zheng Peng, Senior Member, 2002, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications," IEEE, 2002.

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