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Hybrid topology of symmetrical multilevel inverter using less number of switches

D. Venkata Manikanta[1], Gurpreet Singh[2], K. Pramod[3] and R.K. Sharma[4]

ABSTRACT

Step by venture, there are an extensive topologies that have been distributed for the multilevel inverters. The primary thought of these topologies is to diminish the equipment intricacy in the MLIs which can be proficient by decreasing the switches, dc voltage sources voltage push crosswise over switches and misfortunes. Other than traditional topologies, a few late topologies accomplished in this with various voltage yield steps. A symmetrical multilevel inverter is proposed in this paper which not just decreases the multifaceted nature than established and late topologies additionally lessens the size, cost, and many-sided quality and improves general execution by having just seven switches fit for creating 7, 9 and 11 levels of yield voltage alongside diminishing the voltage focuses over the high power switches. To exhibit this proposed topology and examination contrasting and the customary and late distributed topologies in each viewpoint like semiconductor switches, control diodes, necessity, Direct current sources and voltage blocking is finished. Multiple-transporter PWM system is for the most part utilized for producing beats and the reproduction of this topology is made utilizing Matlab/Simulink and tentatively the achievability of the topology has performed.

1. INTRODUCTION

Multi-level inverter was initially presented in 1975, which acquires a fast development the DC/AC control transformation and related applications [1]. The HVDC control transmission, uninterruptible power supplies (ups), AC engine drives, half and half electric vehicles and dynamic channels are relying upon MLIs. MLIs close to having great quality of power, THD is less and decrease in voltage focuses over on switches, its disadvantage is increment in the yield levels and the quantity of semiconductor switch necessity alongside peripherals gadgets like door driver circuit, assurance circuit and warmth sink. Expanding circuit builds multifaceted nature as well as cost, which thusly diminishes the effectiveness and dependability. Topologies of multi-level inverters, for example, flying capacitor, fell H-extension and nonpartisan point clipped and so forth are characterized as for their advantages and disadvantages [15] are as one called "Traditional Topologies". The traditional MLI, CHB gets wide consideration due to measured quality and straightforwardness. Be that as it may, the necessity of disengaged source is a confinement of the topology [16]. A CHB MLI is made out of a few H-connect cell and segregated DC source. In light of voltage extent of DC source, CHB is named symmetrical and lopsided arrangement. In symmetric setup, DC sources sizes are equivalent (V1 = V2 = V3… .), however in unbalanced arrangement, DC sources are not equivalent in size (V1 ≠ V2 ≠ V3… .). The lopsided design of CHB for the most part delivers a bigger number of voltage levels than symmetric setup for similar number of force switches [15]. Topologies and control plans proposed

[1] M.Tech (EEE)/Lovely Professional University, *Email: dasarivm@yahoo.in*

[2] M.Tech (EEE)/Lovely Professional University, *Email: gurprit1994@ymail.com*

[3] B.Tech (ECE)/Pragathi Engineering College, *Email: crazypramod@gmail.com*

[4] Assistant Professor /Lovely Professional University, *Email: rk.sharma@lpu.co.in*

with diminished gadget number uses a mix of unidirectional and bidirectional switches of various evaluations are looked into quickly in [15–40].

In [16–21], similar topologies of MLIs are examined. Deviated topologies of MLI with diminished number of switches are exhibited in [22–35]. The fundamental prerequisite are huge number of bidirectional switches which is a noteworthy issue in this. Another topology is further improved in [33]. with number of switches decreased [32] With proposed calculations, the primary constraint of these topologies is that every one of the means (added substance and subtractive) can't be accomplished. Other topology of MLI having a few bidirectional switches is preferred in [34]. In [35], the topology having diminished switches is initiated, yet need of substantial number of DC voltage sources is the principle downside of the topology. Topology of MLI introduced in [36] utilizes low-recurrence high power switches as a result of which there is a nearness of lower request sounds in yield waveform which is the principle downside. In [37, 38], the multi-twisting transformer in this topology causes high cost and multifaceted nature of general topology. A four-level topology of inverter is exhibited in [39], however the introduced topology can't give zero-voltage level, which brings about high r.m.s qualities and symphonious vitality is aggregated at exchanging recurrence. [40] Another topology of MLI is exhibited, however the topology requires switches of various evaluations. The topology is introduced for five-level by using four DC sources, though in routine topologies it can reach up to nine-level by using four DC sources. Despite the fact that MLI topologies are guaranteeing higher yields levels with lessened number of switches, However, awesome bargain has been made as far as measured quality, effortlessness, number of switches, assortment of DC source, dependability and misfortunes.

The utilization of halter kilter converters are not reasonable for mechanical applications because of measured quality is lost and has distinctive sort of semiconductors In this paper, new topology of symmetrical MLI is proposed which utilizes hexagon switch cell (HSC) fit for creating 7-/9-/11output levels by using seven controlled switches having a particular structure and offering dependable operation with diminished voltage focuses over the switches. Assortment of DC source is adjusted utilizing capacitor voltage. The symmetrical design of proposed topology creates higher number of yield voltage levels with nearly less number of switches. The quantities of bidirectional changes additionally lessens, all things considered, in the topology proposed.

In second section, the suggested topology-I and II of MLI for symmetrical setup is clarified and its performance is given. Segment 3 manages the reenactment and exploratory consequences of the initiated topologies. Segment 4 gives the examination of uniform topology to the past topologies. At long last, Section 5 is conclusion.

2. PROPOSED MLI TOPOLOGIES

2.1. Topology-I

The arrangement of topology-I is represented in Fig. 1a comprising of two DC voltage source VS1 and VS2, alongside capacitor C1 and C2 which shapes a voltage divider circuit. A controlled switch S7 and four diodes D7, D8, D9 and D10 which are associated with HSC contained six switches S1, S2, S3, S4, S5 and S6 frames a helper switch. On the off chance that the DC voltage sources are equivalent i.e. VS1 = VS2' then it can be alluded to as symmetrical MLI generally topsy-turvy. Topology-I is fit for delivering 7-/9-/11-level yield with certain mix of DC voltage source while joining just seven controlled switches. The yield voltage level with specific mix of DC voltage sources is given in Table 1. The summed up type of proposed topology-I is appeared in Fig. 1b.

To assess add up to number of part check, the topology-I is contrasted and established topologies for nine-level yield and condensed in Table 2.

Table 1
Different combinations of DC voltage source for higher output voltage levels

Algorithm	Values of DC sources	No. of output levels	Configuration
first VS1	=	2 × VS2	7 asymmetrical
Second VS1	=	VS2	9 symmetrical
Third Vs1	=	xV s2	11 symmetrical

Table 2
Comparison of different nine-level inverter topologies for symmetrical MLI

Components	*Proposed topology-I*	*NPC*	*FC*	*CHB*
main power switches	6	16	16	16
auxiliary switch	1	0	0	0
diodes	10	72	16	16
capacitors	2	8	36	–

Table 3
Different switching states of topology-I for nine-level output

Output levels, V	*'ON' state switches*	*Conducting diodes*
1	S_4, S_7	
2	S_4, S_5	D_6, D_7, D_{10}
3	S_4, S_5, S_7	D_2, D_7, D_{10}
4	S_1, S_4, S_5	–
0	–	–
–1	S_3, S_7	D_5, D_8, D_9
–2	S_3, S_6	D_1, D_8
–3	S_3, S_6, S_7	D_9
–4	S_2, S_3, S_6	–

Table 4

Output levels, V	*'ON' state switches*	*Conducting diodes*
1	S_4, S_7	D_6, D_7, D_{10}
2	S_1, S_4	D_6
3	S_1, S_4, S_5	–
0	–	–
–1	S_3, S_7	D_5, D_8, D_9
–2	S_2, S_3	D_5
–3	S_2, S_3	D_6

Table 5

Output levels, V	*'ON' state switches*	*Conducting diodes*
1	S_4, S_7	D_6, D_7, D_{10}
2	S_1, S_4	D_6
3	S_4, S_5	D_2
4	S_4, S_5, S_7	D_7, D_{10}
5	S_1, S_4, S_5	–

(contd... Table 5)

Output levels, V	*'ON' state switches*	*Conducting diodes*
0	–	–
–1	S_3, S_7	D_5, D_8, D_9
–2	S_2, S_3	D_5
–3	S_3, S_6	D_1
–4	S_3, S_6, S_7	D_8, D_9
–5	S_2, S_3, S_6	–

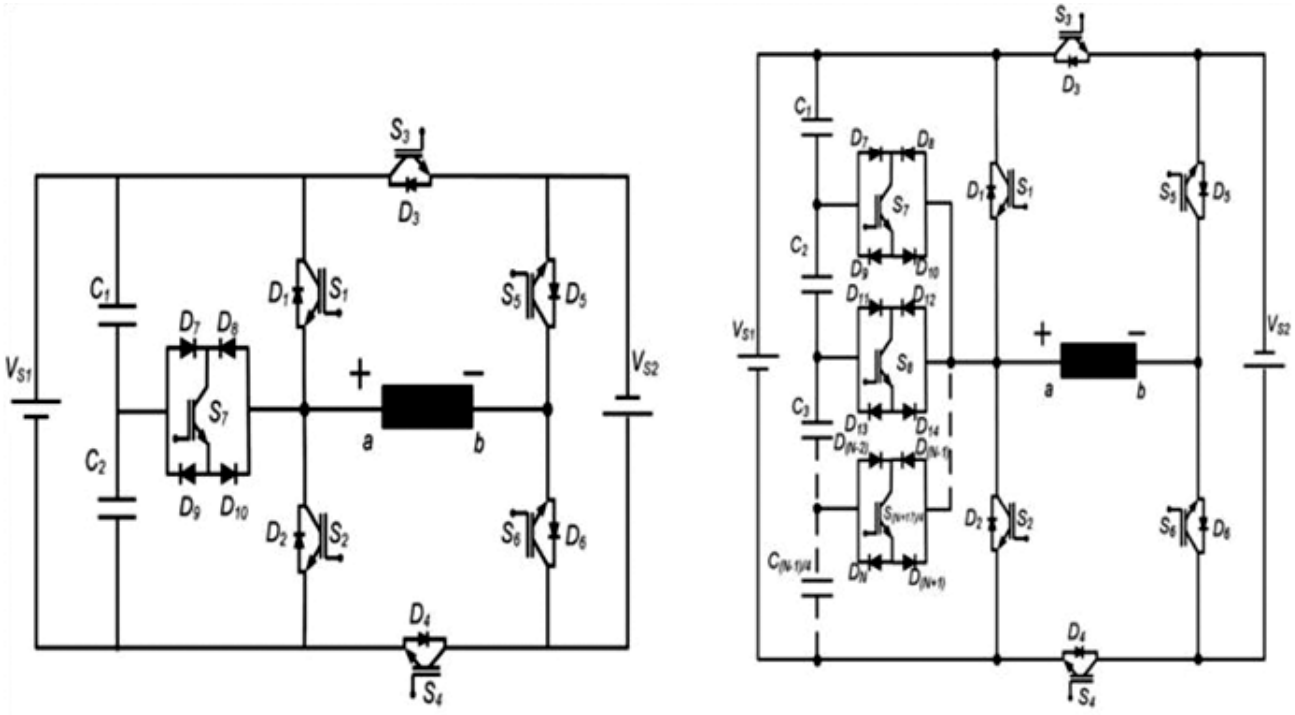


Figure 1: Configuration and generalization of nine level MLI

Principle control exchanging: The proposed topology-I accomplishes 56.25% (7 rather than 16) lessening in number of fundamental power switches while contrasted and the established topologies in symmetrical arrangement.

Power diodes: Compared with FC and CHB, the proposed topology-I in symmetrical arrangement accomplishes 37.5% (10 rather than 16) decrease in the quantity of diodes required, though rate of lessening increments to 86.11% (10 rather than 72) as contrasted and NPC. So also, it accomplishes 74% (2 rather than 8) lessening in capacitor numbers utilized, required when contrasted and the NPC and 94.44% (2 rather than 36) diminishment when contrasted and the FC.

For a nine-level inverter, the working modes and diverse exchanging states alongside yield voltage levels are given in Fig. 2 and Table 3. So also, the different exchanging conditions of topology-I in unbalanced setup for incorporating 7-level and 11-level are outlined in Tables 4 and 5.

$$\text{Total number of controlled switches required} = (N + 19)\ 4\ 4 \quad (1)$$

$$\text{Total number of diodes required} = (N + 1) \quad (2)$$

$$\text{Total number of DC sources required} = 2 \quad (3)$$

$$\text{The number of capacitors required} = (N - 1)\ 4\ 4 \quad (4)$$

$$\text{number of controlled switches required} = \frac{7}{8} \times (N-1) \tag{5}$$

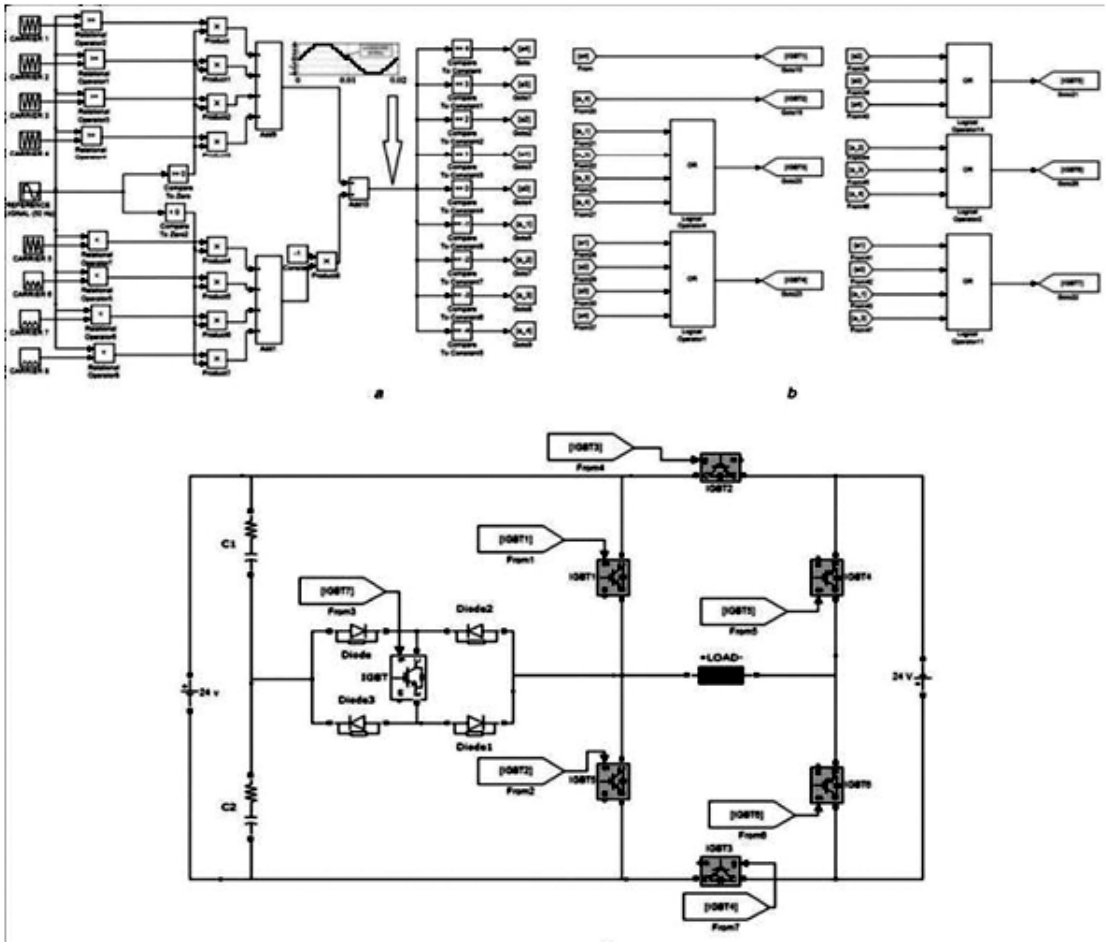
$$\text{number of diodes required} = \frac{5}{4} \times (N-1) \tag{6}$$

$$\text{number of DC sources required} = \frac{1}{4} \times (N-1) \tag{7}$$

2.2. Proposed topology-II, that is, proposed cascade connected

2.2.1. MLI

Ventured waveform is integrated by the MLI comprising of the information DC levels and their added substance and additionally subtractive blends. The voltage waveform has different "levels" with both "positive" and "negative" polarities (in positive and negative half cycles, separately). With one and only extremity, a MLI topology orchestrates various levels and H-scaffold is utilized as extremity converter as displayed in [17–20, 24, 26, 30, 33–35]. These parts are alluded as "level-era part" and "extremity era part". For the extremity era part, the base voltage rating is equivalent to the working voltage of the MLI required for the power switches. Henceforth, the H-scaffold is utilized as extremity generator as a part of the topologies exhibited in [17–20, 24, 26, 30, 33–35] and the switches utilized as a part of H-extension must have the capacity to endure the voltage equivalent to appraised yield voltage of MLI. The four switches of H-extension topology confines the utilization of exhibited topologies for high voltage by turning "ON" and "OFF" once amid a principal cycle. While contrasting and four of those topologies introduced in



[17–20, 24, 26, 30, 33–35], proposed topology-I have just two switches (S3 and S4) to hold up under the full evaluated voltage which are low-recurrence high-voltage switches turning "ON" and "OFF" once amid a central cycle, thus exchanging and conduction misfortunes diminishes by extensive sum. Since S3 and S4 need to endure the full appraised voltage which opposes the use of proposed topology-I in higher voltage applications a course association of the proposed topology-I is utilized which is proposed topology - II appeared in Fig. 3 to beat the issue. This course association of a few crucial cells can be worked for higher voltage applications in symmetrical setup.

Fig. 3 is a change of topology-I with a specific end goal to defeat the issue of voltage push over the switches so that the proposed topology can be connected in higher voltage application. Topology-II is additionally made out of one assistant change associated with HSC. The proposed circuit is provided by two capacitors alongside two DC voltage source. Every cell in course association contains seven controlled switches, ten power diodes, two DC sources and two capacitors.Multi-carrier PWM technique is used for modulation. In multi-carrier PWM scheme, the carrier signal is compared with the reference signal and pulses so obtained are used for switching of devices with respective voltage levels. By increasing the number of carriers is directly proportional to the number of level increase. Carrier frequencies of 100 and 5000 Hz and a reference signal of frequency 50 Hz is used for experiment here.

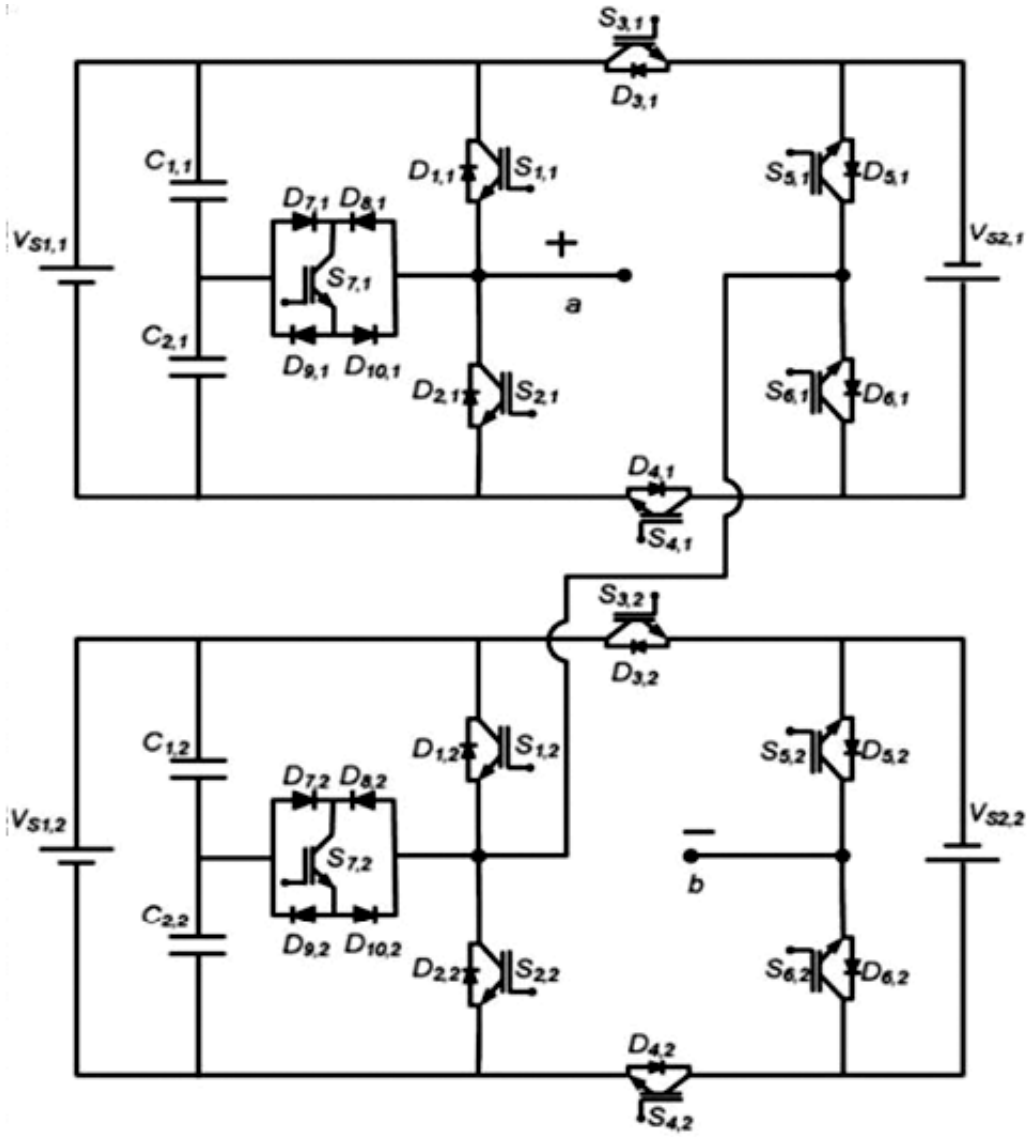


Figure 3:

2.2.2. Simulation results

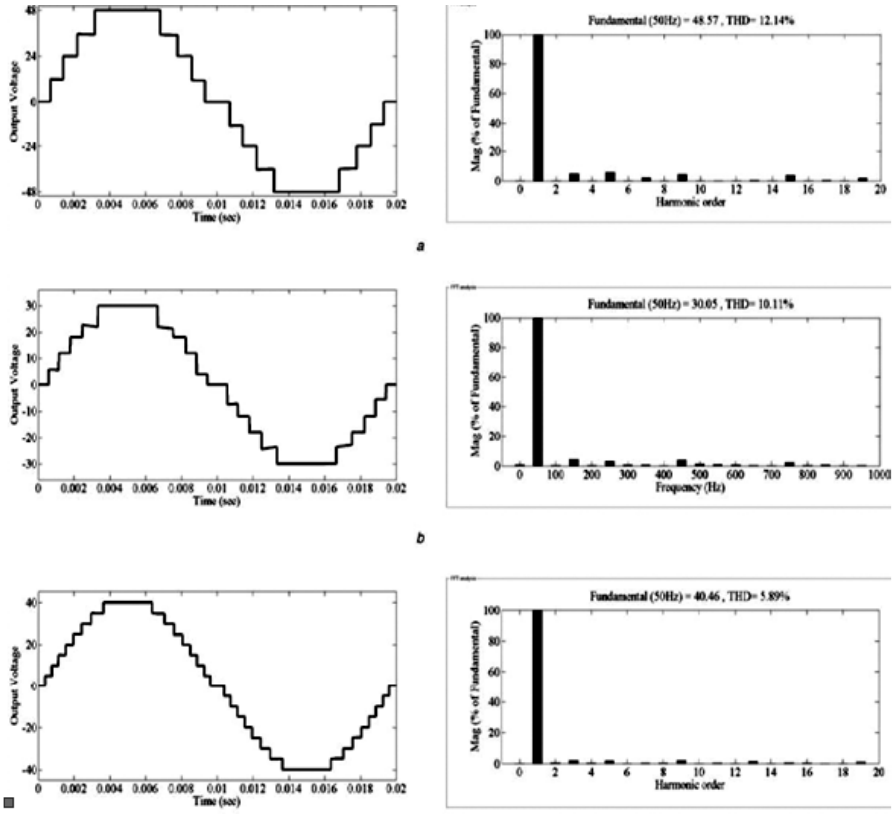


Figure 4:

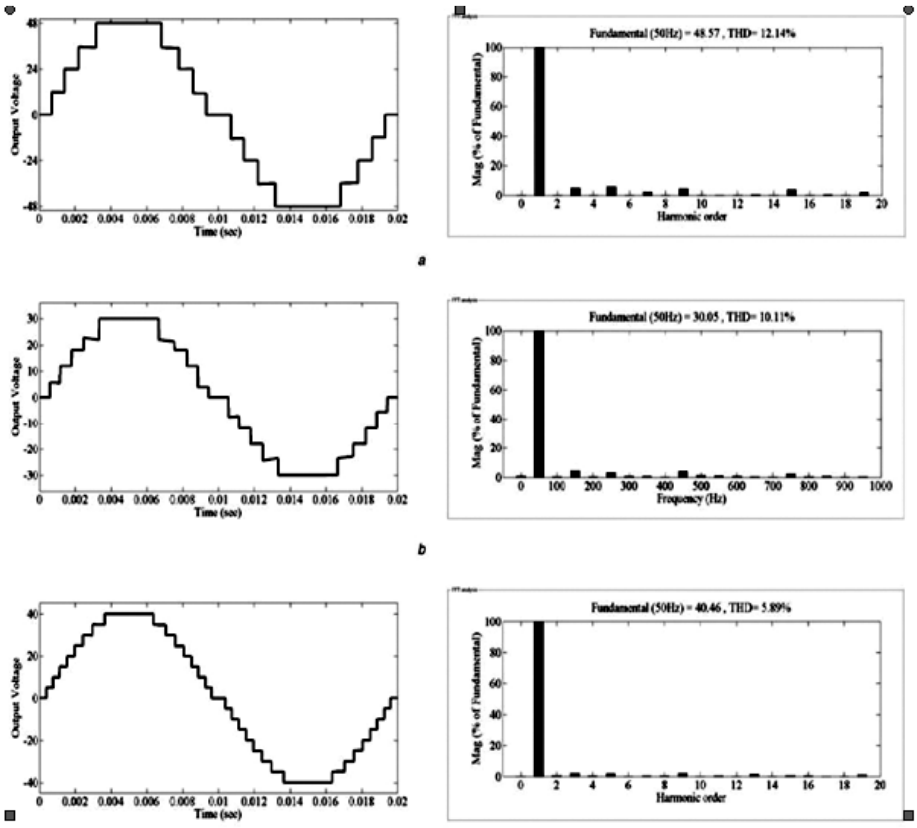


Figure 5:

3. MODULATION SCHEME

Multi-transporter PWM method is utilized for adjustment. In multi-bearer PWM conspire, the transporter flag is contrasted and the reference flag and heartbeats so acquired are utilized for exchanging of gadgets with particular voltage levels. By expanding the quantity of transporters is straightforwardly corresponding to the quantity of level increment. Transporter frequencies of 100 and 5000 Hz and a reference flag of recurrence 50 Hz is utilized for investigation here.

Topology-I is recreated in symmetrical and unbalanced arrangements as 9-level and 11-level inverters. Fig. 5. Speaks to Simulink square graph for nine-level proposed-I topology. Fig. 5a demonstrates the exchanging technique utilized for nine-level inverter, Fig. 5b demonstrates the rationale operations so as to get door heartbeats and Fig. 5c demonstrates the Simulink model of proposed-I nine-level inverter. The reenactment result is at 100 Hz transporter recurrence for 9-level and 11-level inverters with comparing THD are appeared in Figs. 6a and b. Topology-II in symmetrical design is recreated with a specific end goal to acquire 17 level. Fig. 6c demonstrates reproduction result for 17-level. Fig. 6d demonstrates the adjusted voltages on arrangement associated capacitors for 9-/17-level inverters. The reproduction result at 5000 Hz transporter recurrence for nine-level inverter is given in Fig. 7 at various balance file. An examination of THD got for both topology-I and topology-II

Table 6
Analysis of THD for 9-/11-/17-level inverters

MLI topology	*Controlled switches*	*Output levelsSimul*	*ated THD, %*
topology-I symmetric	7	9	12.14
topology-I asymmetric	7	11	10.11
topology-II symmetric	14	17	5.89

3.1. Experimental results

An experimental setup of the proposed 9-level and 11-level inverters has developed and experimentally validated for proposed topologies. A dSPACE DS1103 real-time digital controller for generating switching pulses. To provide DC voltages two identical 24 V batteries for 9-level inverter and two batteries of 12 V and 18 V for 11-level inverter are used. The waveforms obtained by two different carrier frequencies of 100 and 5000 Hz shown in Fig. 8 are measured and recorded by using power quality analyzer (Fluke 434-II) and Agilent's dual channel oscilloscope.

The experimental output voltage waveform with corresponding THD for proposed-I nine-level inverter at carrier frequency of 100 Hz and the current waveform and the voltage across two capacitors are shown in Fig. 8a and Fig. 8b and shows the experimental results obtained at the carrier frequency of 5000 Hz along with the output voltage, current and capacitor voltages for nine-level inverter at modulation index of 1.0 and 0.8, respectively. Fig. 8c shows the output voltage waveform for 11-level inverter along with its corresponding THD. Voltage balancing is not an issue in proposed I topology as both the capacitors maintain $V_{DC}/2$ (i.e. 12 V each) voltage. Irrespective of modulation and switching frequency, the voltage across the capacitors always remains balanced which can be observed from Figs. 8a and 8b.

4. COMPARISON STUDY

In symmetrical setup the proposed Topology-I has predominant execution as contrasted and topology-II and rest of alternate topologies since it requires minimal measure of changes to produce specific yield levels yet for application of high-voltage, topology-II is most appropriate as topology-I is not a perfect one since two (S3 and S4) need to hold up under extremely appraised inverter voltage.

A correlation in view of number of yield levels versus the quantity of IGBTs required is made between proposed topology-I and topologies exhibited in [17–21, 31] and plotted in Fig. 9a. Also, diodes required in Topology-I is less contrasted and [17, 18, 20, 31] topology-II and equivalents to topologies displayed in [19, 21] as appeared in Figure. DC sources required is fundamentally less as contrasted and the as of late proposed topologies as portrayed in Fig. 9c. So with the least number of switches, less driver circuits,less diodes and DC sources alongside minimal effort, many-sided quality and size, the proposed topology-I creates higher number of yield levels.

In any case, the primary disadvantage of topology-I is that two of the switches in this circuit limits the application of high-voltage which additionally happens in topologies displayed in where four changes need to hold up under the full evaluated voltage which constrains their applications for high-voltage applications.in topology-I the issue of bearing the full appraised voltage by two switches can be understood by topology-II where the fell association is utilized. The two proposed topologies are utilized which are reliant upon the kind of use i.e. for low-to-medium voltage application topology-I is most appropriate and topology-II is favored for high-voltage application. DC source prerequisite is best among the other thought about topologies, and consequently offers decreased cost and intricacy. The nitty gritty rundown of examination of aggregate number of part required is displayed in Fig. 9d and Table 8 where "N" indicates number of yield levels.

5. CONCLUSION

In this paper, symmetrical configuration of MLI topology and modification of topology-I to topology-II for a wide range of application (i.e. medium–to-high voltage) and its operation is explained. The topology-I in symmetrical configuration is presented and a comparison is drawn for nine-level inverters and also symmetrical configuration for the proposed topology-II is given along with its operating states. When compared with conventional ones and other topologies recently presented, these proposed topologies reduce the number of controlled switches significantly. A wide range of comparison is made between the proposed topology and some of the recent published topology which shows that these topologies with minimum number of IGBTs, diodes, capacitors and blocking voltage of switches the output voltage is obtained up to maximum number of levels. Finally, verified through simulation.

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