

A Novel Reversible n -Bit Counter for Low Power Quantum Computing

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Abstract : Reversible logic in quantum computing and nanotechnology provides solution to optimize the power which can be used in a variety of low power applications such as CMOS VLSI design, and optical computing. This paper proposes a new reversible n -bit counter circuit based on reversible T flip-flop, FG & PG logic gates. Experimental and simulation results prove that the efficiency of the circuit is majorly improved as the delay that occurs in each of the components in the circuit is minimized. The performance of the circuit in terms of delay aspect is well addressed in the proposed design, thus opening up more avenues to design further complex arithmetic systems using reversible logic.

Keywords : Reversible logic gates, Synchronous Counter, Low power, CMOS, Quantum computing.

1. INTRODUCTION

Major thrust is being given to the design, implementation, and analysis of logic circuits that are reversible, in the area of research. The idea of reversible logic is increasingly employed in the areas of low power VLSI design, nanotechnology, quantum computing and optical computing. As the complexity in CMOS VLSI circuits increases, the dissipation of power in the circuit becomes a major challenge in the design. Due to loss of the information, there will be dissipation of energy and consumption of power in irreversible logic circuits. It was demonstrated by Landauer (1961)[1] that heat energy of $kT \cdot \log_2$ joules is dissipated when there is a loss of each bit of information, where the absolute temperature is represented by T (measured in Kelvin) and k is the Boltzmann's constant ($1.38 \times 10^{-23} \text{ m}^2 \text{ Kg s}^{-2} \text{ K}^{-1}$) respectively. The power dissipation depends on the information lost or number of bits erased during computation. It was shown by Bennet [1973] that logic circuits with zero power dissipation are possible only if the circuits comprises of gates that are reversible [2]. The state of the output prior to and during present output transition must be known to perform a non-dissipative transition of the output. The presence of the copy of the state of the output all through the computation can be obtained by the use of reversible logic. Circuit constructed using Reversible logic does not erase or lose information. Systems comprising of reversible gates only allow reversible computation. Further, quantum computing also use concept of reversible logic. Rather than manipulating the pure logic values, the Quantum gates manipulate qubits and are reversible [3]-[7]. A 2-D complex Hilbert space describes a 2-level quantum system, called qubit. The logic 0 and logic 1 values are represented by the two orthogonal quantum states. A number of elementary quantum gates constitute a quantum circuit and a reversible logic gate can be decomposed into such a circuit.

Generally compared to the input bits in majority of computing tasks, the output bits are small in number. In applications such as computer graphics, cryptography, digital signal processing and communication, the information extracted at the output need to be same as that encoded in the input. Hence reversible gates are considered in the circuits for implementing such networks.

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A Boolean function that is completely specified, describing a logic network with n -inputs and n -outputs would be reversible if each unique output pattern is mapped to each input pattern. The mapping helps in identifying the outputs of the circuit from the inputs and also helps the recovery or retrieval of inputs back from the outputs. The primary requirement for an ' n ' input, ' k ' output logic expression to be reversible is that the values of ' n ' and ' k ' must be equal. Constant Inputs (CI) are the additional inputs added to fulfill this requirement. Similarly, the additional outputs that are not used further in the computation, in the reversible circuits are called the Garbage Outputs (GO). The primitive 2 X 2 and 1 X 1 gates used in the quantum circuit of the reversible network gives the quantum cost. The major drawback in the implementation of reversible logic networks is that feedback of output and fan out are not permitted. This has to be achieved using additional gates.

Computation of delay of any circuit is an important parameter as it affects the speed of the circuit and thus the efficiency. The time taken for a circuit to respond to the changes in the input is called delay. According to reference [8], delay of the reversible circuit through which an input signal has to traverse, is computed by finding the number of primitive 2 X 2 and 1 X 1 gates which constitute the design. Delay through primitive 2 X 2 and 1 X 1 gates is assumed to be equal to unit delay (1Δ).

In this paper a Reversible n -bit synchronous counter is proposed. This design forms the basis for sequential circuits that are reversible. For the purpose of simplicity, analysis and illustration a 4-bit synchronous counter is implemented using the proposed design methodology. The parameters, quantum cost, hardware complexity, reversible gates used, computational delay, garbage outputs, and constant inputs, are optimized to a large extent in the 4-bit reversible counter that is proposed in this paper. Adequate care has been taken during connections of the gates so that the delay is minimized. In section 2 & 3, preview of Reversible gates used and the design of proposed counter is discussed followed by simulation results, analysis, and conclusion in section 4 & 5 respectively.

2. REVERSIBLE LOGIC GATES

Many reversible logic gates are available in literature and few of them are discussed in this section with respect to quantum cost, input and output vectors.

- A two-bit reversible gate called Feynman gate (FG) [8] has quantum cost of one and its input & output vectors are $I_v = (X, Y)$ & $O_v = (M, N : M = X, N = X \oplus Y)$ respectively (Fig 1a).
- Toffoli gate (TG) [8] is a three-bit reversible gate whose input & output vectors are $I_v = (X, Y, Z)$ & $O_v = (L, M, N : L = X, M = Y, N = X \oplus Z)$ respectively and the quantum cost is five (Fig 1b).
- Fredkin gate (FRG) [8] is a three-bit reversible gate whose quantum cost is five and has input & output vectors as $I_v = (X, Y, Z)$ & $O_v = (L, M, N : L = X, M = \overline{X}Y + XZ, N = XY + \overline{X}Z)$ respectively (Fig 1c).
- Peres gate (PG) [8] is a three-bit reversible gate with input vector $I_v = (X, Y, Z)$ and output vector $O_v = (K, L, M : K = X, L = X \oplus Y, M = X \oplus Z)$. Its quantum cost is 4 (Fig 1d).
- SRK gate [9] is a 3-bit reversible gate with input vector $I_v = (X, Y, Z)$ and output vector $O_v = (K, L, M : K = X, L = X \oplus Y \oplus Z, M = \overline{X}Y \oplus XZ)$. Its quantum cost is 4 (Fig 1e).
- DKGP gate [10] is a 4-bit reversible gate (Fig 1f) with input vector $I_v = (D, E, F, G)$. Its quantum cost is 15 and is calculated directly from the quantum circuit. If quantum circuit is reduced using optimization techniques, the Quantum cost of the whole design can be lowered. Its output vector is given as:

$$O_v = (J, K, L, M : J = D \oplus F, K = E, L = E \oplus F \oplus G), \\ M = D \oplus (D \oplus F) (D \oplus G) \oplus E(F \oplus G)$$

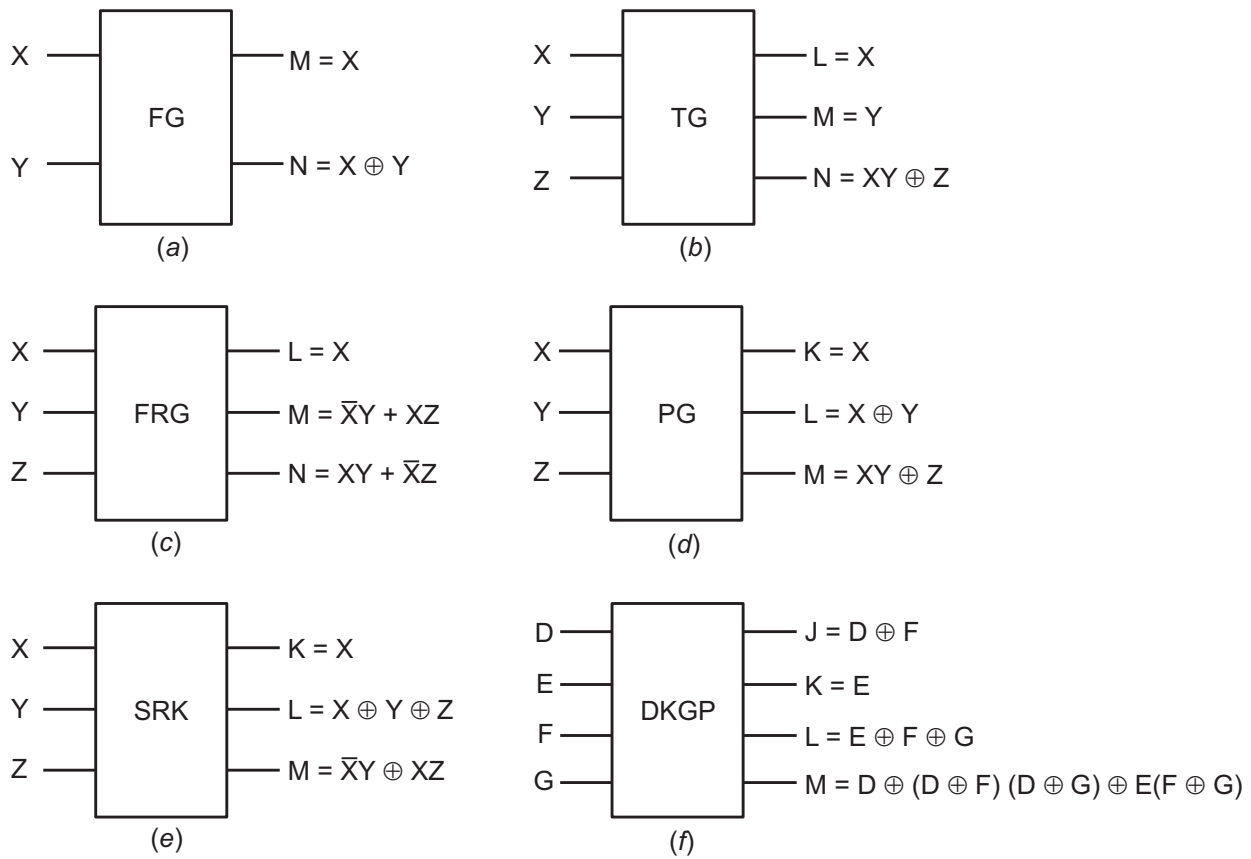


Figure 1: (a) Feynman (FG) (b) Toffoli (TG) (c) Fredkin (FRG) (d) Peres (PG) (e) SRK (f) DKGP gates

3. PROPOSED REVERSIBLE N -BIT AND 4-BIT SYNCHRONOUS COUNTER

In general, a counter is a register which produces specified output sequence or counts the clock pulses arriving at the clock input. It has wide variety of applications in almost all the areas, to name a few, industrial, domestic, security surveillance and communication. The important feature of the counter circuit is that different subsystems of a digital system can be controlled using the sequence generated; timing signals can be generated and clocks of different frequencies can be generated. There are a variety of counters available. They can be classified as synchronous and asynchronous counters based on clock input, positive edged or negative edged based on the clock trigger, binary or decade counter based on the counts, up, down or up/down counter based on the direction of the count, and JK, T or D based on the Flip-flops used in the counter circuit.

Primitive logic blocks used in counters are Flip flops and combinational gates. Asynchronous or ripple counter does not use common clock and output of a stage effects the clock input of next stage. In Synchronous counters, simultaneously clock is given to all the flip flops. A count comprises of 'n' bits which do not change simultaneously, but synchronously at the rising or falling edge of clock depending on the type of edge triggered Flip flops used in the counter.

The proposed n -bit synchronous counter is based on reversible Feynman (FG), Peres gate (PG) and T Flip-Flops. In turn, the T Flip flop is designed using Feynman (FG) and Peres gate (PG). For simulation and illustration purpose a simple 4-bit synchronous counter was designed which counts through the states 0000, 0001, 0010, ..., 1110, 1111, 0000, 0001, ... for every clock pulse that arrives at its clock input. The proposed designs of n -bit and 4-bit synchronous counters (RTL schematic) are shown in Fig 2 and Fig 3 respectively. Fig 4 represents the quantum circuit of the 4-bit synchronous counter proposed in this paper, which is used to make the calculation for improvement parameters. The functionalities of reversible FG, PG, T Flip flop and the proposed 4-bit counter are explained briefly below.

- Feynman gate (FG) [8], a two-bit reversible gate whose quantum cost is one (Fig 5) and has input & output vectors as $I_v = (X, Y)$ & $O_v = (M, N : M = X, N = X \oplus Y)$ respectively. When a logic 0 is given as Y input to FG gate, then this gate can be used to overcome the fan out problem as $M = N = X$. If Y input is logic 1, $M = X, N = \bar{X}$ or the complemented input is obtained as the output.
- Three-bit reversible Peres gate (PG) [8] has a quantum cost of 4 and input vector of $I_v = (X, Y, Z)$ and output vector $O_v = (K, L, M : K = X, L = X \oplus Y, M = X \oplus Z)$. The Peres (PG) gate is shown in Fig 6.

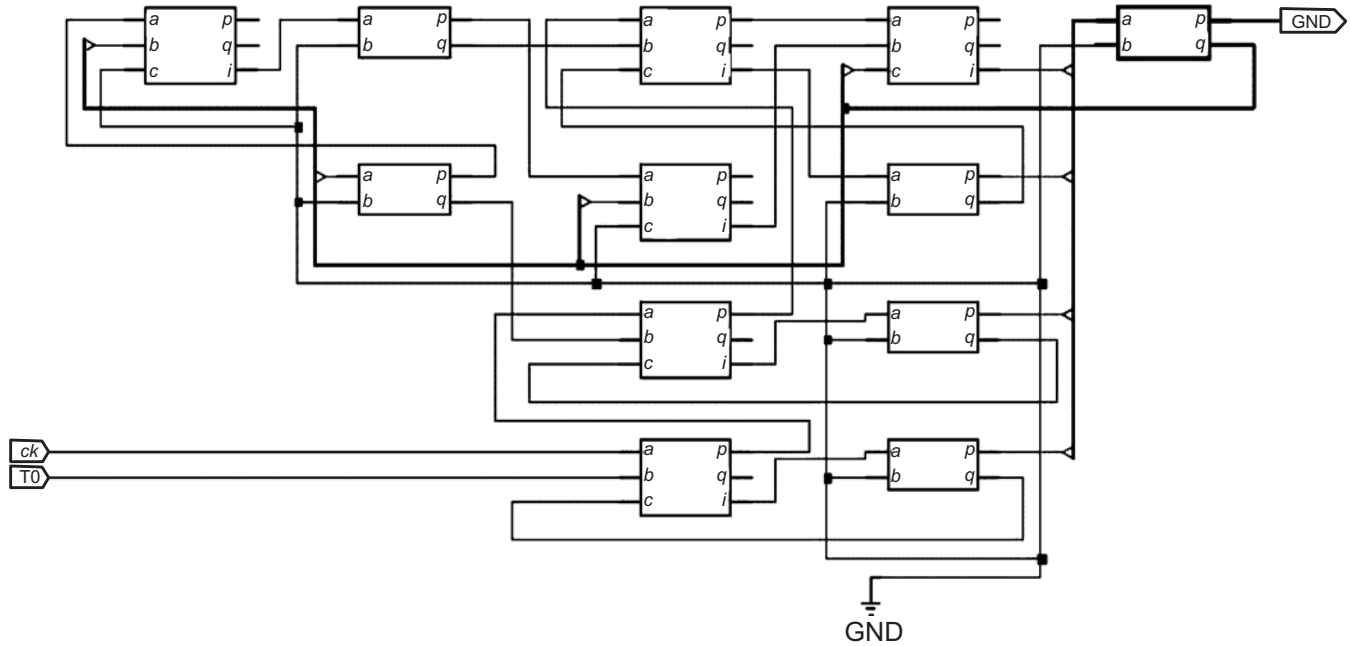


Figure 2: RTL schematic of Proposed reversible 4 bit counter

The characteristic equation of a T Flip-Flop is given as $Q^+ = (T.CLK) \oplus Q$. It toggles whenever the T input is logic 1 and the clock is asserted. The given expression can be realized using an AND gate and an EXOR gate. The reversible T Flip-Flop [8] consists of a PG and an FG gates as shown in Fig 7, where PG gate acts as a reversible AND gate and FG gate as a reversible EXOR gate. The garbage outputs, quantum cost, and constant inputs of TFF that is reversible are 2, 5 and 1 respectively. As the reversible gates cannot have fan out and feedback from output cannot be given to input of reversible gates, additional gates such as Feynman (FG) gates are used to overcome this problem. Table 1 compares the T Flip-Flop used in the design of reversible synchronous counter by different authors. Table 1 shows that the reversible T Flip-Flop constructed from FG and PG gates is a good candidate for building a counter circuit when compared with other T-Flip-Flop structures in terms of performance of parameters like garbage outputs, quantum cost, and constant inputs. T Flip-Flop constructed using SVS gate [14] uses only one reversible gate compared to the one used in the proposed design, where two gates are used. But, as the quantum cost of reversible SVS gate is not known, T Flip-Flop using PG and FG gates is used to design the reversible counter.

In the proposed reversible 4-bit synchronous counter, the state of T- (toggle) Flip-Flop toggles or changes continuously whenever the clock input is asserted and a ‘1’ is given as input to the Flip-Flop. Clock input from common source is given synchronously to all the Flip-Flops so that there is a change in the state of the Flip-Flops simultaneously. The 4-bit counter or mod-16 counter has 16 states and it generates a count sequence of ‘0000’ to ‘1111’ which repeats itself. The same design can be extended to n-bit synchronous counter which counts $2n$ states starting from 0 to $2n-1$. Adequate care has been taken during connections of the gates so that the delay is minimized. For the proposed 4-bit reversible counter,

reversible gates, constant inputs, garbage outputs and critical path delay are computed as 15, 12, 8, 33Δ . In general, for the proposed n bit counter, $(5n-5)$ reversible gates, $(4n-4)$ constant inputs, $(3n-4)$ garbage outputs are used. The critical path delay is calculated to be $(11(n-1)\Delta)$. The quantum cost of the reversible 4-bit synchronous counter is obtained from the quantum circuit drawn and is found to be 33. For an n -bit counter it is $11(n-1)$.

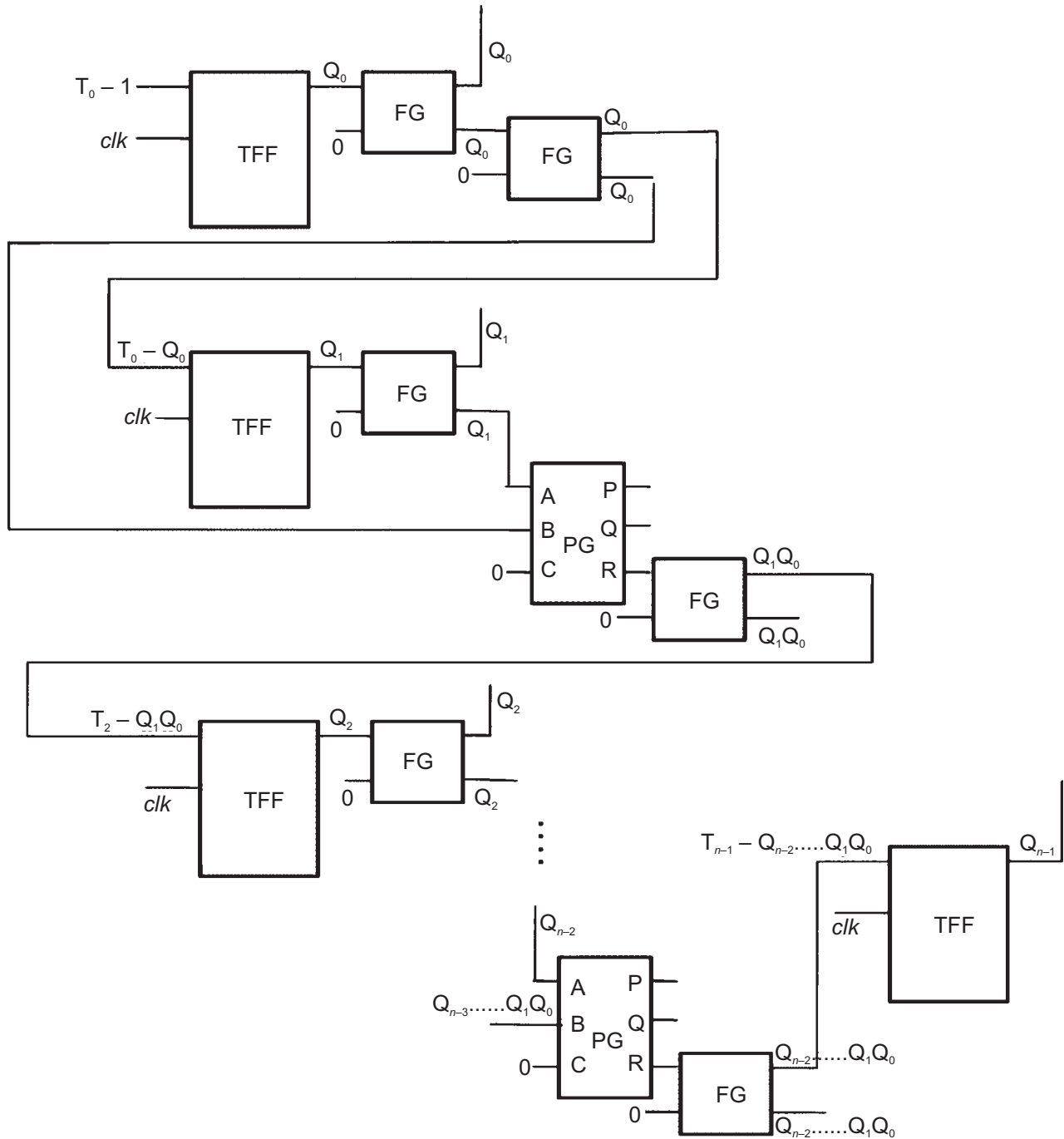


Figure 3: Reversible n bit Counter

4. SIMULATION RESULT AND ANALYSIS

For the purpose of evaluation of the performance of the proposed 4-bit reversible synchronous counter, simulation has been conducted using Verilog language on Xilinx version 7.1, and ModelSim version 6.1 software. Fig 8 displays the results obtained during simulation of the reversible four-bit counter. To have a better analysis of the performance of proposed 4-bit reversible synchronous counter, the results are

compared with designs of 4-bit reversible synchronous counters in [11], [12], [13], and [14]. The evaluation purpose the parameters taken for comparison are quantum cost, hardware complexity, reversible gates used, critical path delay, garbage outputs, and constant inputs for 4 bit reversible synchronous counter. This comparison has been given in Table 2. Adequate care has been taken during connections of the gates so that the delay is minimized.

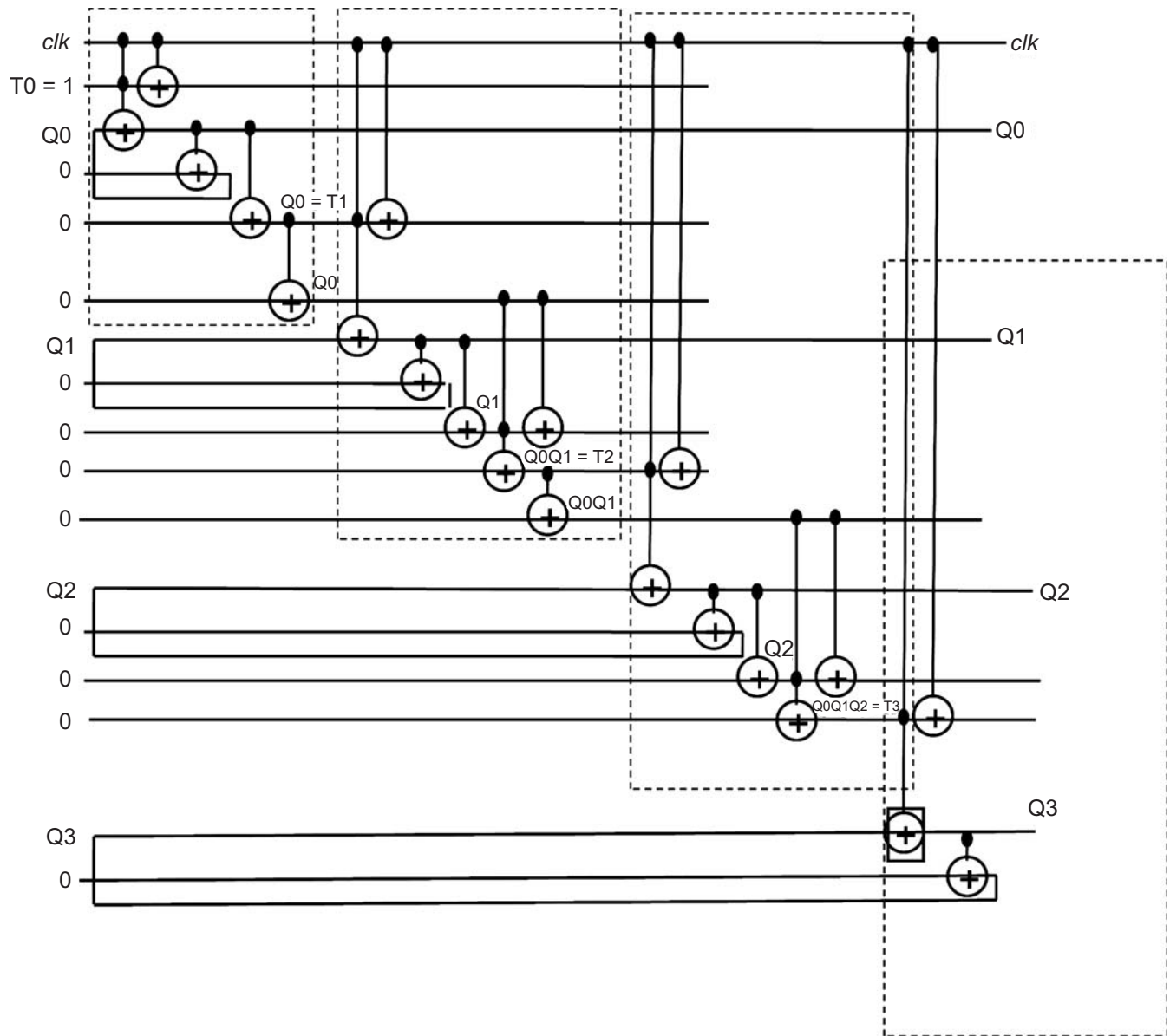


Figure 4: Quantum circuit of 4 bit reversible synchronous counter proposed

The design of reversible synchronous counter given in [11] uses MUX gate. Saymen (SG) gate is used to design the counter in [12] and [13]. Authors of [14] have proposed a new gate called SVS gate and designed the counter using SVS gate. But quantum cost of SVS gate is not computed.

The analysis of the counter designs with respect to the Table 2 is as follows.

- Hardware complexity is computed in terms of EXOR, AND and NOT operations performed in the design which need to be minimized. The hardware complexity of the proposed design is computed to be $21\text{XOR} + 6\text{AND}$ whereas the hardware complexity of the designs in [11], [12], [13] and [14] is given as $90\text{XOR} + 52\text{AND} + 42\text{NOT}$, $56\text{XOR} + 56\text{AND} + 14\text{NOT}$, $63\text{XOR} + 68\text{AND} + 17\text{NOT}$, and $29\text{XOR} + 26\text{AND} + 12\text{NOT}$ respectively. The hardware complexity of the proposed design has significantly reduced as compared to other counter circuits.

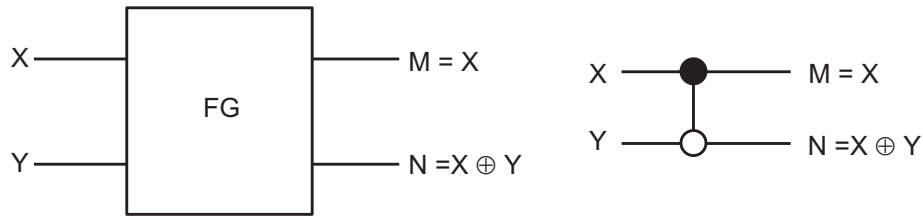


Figure 5: Feynman gate, and its Quantum circuit

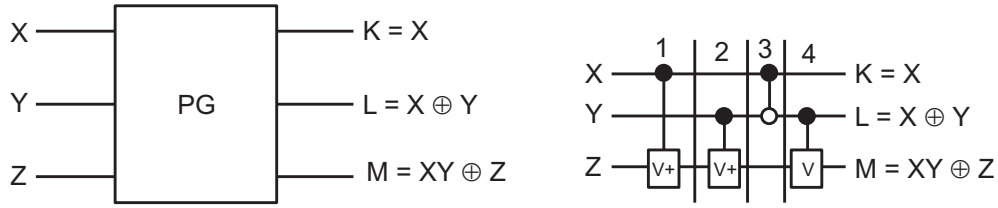


Figure 6: Peres gate, and its Quantum circuit

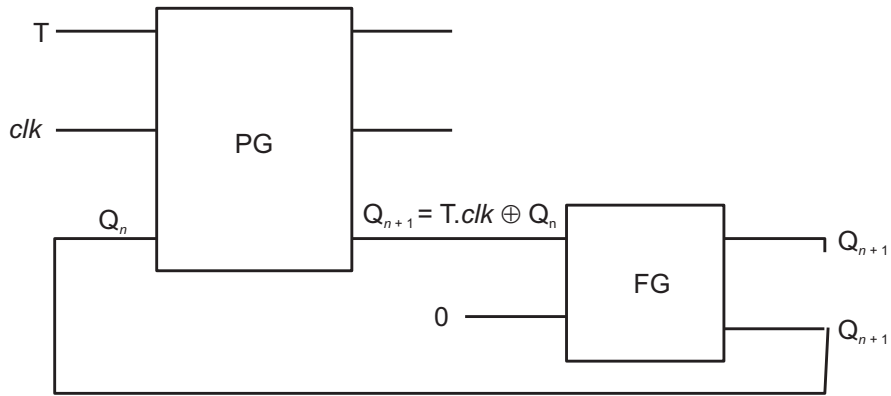


Figure 7: Reversible T Flip Flop used in proposed design

Table 1
Comparison of different parameters of reversible $t ffs$

	<i>Garbage outputs</i>	<i>Reversible Gates</i>	<i>Quantum cost</i>	<i>Constant Inputs</i>
TFF used in Proposed design	2	2	5	1
TFF using MUX gate [11]	14	10	34	10
TFF using Sayem (SG) gate[12]	3	3	13	2
TFF using Sayem (SG) gate [13]	3	3	13	2
TFF using SVS gate [14]	2	1	Not Available	1

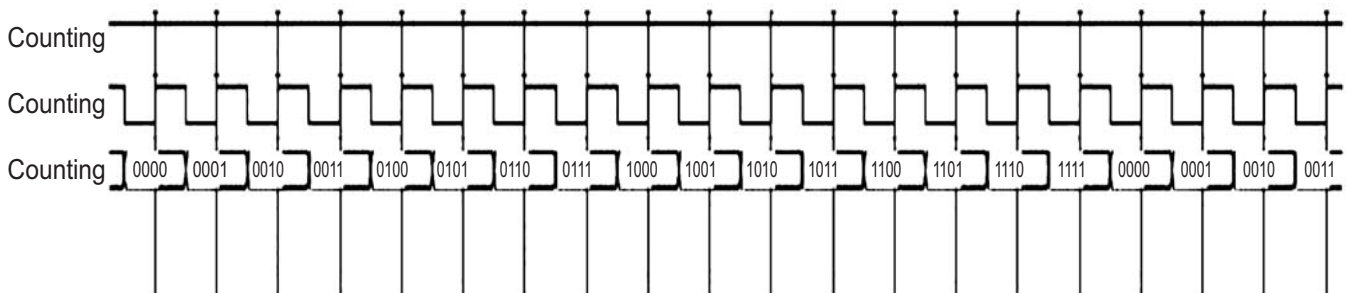


Figure 8: Simulation result of proposed 4-bit reversible synchronous counter

Table 2
Comparison of performance parameters of proposed n bit reversible synchronous counter with existing counters

		Quantum cost	Hardware Complexity	Reversible Gates	Critical Path Delay	Garbage outputs	Constant Inputs
Proposed n -bit Reversible Synchronous counter	Except for $n = 1$ bit	$11n - 11$	$7(n-1)XOR + 2(n-1)AND$	$5n - 5$	$11(n-1)\Delta$	$3n - 4$	$4n - 4$
	4-bit counter	33	$21XOR + 6AND$	15	33Δ	8	12
	3-bit counter	22	$14XOR + 4AND$	10	22Δ	5	8
	2-bit counter	11	$7XOR + 2AND$	5	11Δ	2	4
Reversible Synchronous counter using MUX gate [11]	3-bit counter	109	$66XOR + 38AND + 31NOT$	34	109Δ	39	34
	4-bit counter	148	$90XOR + 52AND + 42NOT$	46	148Δ	53	46
Reversible Synchronous counter using Sayem (SG) gate [12]	4-bit counter	99	$56XOR + 56AND + 14NOT$	22	99Δ	32	23
Reversible Synchronous counter using Sayem (SG) gate [13]	4-bit counter	106	$63XOR + 68AND + 17NOT$	28	106Δ	38	17
Reversible Synchronous counter using SVS gate [14]	4-bit counter		$29XOR + 26AND + 12NOT$	9	$(13 + 4 * QC(SVS)) \Delta$	10	9

- While constructing a reversible logic network, the usage of gates that are reversible need to be minimum for better performance. The design of the counter given in [11], [12], [14], and [13] uses 46, 22, 9 and 28 reversible gates respectively whereas the proposed 4 bit reversible synchronous counter uses 15 gates. Thus, it is seen that there is a reduction in this parameter in the proposed design. Even though the gates used in [14] is 9, the hardware complexity of the counter designed is very high compared to the proposed design and quantum cost is not known.
- The constant inputs present in the proposed design are 12 and that in [11], [12], [13] and [14] are 46, 23, 17 and 9 respectively.

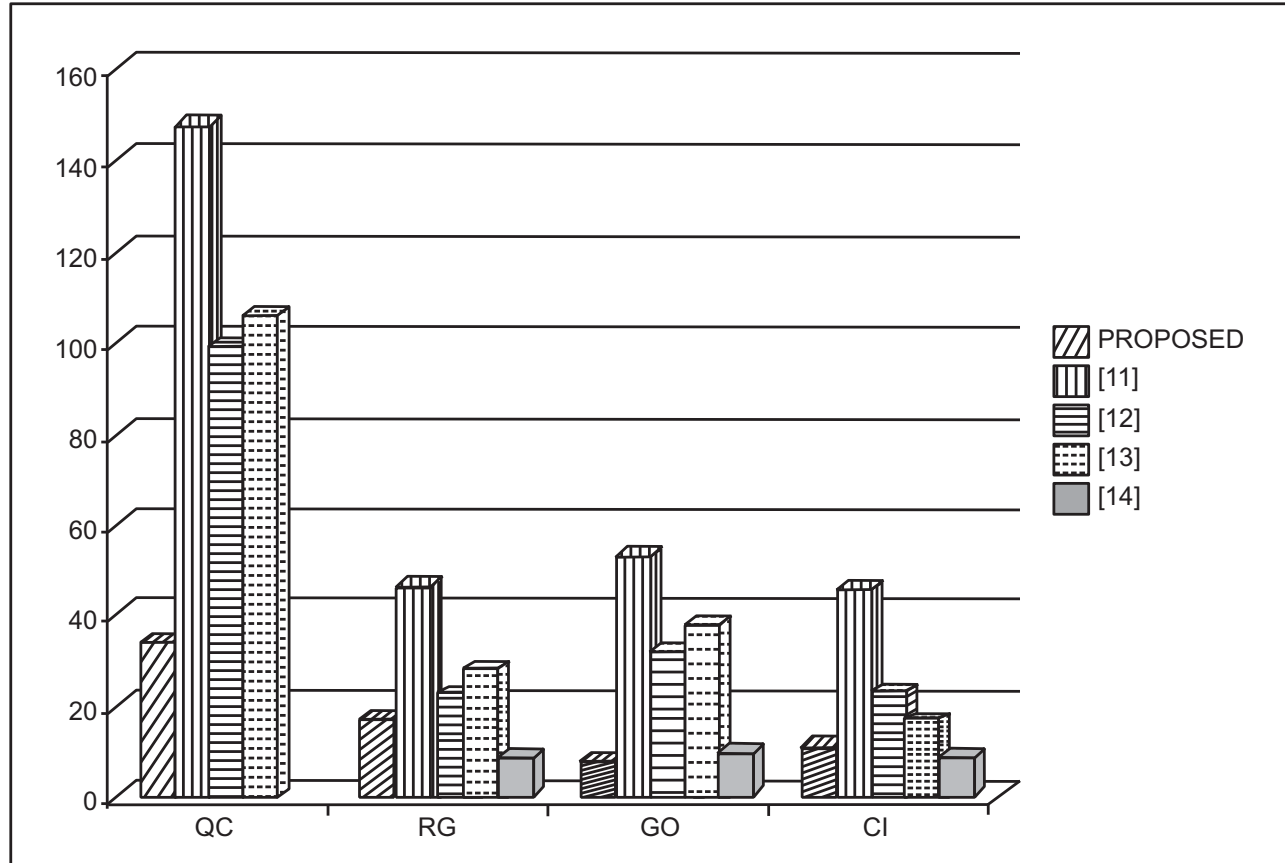


Figure 9: Improvement factor

- To increase the performance and minimize the complexity of the logic network, garbage outputs (unwanted or unused outputs) generated from the reversible circuit should be minimized. Garbage outputs generated in the proposed design is 8 and that in designs given in [11], [12], [13] and [14] are 53, 32, 38 & 10 respectively. Thus, in the proposed design, there is a drastic reduction in the garbage outputs produced.
- The quantum cost for the designs given in [11], [12], [13] and [14] are 148, 99, 106 and [13 + 4*QC(SVS)] respectively and that for proposed design, it is 33 which is very less compared to others. The authors of design in [12] and [14] have not computed the quantum cost. But, Quantum cost for the design in [12] is computed to be 99 as it is given that the quantum cost of reversible Sayem (SG) gate is 7 [13].
- The critical path delay is 33 Δ for the proposed design, where as it is 148 Δ , 99 Δ , 106 Δ and [13 + 4*QC(SVS)] Δ in case of designs in [11], [12], [13] and [14] respectively.

Thus, the values of quantum cost, hardware complexity, reversible gates used, critical path delay, garbage outputs, and constant inputs has been optimized for the proposed 4-bit reversible counter. Fig 9 shows the improvement factor by which the values of constant inputs (CI), quantum cost (QC), garbage outputs (GO), and reversible gates used (RG), have improved.

Thus, in addition to different power reduction techniques employed in CMOS circuits [15]-[17], as the complexity of CMOS circuits increases, the concept of reversible logic greatly reduces the power dissipation in digital circuits.

5. CONCLUSION

An n bit Synchronous reversible counter has been proposed where emphasis is on reducing the values of quantum cost, hardware complexity, reversible gates used, critical path delay, garbage outputs, and constant inputs, as compared to the already existing designs. The values of constant inputs, quantum cost, garbage outputs, and reversible gates used, are optimized in the proposed design and have improved by a factor of 3.83, 4.48, 6.63, and 3.07 respectively over the design in [11], 1.92, 3, 4, and 1.47 respectively over [12], 1.42, 3.21, 4.75, and 1.87 over the design in [13], and with respect to [14] by a factor of 0.42, NA, 1.3, and 0.6 (NA: not available). The proposed reversible counter can also be used to build reversible sequential circuits of higher order and complex design of quantum computers. Thus this design forms the basis for a reversible arithmetic circuit design and thus contributing to reduced or zero power dissipation.

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