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DESIGN AND IMPLEMENTATION OF BCD TO SEVEN SEGMENT DISPLAY DECODER USING REVERSIBLE DECODER ON FPGA

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Abstract: Reversible logic is the emerging field for research in present era. The aim of this paper is to design and synthesize a BCD to seven segment display decoder using a reversible decoder which is designed using reversible logic with minimum quantum cost. The designed BCD to seven segment display decoder is then implemented over FPGA SPARTAN – 3E. The seven segment display decoder finds its applications in digital calculators, clock radios, electronic meters etc., An n input and k output Boolean function is said to be logically reversible if and only if, the number of inputs are equal to the number of outputs i.e., 'n' equals 'k' and the input pattern uniquely maps the output pattern. The reversible logic must run both forward and backward as well such that the inputs can also be retrieved from outputs. If the device obeys above two conditions, it satisfies the second law of thermodynamics which preserves the information bits without getting erased and guarantees that no heat is dissipated. There are many reversible logic gates in literature like NOT gate, Feynman Gate, Double Feynman Gate, Peres Gate, TR gate, Seynman Gate and many more. Fan-out and Feed-back are not allowed in Logical Reversibility. To overcome the Fan out limitation, the signals from required output lines are duplicated to desired lines using additional reversible combinational circuits. Reversible Logic owns its applications in various fields which include Quantum Computing, Optical Computing, Nano-technology, Computer Graphics, low power VLSI etc., Reversible logic is gaining its own importance in recent years largely due to its property of low power consumption and low heat dissipation. In this paper the BCD to seven segment display decoder using reversible decoder which has less heat dissipation and low power consumption is proposed. The designed circuit is analyzed in terms of quantum cost, garbage outputs, number of gates etc., The Circuit has been designed and simulated using Xilinx software and implemented on FPGA SPARTAN – 3E.

Keywords: Quantum Cost, Reversible Gates, Garbage Outputs, Number of gates.

1. INTRODUCTION

In present VLSI Technology, Power Consumption and heat dissipation has become a very important factor for consideration. By using Reversible logic power consumption and heat dissipation can be minimized. There is no wonder even if heat dissipation becomes zero. Power consumption is very less in reversible logic circuits when compared to irreversible logic circuits. Reversible Logic finds its own application in Quantum computing, Nano-technology, Optical computing, Computer graphics and Low Power VLSI. An n input and k output Boolean function f ($a1$, $a2$, $a3$, …, an) (referred as (n, k)) is said to be logically reversible if and only if, the number of inputs are equal to the number of outputs i.e., 'n' equals 'k' and the input pattern uniquely maps the output pattern. Ralf Launduer [1] contributed his research on irreversible logical circuits. He told that heat dissipated in irreversible logical circuits is not because of the process involved in the operation of that circuit, but it is due to the information bits that were erased during the process of logical computing. He demonstrated Launder's principle which describes the lower theoretical limit of heat dissipation in logical computation. He introduced that losing of a single bit in the circuit causes the smallest amount of heat in the computation which is equal to KTln2 joules which is known as Launder's limit where K is Boltzmann constant (approximately 1.38×10^{-23} J/K), T is Temperature and ln 2 is natural algorithm of 2 (approximately 0.69315). The amount of heat

dissipated in simple circuits is very small but it becomes large in the complex circuits which imply propagation delay also. It is necessary to notice that there is a direct relationship between the number of information bits erased to the amount of heat dissipated in the circuit. He also told that energy dissipation can be made zero if the logical computation is done without any information bits loss. Later in 1973 C. H. Bennett [2] described that the heat dissipation due to the information bit loss can be overcome if each and every computation in circuit was carried out in reversible manner. Quantum networks are designed of quantum logic gates. As each gate perform a unitary operation, KTln2 Joules energy dissipation wouldn't occur if the computation is carried out in reversible manner. He argued that for zero heat dissipation, the computation must be done in reversible. But if reversible logic is utilized to do logical computation, the heat dissipation will be less than KTln2 for one information bit in contrast to Launder. Thus computation done in reversible manner doesn't require erasing of bits. The amount of heat dissipated in the system holds a direct relationship to the number of bits erased or lost during the computation. In this paper a BCD to seven segment display decoder using a reversible decoder with minimum quantum cost is proposed and this circuit was implemented on FPGA SPARTAN – 3E.

2. MOTIVATION

At present consumers demand is more focused on electronic devices which are smaller and smaller. Consumers are enthusiastic in acquiring devices with less heat dissipation and low power consumption. According to Moore's law the number of transistors that are integrated per square inch on an integrated circuit gets doubled every year. At present the VLSI technology has already reached Nanotechnology and researchers were predicting that the roadmap of Moore's law is going to end because the size of the transistor can't be reduced more without falling into leakage problems. The logical voltages can't be reduced further more than their current levels without compromising to efficiency and impacting power consumption. The reversible logic given an interesting solution that if the information bits are conserved by un-computing them rather than erasing them, there will be a possible way for improved performance. Logical reversible computing gives improved energy efficiency. Reversible computing gives improved portability of devices. The energy efficiency of logical reversibility affects the speed of the circuits. Although the hardware complexity increases by reversible computing, the need of power consumption cost and performance cost are dominating the logical hardware cost. Hence the need of logical reversible computing cannot be ignored.

3. CONCEPT

The Reversible Logic involves the use of Reversible Gates consists of the same number of inputs and outputs i.e., there should be one to one mapping between input vector lines and output vector lines. In reversible computation, the reversible gates are made to run both forward and backward directions. Hence Reversible logic conserves information bits. Certain limitations are to be considered while designing circuits based on reversible logic (i) Fan out is not permitted in reversible logic and (ii) Feedback is also not permitted in reversible logic. In Reversible logic using outputs we can obtain full knowledge of inputs making use of garbage outputs. To overcome the Fan-out limitation, by using additional reversible combinational circuits, the output lines are duplicated into required number of lines that are required to drive the inputs of consecutive device. Similarly for Feed-back limitation delay elements are used. Here Feed-back and Fan-out became the main reason for heat dissipation in reversible logic circuits. The reversible and irreversible EX-OR gate figures along with their truth tables are illustrated in figure1. Some cost metrics like Garbage outputs, Number of gates, Quantum cost, constant inputs are used to estimate the performance of reversible circuits. Garbage outputs are the extra outputs which help to make inputs and outputs equal in order to maintain reversibility. They are extra output lines that are kept alone without performing any logical computation. Hence garbage outputs possess no involvement in logical reversible computation. Number of gates count is not a good metric to evaluate the performance of

Logical reversibility since more number of primitive gates are taken together to form a new gate. In logical reversibility the number gates required to implement any reversible circuit will be more hence it is required to maintain it to precise number. Quantum Cost is the number of elementary or primitive gates needed to implement a reversible logic gate. It is nothing but the number of reversible gates (1×1 or 2×2) required to construct the circuit. The quantum cost plays an important role in logical reversibility. If the quantum cost is more, then the area of the circuit increases, thereby increasing the propagation delay. But quantum cost doesn't impact heat dissipation. Delay is one of the important cost metrics. A Reversible circuit design can be modelled as a sequence of discrete time slices and depth is summation of total time slices. In Digital Electronics the binary decoder is a combinational logic circuit that converts the binary integer value to the associated output pattern. Various proposals are given to design of combinational and sequential circuits in the undergoing research.

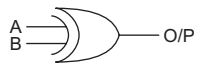

Figure 1: (a) Irreversible logic gate

Table 1
(a) Truth table for Figure 1(a)

A	*B*	*O/P*
0	0	0
0	1	1
1	0	1
1	1	0

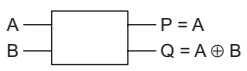

Figure 1: (b) Reversible logic gate

Table 1
(b) Truth table for Figure 1(b)

A	*B*	*P*	*Q*
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

In this paper, a BCD to seven segment display decoder using a reversible decoder is proposed with minimum Quantum cost. The designed BCD to seven segment display decoder is implemented on FPGA SPARTAN-3E.

4. REVERSIBLE LOGIC GATES

The reversible logic gate consists of same number of inputs and outputs as shown in the Figure 2. The basic Reversible Logic Gates present in the literature are briefed below. The gates that are suitable for the design with optimum quantum cost can be selected.

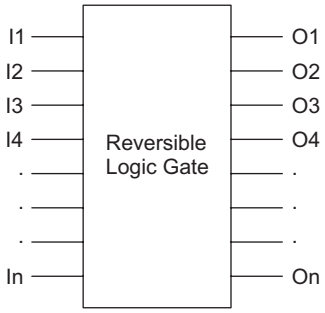

Figure 2: Simple reversible logic gate

1. NOT Gate

The NOT GATE is the simple Reversible Logic gate. It is 1×1 Reversible Logic Gate with the quantum cost zero. The Not gate simply shifts the complementary of the input to output as shown in the Figure 3. It is the basic primitive gate which may involve in construction of reversible logic gate, thus owing its own importance in determining the quantum cost of designed Reversible logic gate.

Figure 3: NOT Gate

Table 2
Truth table for NOT Gate

A	*B*
0	1
1	0

2. Feynman Gate (FG):

Feynman gate is a 2×2 reversible gate as shown in below Figure 4. The Feynman gate is also called as CNOT gate i.e., controlled NOT gate. The Feynman gate is used to duplicate of the required outputs since Fan-out is not allowed in reversible logic gates. The Quantum Cost of FG is 1. This is also the primitive

gate owing its importance in determining quantum cost metric.

Table 3
Truth table for Feynman Gate

A	*B*	*P*	*Q*
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Figure 4: Feynman Gate

3. Double Feynman Gate (DFG)

Double Feynman Gate is a 3×3 reversible gate. The outputs are defined as shown in the below figure5. The quantum cost of DFG is 2. This gate can also be used for duplicating outputs.

Table 4
Truth table for Double Feynman Gate

A	*B*	*C*	*P*	*Q*	*R*
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

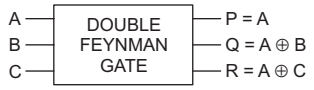

Figure 5: Double Feynman Gate

4. Toffoli Gate (TG)

Toffoli Gate is 3×3 reversible gate. The outputs P, Q, R are defined as shown in the below Figure 6. The Quantum Cost of TG is 4.

5. Fredkin Gate (FDG):

Fredkin Gate is a 3 × 3 reversible gate. The outputs are defined as shown in the below Figure 7. The Quantum Cost of FDG is 5. This paper mainly surrounds around Fredkin gate.

Table 5
Truth table for Toffoli Gate

A	*B*	*C*	*P*	*Q*	*R*
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

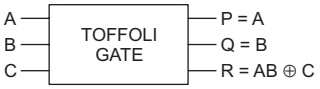

Figure 6: Toffoli Gate

Table 6
Truth table for Fredkin Gate

A	*B*	*C*	*P*	*Q*	*R*
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

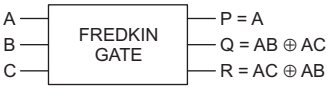

Figure 7: Fredkin Gate

6. Peres Gate (PG):

Peres Gate is a is a 3 × 3 reversible gate. The outputs are defined as shown in the below Figure 8. The Quantum Cost of PG is 4.

Table 7
Truth table for Peres Gate

A	*B*	*C*	*P*	*Q*	*R*
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

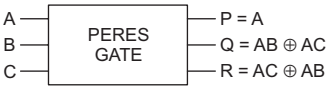

Figure 8: Fredkin Gate

7. TR GATE:

TR Gate is a 3 × 3 reversible gate. The outputs are defined as shown in the below Figure 9. The quantum cost of TRG gate is given by 4.

Table 8
Truth table for TR Gate

A	*B*	*C*	*P*	*Q*	*R*
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	0	1

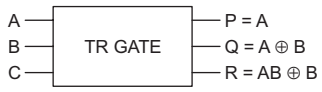

Figure 9: TR Gate

5. BASIC GATES USING REVERSIBLE GATES

Considering our circuit requirements we need to design AND gate and OR gate using reversible gates. Fredkin gate is used to design AND and OR gates as shown in figure10. Importance is given to fredkin gate because it gives optimistic performance at less Quantum Cost for designing AND and OR gates.

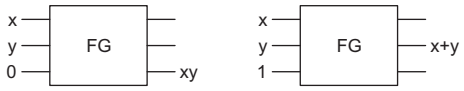

Figure 10: AND Gate using fredkin and OR Gate using fredkin

6. REALIZATION OF REVERSIBLE DECODER

In order to reduce the power dissipation in the decoder circuit, concept of reversible logic has been used. A 2 to 4 decoder has been designed using fredkin gates. Figure 11 shows the reversible 2 to 4 decoder. Every irreversible circuit has a heat dissipation problem. Heat dissipation of any irreversible circuit depends on number of information bits erased and the heat generates due to irreversibility is minimum of KTln2 Joules per bit loss.

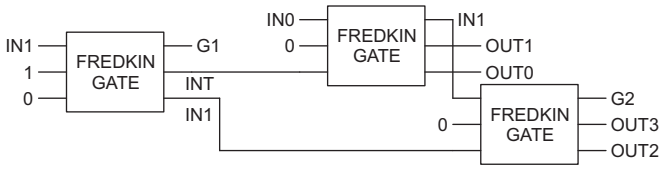

Figure 11: Reversible 2 to 4 decoder

Table 9
Truth table for Reversible 2 to 4 decoder

In1	*In2*	*Out3*	*Out2*	*Out1*	*Out0*
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

In Figure 11 IN1, IN0, E are three input signals and OUT0, OUT1, OUT2, OUT3 are four outputs. For the decoder to operate E signal should be at logic '1'. Three constant inputs i.e., logic 0 is provided to the circuit as shown in figure11 and G1, G2 are two garbage outputs. The total circuit works as a decoder, if it is realized making use of values as mentioned above and by Fredkin gate outputs P, Q, R expressions. Since in all the three Fredkin gates same number of inputs, power dissipation is less as compared to conventional logic gates. Hence by making use of Fredkin gates in similar manner any n to 2^n decoder can be designed. Here 'n' represents the number of inputs. The truth table for the reversible 2 to 4 decoder is as shown in the above Table 9.

7. EXISTING MODEL

The Design of Combinational and Sequential Circuits has been ongoing in research. Various proposals are given for the design of combinational circuits like adders, subtractors, multiplexers, decoders etc., in the existing method the author has given a novel design of 4 × 16 decoder whose Quantum Cost is less than the previous design. Replacing fredkin gates for designing 2 × 4 decoder reversible gates like peres gate, TR gate, NOT gate and CNOT gate are used as shown in Figure 12. The whole design is done using Fredkin, CNOT, Peres gates which give better Quantum Cost when compared to the other reversible Logic gates. The number of gates required to design 4 × 16 decoder are 18 in which there are 12 fredkin gates, one peres gate,

one TR gate, one NOT gate and 3 CNOT gates. The sum of all the quantum costs of each gate gives total quantum cost of 4x16 decoder.

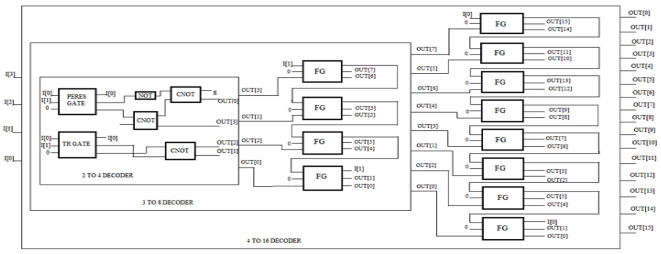

Figure 12: Circuit diagram of Reversible 4×16 decoder

8. IRREVERSIBLE SEVEN SEGMENT DISPLAY DECODER

A decoder is defined as a digital circuit which converts the binary integer value into associated output pattern. One of the most commonly used decoder in day to day life is BCD to seven segment display decoder. The BCD to seven segment display decoder consists of a seven segment display which is connected to a logical combinational circuit. The seven segment display is equipped with seven individual segments which can be either light emitting diodes (LEDs) or light crystal displays (LCDs). These segments are arranged in eight shaped pattern in the below Figure 13.

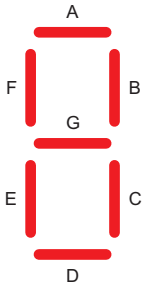

Figure 13: Seven Segment display

To make the display to work, these segments has to be driven with certain logic level. It must be either '0' or '1'. There are two types of seven segment displays. They are

1. Common cathode type segment display and
2. Common anode type segment display.

In a common cathode type seven segment display all the cathodes of the segments are tied together and grounded which is considered as logic 'o'. Logic '1' has to be driven to individual segment's anode to make the segment to glow.

In a common anode type seven segment display decoder, all the anodes are tied together and they are connected to VCC, which is considered as logic '1'. Hence to make the individual segment to glow the segment's cathode is to be driven with Logic '0'.

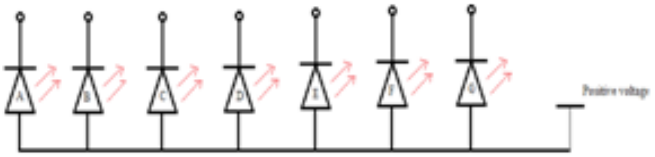

Figure 14: Common anode type connection of seven segment display

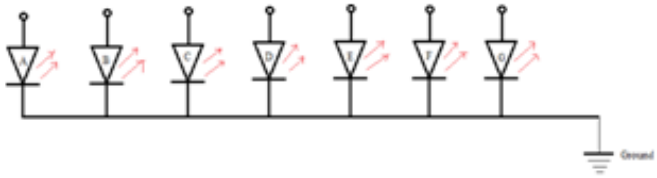

Figure 15: Common cathode type connection of seven segment display

The pin diagram *f* a seven segment display is drawn in the below Figure 16.

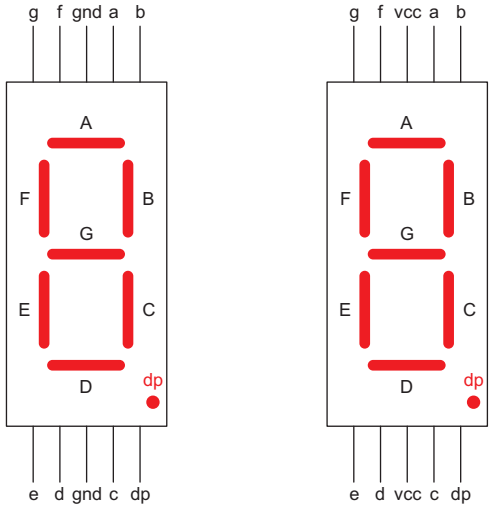

Figure 16: (a) Common cathode type (b) common anode type

The BCD to seven segment display decoder is a combinational circuit which converts the binary coded decimal value to suitable associated output pattern that drives seven segments which illuminates desired shape of a number or alphabet. The BCD to seven segment decoder consists of four input lines I[3], I[2], I[1], I[0] and seven output lines A, B, C, D, E, F, G. The block

diagram of BCD to seven segment decoder is shown in the below Figure 17.

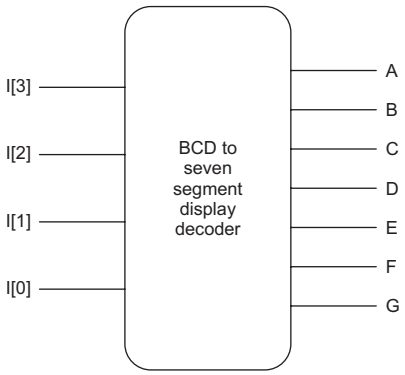

Figure 17: Simple block diagram of seven segment display decoder

Considering a common cathode type seven segment display decoder the truth table of BCD to seven segment display decoder is as shown below Table 10.

The below truth table indicates that the high input level is given to the anodes of segments of display which illuminates desired decimal value. If the common anode type segment display is considered then the ones in the truth table are replaced with the zeros which indicate that the low level input as to be driven to the cathode of segments in display to obtain desired decimal value.

Table. 10
Truth Table for seven segment display decoder

S	*BCD*	*G*	*F*	*E*	*D*	*C*	*B*	*A*
0	0000	0	1	1	1	1	1	1
1	0001	0	0	0	0	1	1	0
2	0010	1	0	1	1	0	1	1
3	0011	1	0	0	1	1	1	1
4	0100	1	1	0	0	1	1	0
5	0101	1	1	0	1	1	0	1
6	0110	1	1	1	1	1	0	1
7	0111	0	0	0	0	1	1	1
8	1000	1	1	1	1	1	1	1
9	1001	1	1	0	1	1	1	1

To understand the design of seven segment display decoder it is necessary to have complete knowledge of Boolean algebra rules. Consider the truth table in Table 10. The min term expressions for each and every output lines i.e., A, B, C, D, E, F, G can be written as

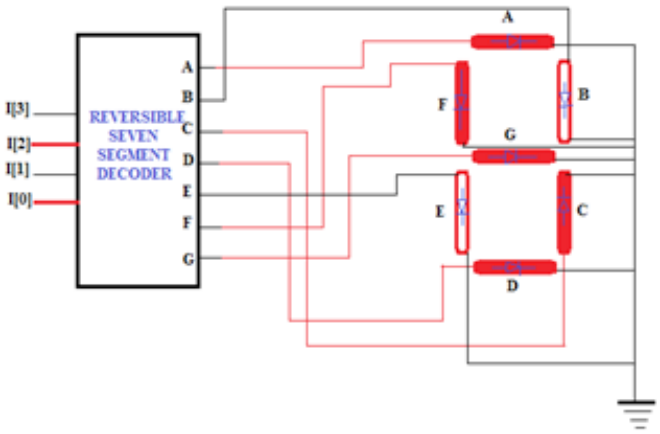

Figure 18: Seven segment display decoder displaying 5

$$A = F1\ (I[3], I[2], I[1], I[0])$$
$$= \Sigma m\ (0, 2, 3, 5, 7, 8, 9) \quad (1)$$
$$B = F2\ (I[3], I[2], I[1], I[0])$$
$$= \Sigma m\ (0, 1, 2, 3, 4, 7, 8, 9) \quad (2)$$
$$C = F3\ (I[3], I[2], I[1], I[0])$$
$$= \Sigma m\ (0, 1, 3, 4, 5, 6, 7, 8, 9) \quad (3)$$
$$D = F4\ (I[3], I[2], I[1], I[0])$$
$$= \Sigma m\ (0, 2, 3, 5, 6, 8) \quad (4)$$
$$E = F5\ (I[3], I[2], I[1], I[0])$$
$$= \Sigma m\ (0, 2, 6, 8) \quad (5)$$
$$F = F6\ (I[3], I[2], I[1], I[0])$$
$$= \Sigma m\ (0, 4, 5, 6, 8, 9) \quad (6)$$
$$G = F7\ (I[3], I[2], I[1], I[0])$$
$$= \Sigma m\ (2, 3, 4, 5, 6, 8, 9) \quad (7)$$

Consider 10 to 15 minterms as don't cares. The minterm expression for every output line is simplified using karnough's map to retrieve a logic combination of inputs for every output line. By using those simplified expressions the combinational circuit using basic gates can be constructed. There is another way to construct the BCD to seven segment decoder i.e., by using 4 to 16 decoder. The outputs of 4 to 16 decoder are treated as minterms. By using the output lines of 4 to 16 decoder the circuit is constructed based upon the minterm expressions listed above. But this is not highly recommended because it becomes complex. But

this type of procedure is to be followed to design the BCD to seven segment display decoder using reversible logic because if the reversible circuit is designed based upon the simplified boolean expressions by using basic gates made of reversible logic gates the quantum cost increases.

9. PROPOSED METHOD

Different Reversible Decoder circuits like 2 × 4, 3 × 8, 4 × 16 are designed using Fredkin Gates (mainly), Feynman gates and Peres gate. A design of BCD to seven segment display decoder using 4 to 16 reversible decoder and reversible OR gates is proposed. Here the reversible decoder is used to implement BCD to seven segment decoder instead of using the basic gates made of reversible logic gates because the quantum cost increases. Hence the 4 to 16 reversible decoder is preferred to design a BCD to seven segment decoder using reversible logic. The concept of duplicating a single output to required number of outputs using Feynman gate is introduced where Fan-out was not allowed in reversible computation.

Duplicating Outputs

The concept of duplicating one output to two outputs using Feynman gate is introduced. The second input of Feynman gate was made to 0 which drives two splitted equivalent outputs. Feynman gate is selected for duplicating of inputs because its quantum cost is less. It is also known as CNOT gate whose quantum cost is 1. The number of duplicating outputs can be increased by increasing the number of CNOT gates as shown in the below Figure 19.

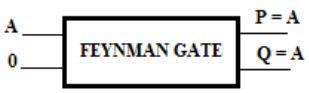

Figure 19: (a) Split circuit with 2 duplicating outputs

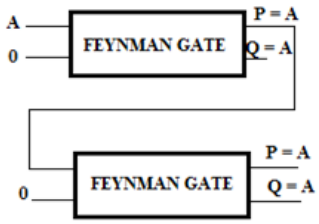

Figure 19: (b) Split circuit with 3 duplicating outputs

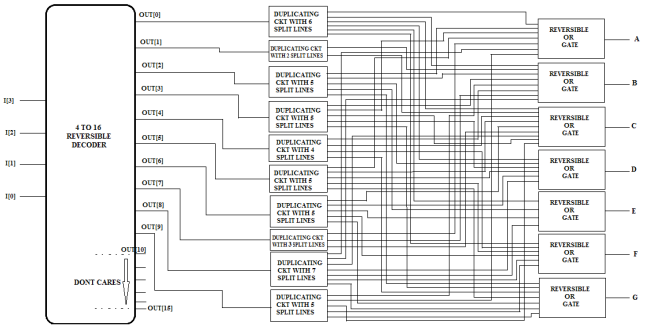

Figure 20: Circuit diagram of BCD to Seven segment decoder using reversible decoder.

The circuit diagram of BCD to seven segment display decoder using reversible decoder is as shown in the below Figure 20. In the above min term expressions i.e., Eq1, Eq2, Eq3, Eq4, Eq5, Eq6, Eq7 the min term out [0] drives signal to 6 ports to retrieve inputs A, B, C, D, E, F. Since in reversible logic Fan-out is not allowed a reversible duplicating combinational circuit capable of splitting or duplicating six signals is to be introduced. Hence split circuits are introduced in the circuit diagram. Those split circuits are made of Feynman gate and Double Feynman gate. Similarly to the remaining min terms also the duplicating is done to retrieve outputs wherever necessary. The simulated outputs and the results of circuit implementation over the FPGA SPARTAN-3E are shown in chapter X.

10. SIMULATION RESULTS

1. 4×16 Reversible Decoder

It is clear from the above simulated output in Figure 22 resembling stair case that different binary integer value is converted to associated pattern of outputs.

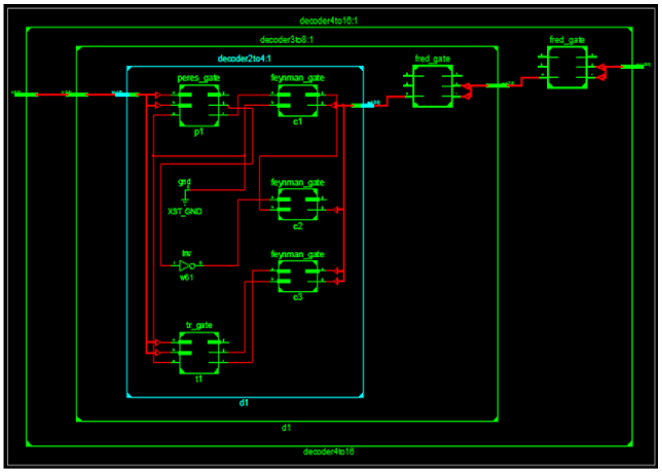

Figure 21: RTL Schematic of 4×16 reversible decoder

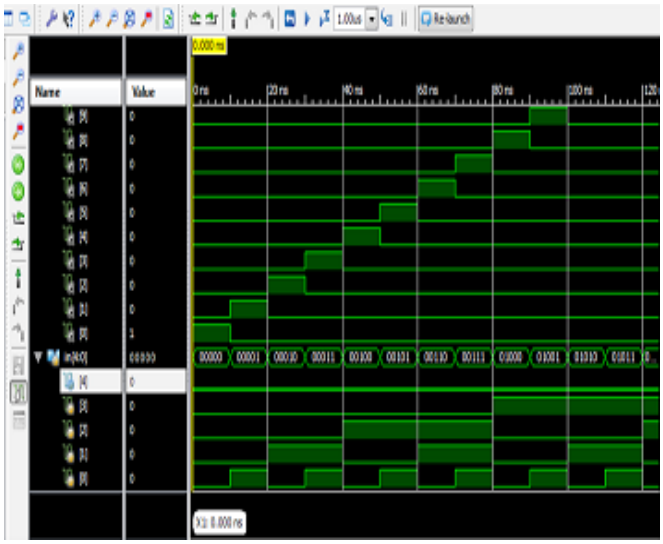

Figure 22: Simulated output for Reversible 4 ×16 decoder

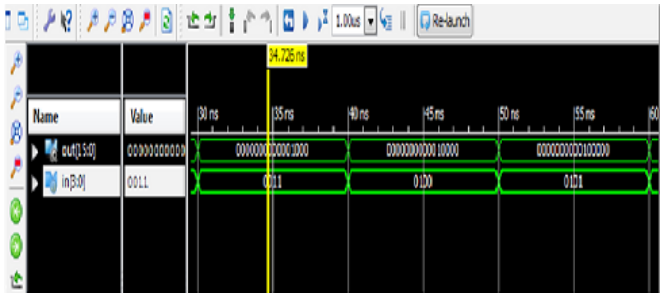

Figure 23: Simulated output for Reversible 4 ×16 decoder in vector form

11. BCD TO SEVEN SEGMENT DECODER USING REVERSIBLE DECODER

The number for the selected input BCD value is displayed over the seven segment display. For example for the binary BCD input value '0111' the output that appears over seven segment display is 7. Practically eighty percent efficiency can be obtained in terms of heat dissipation by using this reversible seven segment display decoder. Hence this BCD to reversible seven segment display decoder is considered when compared to conventional BCD to seven segment display decoder. The simulated output is shown in Figure 25.

12. COMPARITIVE STUDY

The reversible decoder, Reversible gates designed and used in this paper are analyzed in terms of Quantum cost and Garbage outputs (G.O). The Quantum Cost (Q.C) of total circuit is the sum quantum costs of each

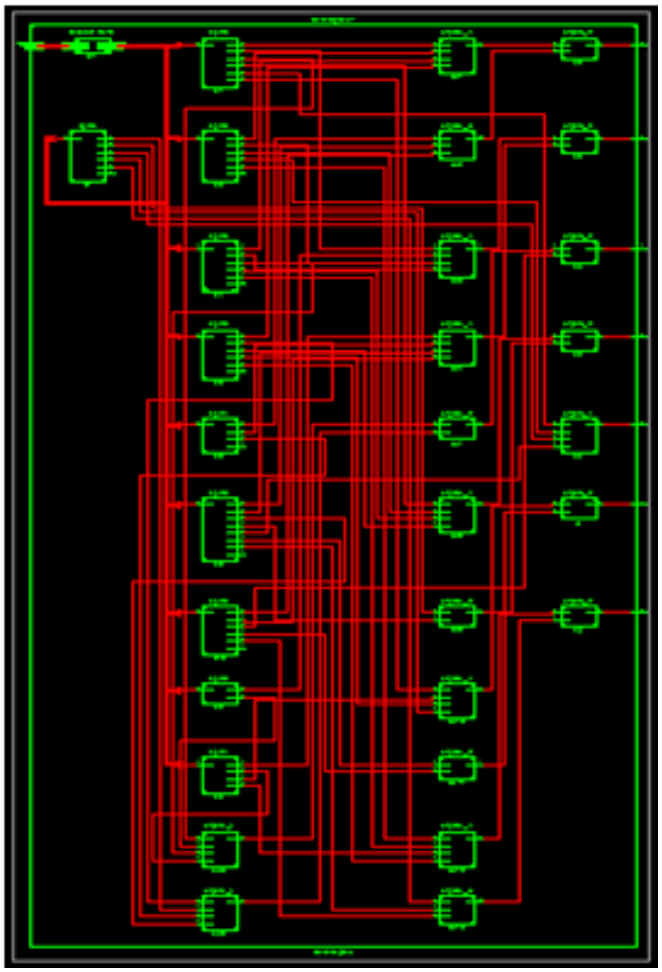

Figure 24: RTL Schematic of BCD to seven segment decoder using reversible decoder

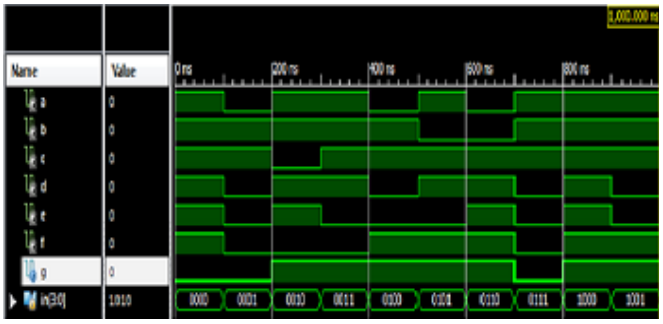

Figure 25: Simulated output of BCD to seven segment decoder using reversible logic

reversible circuit or gate used in designing the whole circuit. The Quantum cost is the important parameter in reversible logical computation because Quantum Cost has a serious relation with propagation delay. If Quantum Cost increases the propagation delay also increases. The minimum the quantum cost the minimum the propagation delay.

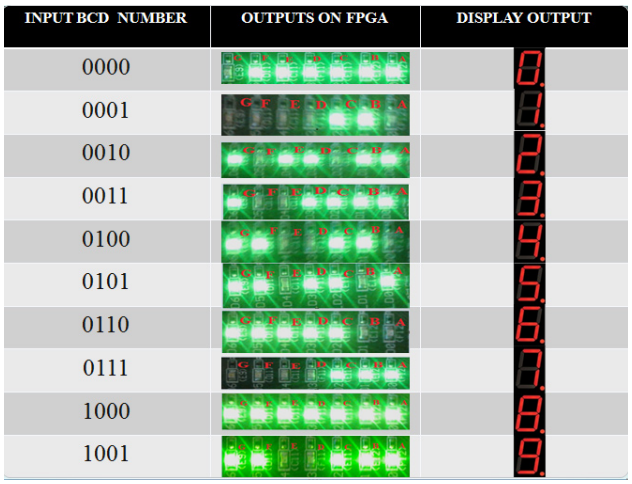

Figure 26: FPGA output of BCD to reversible seven segment display decoder

Source Pad	Destination Pad	Delay
in<0>	a	7.944
in<0>	b	8.023
in<0>	c	7.927
in<0>	d	7.808
in<0>	e	8.228
in<0>	f	7.687
in<0>	g	8.683
in<1>	a	9.209
in<1>	b	9.259
in<1>	c	9.125
in<1>	d	9.073
in<1>	e	8.152
in<1>	f	8.912
in<1>	g	9.919
in<2>	a	8.466
in<2>	b	8.511
in<2>	c	8.510
in<2>	d	8.330
in<2>	e	7.541
in<2>	f	8.320
in<2>	g	9.171
in<3>	a	8.374
in<3>	b	8.475
in<3>	c	8.522
in<3>	d	8.238
in<3>	e	8.610
in<3>	f	8.276
in<3>	g	9.135

Figure 27: Propagation Delay to each output line in Reversible seven segment display decoder circuit

Table 11
Analysis Reversible circuits used in the design

Circuit	*Quantum Cost*	*Garbage Outputs*
Reversible 2 to 4 decoder	11	3
Reversible 3 to 8 decoder	31	4
Reversible 4 to 16 decoder	71	5
Reversible And Gate	5	2
Reversible OR Gate	5	2

Source Pad	Destination Pad	Delay
i<0>	a	7.485
i<0>	b	7.505
i<0>	c	7.828
i<0>	d	7.970
i<0>	e	7.749
i<0>	f	8.293
i<0>	g	8.528
i<1>	a	7.877
i<1>	b	8.161
i<1>	c	8.434
i<1>	d	8.312
i<1>	e	8.236
i<1>	f	8.746
i<1>	g	8.920
i<2>	a	6.989
i<2>	b	7.009
i<2>	c	7.276
i<2>	d	7.418
i<2>	e	7.205
i<2>	f	7.693
i<2>	g	8.032
i<3>	a	7.881
i<3>	d	8.343
i<3>	f	8.817

Figure 28: Propagation Delay to each output line in Irreversible seven segment display decoder circuit

13. CONCLUSION

In this paper, a BCD to seven segment display decoder constructed using reversible decoder is designed. This circuit is designed for minimum quantum cost and minimum garbage outputs. The method proposed for designing the decoder circuit can be generalized. For example, a 3×8 decoder can be designed using a 2×4 decoder followed by 4 fredkin gates, Similarly a 4×16 decoder can be designed using 3×8 decoder followed by 8 fredkin gates. The concept of duplicating the single output to required number of outputs is utilized to overcome the fan-out limitation in reversible logic circuits. This method of designing combinational circuits helps to implement many digital circuits with better performance for minimum quantum cost.

The propagation delay to every segment from input is around 5.99ns. When compared to conventional

irreversible circuit the propagation delay increases slightly which can be termed as a demerit in this circuit. Hence this circuit can be designed further more with less quantum cost. If quantum cost increases the propagation delay increases. Finally eighty percentage of efficiency is observed with respect to heat dissipation when compared to conventional irreversible circuit.

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