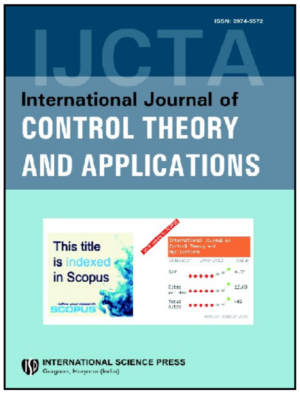

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Voltage Unbalance and Harmonic Compensation for Islanded Droop Controlled Microgrid Inverters

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Abstract: *Objectives:* This study proposes a droop controlled voltage unbalance reimbursement technique in an islanded microgrid. *Methods/Analysis:* The control system is executed in áâ static reference frame work. Here the distributed generators (DGs) inverters are managed appropriately to compensate imbalance in allocating active as well as reactive powers. The control system includes active as well as reactive power droop controllers, virtual impedance loop, voltage as well as current controllers. An unbalance compensator is provided for restoring the voltage amplitude as well as frequency at output of the DG inverter. *Findings:* Voltage unbalance factor, which is considered as the index of voltage unbalance is reduced from >3% to <1.5%. THD of output voltage is reduced to 5.51% from 19.77%. *Improvement:* The obtained results show that voltage unbalance is well compensated by utilizing this control technique. Harmonics in microgrid are reduced by compensation of selective main harmonics by resonant controllers.

Keywords: Microgrid, Distributed Generators (DGs), Voltage Unbalance Compensation.

1. INTRODUCTION

Impacts of energy conservation with environment over the raise in price are rapid moving the focal point to the renewable use as well as prolong energy sources. In this regard, the microgrid approach has unlocked the scope of incorporating renewable energy resources in conservative grid, Devoid of direct coupling with conservative grid parts. A grid with distributed generators (DGs), energy storage system as well as dispersed load to function in a mode of grid attached or islanded is the microgrid [1]. Distributed generators are frequently attached to the value grid or microgrid by a power-electronic interface converter. The major objective of the DG inverter is to regulate output voltage phase angle as well as amplitude to organize the active as well as reactive power inoculation, despite the fact that reimbursement of power value issue attained by means of appropriate control approach. Between varieties of power quality occurrences, voltage imbalances are extremely frequent. Voltage imbalance has unfavorable impacts on the tools as well as power system, result in adverse effects on the equipment as well as power system. In imbalanced circumstances, the power system will acquire further failures as well as less constant. In addition, voltage imbalance has unenthusiastic affects on equipment like induction motors, power electronic converters as well as adjustable speed drives (ASDs). Hence, the international Electrotechnical Commission (IEC) suggested the 2% voltage imbalance limit in electrical systems [2]. Currently some concepts of control are intended to manage the DG interface converter aims to recompense power value issues. This concept is in [3] based on managing all DG microgrid units as an unenthusiastic series conductance to recompense voltage imbalance. The conductance allusion is decided by means of employing a sag attribute to be used as an Unenthusiastic series reactive power in providing the recompense sharing attempt. Voltage imbalance recompensation can be done by means of sequence active power filter with negative series voltage on distribution line [4-6].

The control scheme is in [7] based on two-inverter interface converter with shunt attached in one end as well as grid attached in another with series to manage power stream in order to recompense the voltage imbalance. The two inverter configuration can be unappeased of considering DG interface converter with the charge as well as quantity. A hierarchical control concept for voltage imbalance recompense in an islanded microgrid is suggested in [8]. The control configuration contains local controllers as well as a central controller for compensation of imbalance to the aspiration value.

A load balancing reimbursement approach as well as restraining local currents for the power electronic hybrid system (PEHS)on the voltage vector transformation scheme is recommended in [9]. Harmonic compensation scheme [10, 11, 12] is on creating the DG units for power distribution organization in which resistance is incorporated at harmonic frequencies. Furthermore, a technique for compensating voltage harmonics in an islanded microgrid is in [13]. This technique is also on the basis of resistance enclosure as well as applied a harmonic power sag attribute to distribute the recompense effort between DGs. This paper most importantly focuses at the DGs inverters output on the voltage value. The DG power stage as well as control structure are given in figure 1. As exposed, the power stage of DG unit contains DC voltage source, an interface inverter as well as an LC filter. The control configuration mostly has:

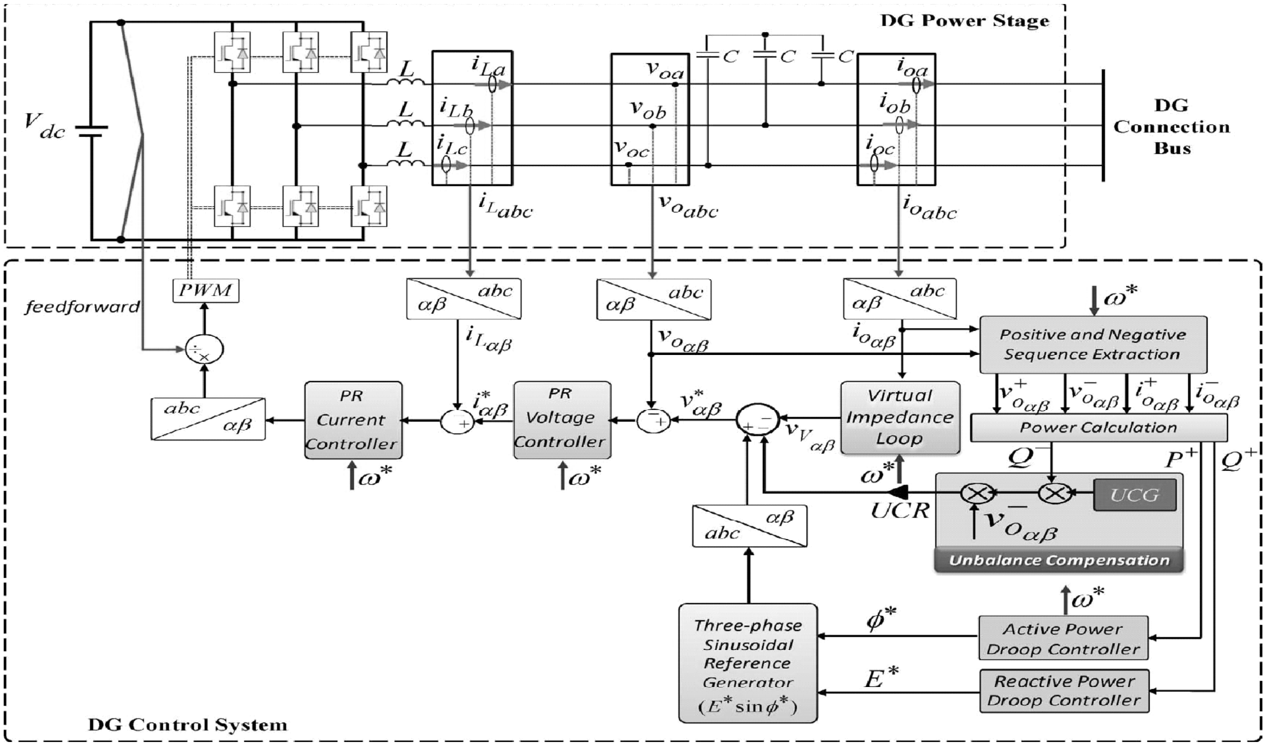

Figure 1: DG power stage and control system

- Active as well as reactive power droop controllers
- Virtual impedance loop
- Proportional as well as resonant controllers
- Voltage unbalance compensator

Here, voltage imbalance reimbursement is obtained through change in the DG inverter voltage reference value [14]. Harmonic distortion compensation caused by imbalanced load is also considered here. Changes in reference value have been feed to the voltage controller as input in order to control the interface inverter output voltage.

2. DG CONTROL SYSTEM

In αβ reference frame the DG control system is planned. So that Clarke transformation has been used to alter the abc as well as αβ frame variables. In αβ frame DG output reference voltage ($V^*_{\alpha\beta}$) is offered through power droop controllers, virtual impedance loop as well as imbalance compensation block. In accordance with $V^*_{\alpha\beta}$ as well as the $V_{0\alpha\beta}$, instantaneous measured value, the reference current $i^*_{\alpha\beta}$ is created. After that, LC filter inductor current is computed ($i_{L\alpha\beta}$) as well as regulated by means of current controller in providing voltage reference for pulse width modulator (PWM) to produce gate pulses in DG inverter. A feed forward loop has been comprised to concern the dc source voltage (V_{dc}) variation within the permitted limits.

(A) Active as well as Reactive power control

A three phase DG attached to the grid by means of impedance is considered, the fundamental positive sequence (FPS) active as well as reactive powers infused into the grid as:

$$P^+ = 3\left(\frac{EVCos\emptyset}{Z} - \frac{V^2}{Z}\right) Cos\theta + 3.\frac{EV}{Z} Sin\emptyset\, Sin\theta \tag{1}$$

$$Q^+ = 3\left(\frac{EVCos\emptyset}{Z} - \frac{V^2}{Z}\right) Sin\theta - 3.\frac{EV}{Z} Sin\emptyset\, Cos\theta \tag{2}$$

Where E denotes phase rms value of the DG inverter FPS output voltage, V indicates the grid phase rms voltage, φ represents the load angle (the angle between E as well as V), Z as well as θ represents the magnitude as well as the phase of the impedance, correspondingly. For grid voltage a zero phase angle is assumed, φ is equal to the phase angle of the inverter voltage. Considering inductive electrical system ($Z \approx X$ and $\theta \approx 90$), as well as small value of φ, equations (1) and (2) will be:

$$P^+ \approx 3.\frac{EV}{X}\phi \tag{3}$$

$$Q^+ \approx 3.\frac{V(E-V)}{X} \tag{4}$$

Hence, the FPS active as well as reactive powers can regulate the phase angle as well as amplitude of the DG unit FPS output voltage, in that order. In accordance with this circumstance, the power droop controllers establish the DGs output voltage amplitude and phase angle (E* and ö*, correspondingly) reference values in an islanded microgrid:

$$\emptyset^* = \emptyset_0 - \left(m_p P^+ + m_I \int P^+ dt\right) \tag{5}$$

$$E^* = E_0 - n_P Q^+ \tag{6}$$

Where,

E_0 rated voltage amplitude;

Φ_0 rated phase angle;

m_p FPS active power proportional coefficient;

m_I FPS active power integral coefficient;

n_p FPS reactive power proportional coefficient;

E* FPS Voltage amplitude reference;

Φ * FPS Voltage phase angle reference;

(B) Power calculation

Instantaneous values of active as well as reactive power can be calculated based on the instantaneous reactive power theory as follows:

$$p = v_{o\alpha} i_{o\alpha} + v_{o\beta} i_{o\beta} \tag{7}$$

$$q = v_{o\alpha} i_{o\beta} - v_{o\beta} i_{o\alpha} \tag{8}$$

The instant power values contain dc as well as ac components. The dc components are FPS active and reactive powers and ac (oscillatory) parts are produced by imbalance harmonics at case of voltage and current. FPS active and reactive powers are computed through pertaining conventional power equations with particular voltage and current.

Thus equations (7) and (8) are modified to estimate instantaneous FPS active as well as reactive powers and fundamental negative sequence (FNS) reactive power respectively:

$$P'^{+} = v_{0_\alpha}^{+} i_{0_\alpha}^{+} + v_{0_\beta}^{+} i_{0_\beta}^{+} \tag{9}$$

$$Q'^{+} = v_{0_\alpha}^{+} i_{0_\beta}^{+} - v_{0_\beta}^{+} i_{0_\alpha}^{+} \tag{10}$$

$$Q'^{-} = v_{0_\alpha}^{-} i_{0_\beta}^{-} - v_{0_\beta}^{-} i_{0_\alpha}^{-} \tag{11}$$

Where the superscripts "+" and "–" denotes positive as well as negative sequence components, correspondingly.

(C) Virtual impedance loop

Virtual impedance block diagram is depicted in figure2. Virtual impedance addition creates the oscillations, such that the system is further damped. P^+ and Q^+ decoupling can be attained through the virtual impedance which is much more inductive and it generates the constant droop controller operation.

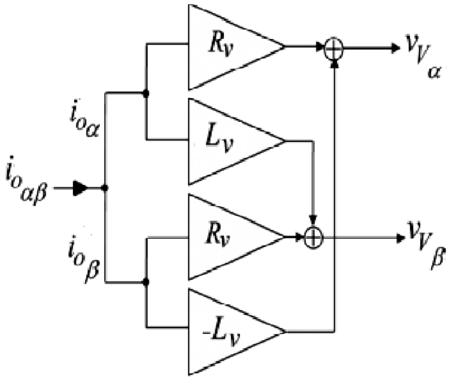

Figure 2: Virtual output impedance

As in figure1, the instantaneous current output is given into the virtual impedance control loop followed by reference voltage with the output loop and virtual impedance is executed as given in figure2, where in the virtual resistance and inductance values are RvandLv correspondingly. Hence the virtual impedance in the áâ frame expressed in the subsequent equation:

$$v_{V\alpha}=R_v.i_{0\alpha}-L_v.i_{0\beta} \tag{12}$$

$$v_{V\beta}=R_v.i_{0\beta}+L_v.i_{0\alpha} \tag{13}$$

(D) Proportional and resonant controllers

Because of the challenges in proportional-integral (PI) controllers for tracking non-dc parameters, proportional-resonant (PR) controllers are typically desired to regulate the voltage and current in the static reference frame.

$$G_V(s) = k_{pv} + \frac{k_{rV}.s}{s^2+(\omega^*)}{}^2 \tag{14}$$

$$G_I(s) = k_{pI} + \frac{k_{rI}.s}{s^2+(\omega^*)}{}^2 \tag{15}$$

Equations (9) and (10) indicate the PR voltage and current controllers correspondingly. Where in kpV (kpI) andkrV (krI) are the proportional as well as resonant coefficients of the voltage (current) controller, correspondingly. The direct filter inductor current is regulated by the current controller to control this instant of the DG output current, the load current perused is appropriately rejected on the performance of the control system.

Because on extremely narrow band, the PR controller acts on it about its resonant frequency ω, for a lower order harmonics, a harmonic compensator can be executed devoid of any unfavorable behavior controller effects. The harmonic compensator contains structure by means of cascading some common integrators tuned in to reverberate at the required frequency ω. The PR controller transfer function with harmonic compensator is expressed as:

$$G_V(s) = k_{pv} + \sum_{h=1,2,3,4,5} \frac{k_{rVh}.s}{s^2+(h\omega^*)}{}^2 \tag{16}$$

$$G_I(s) = k_{pI} + \sum_{h=1,2,3,4,5} \frac{k_{rIh}.s}{s^2+(h\omega^*)}{}^2 \tag{17}$$

Where h signifies the harmonic order.

(E) Voltage unbalance compensation

Voltage unbalance causes the negative appearance of voltage their reduction will recompense the imbalance. As in Figure1, the Unbalance Compensation output block [Unbalance Compensation Reference (*UCR*)] is infused for the voltage controller as a reference. This reimbursement reference is to create the FNS reactive power (Q^-) which is multiplied through constant [Unbalance Compensation Gain (*UCG*)] as well as by the instantaneous FNS voltage ($v^-_{o\alpha\beta}$). UCG is a constant to regulate the effort compensation on DGs and chosen so that the imbalance voltage is compensated with a satisfactory level devoid of making the control system unbalance. Here 1.5 is selected in UCG and with the increase of UCG, compensation effort will also increase. Conversely, to preserve the stable control system UCG has been preferred.

For voltage imbalance compensation as the negative sequence voltage decrease, Q^- decreases. Therefore, to create reference for compensation, Q^- has been considered leads to the appropriate compensation sharing between the micro grids DGs. Hence, DGs can separately recompense for voltage imbalance, so that communication link is not necessary between them. Additionally, multiplying with $v^{-}_{o\alpha\beta}$ guarantees the compensation reference will perform in to negative sequence voltage opposite phase with negative sign for the reference inoculation in Figure 1.

3. RESULTS

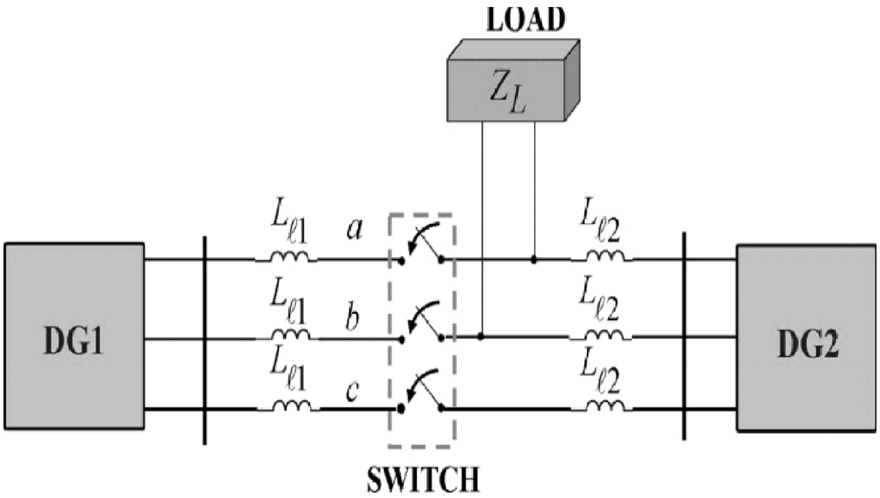

Figure 3: Test system for simulation evaluation

Simulation consequence of voltage unbalance recompense is offered to consider a resistive load. The islanded microgrid given in figure3 is regarded as the test system to evaluate with the simulation for voltage unbalance compensation. This microgrid consist two DGs in the company of the power stage as well as control system, as in Figure1. A single-phase load is attached among phase-*a* and phase-*b* for creating voltage imbalance. The switch in Figure3 is clogged following harmonization in forming a microgrid. The three-phase inductors between every DG and load connection point (*Ll*1 as well as *Ll*2 for DG1 as well as DG2, correspondingly) model the distribution lines and are asymmetrical, *Ll*1=2·*Ll*2.

Table 1
Electrical System Variablees

DC source Voltage	*LC filter Inductance*	*LC filter capacitance*	*Distribution line impedance*	*Linear Load*
Vdc(V)	L(mH)	C(μF)	L*l*1/L*l*2(mH)	ZL(Ω)
650	1.8	25	3.6/1.8	73

Table 2
Control System Variablees

	Power controllers				*Virtual impedance*	
mp	*mI*	*np*	*E0 (V)*	*ω0 (rad/sec)*	*Rv (Ω)*	*Lv (mH)*
0.00002	0.0002	0.13	330	314.1	1	4

Unbalance				
Voltage controller		*Current controller*		*compensator*
K*pv*	K*rv*/K*rv2*/K*rv4*	K*pI*	K*rI*/K*rI2*/K*rI4*	UCG
0.35	25 / 10 / 2	0.7	500 / 30 / 4	1.5

In Tables 1 and 2 the variables of the microgrid power stage as well as control system are programmed, respectively. The parameters L, C and V_{dc} are similar in both DGs. The switching frequency of the DG inverters is 10 kHz. In the simulation unbalance compensation is activated at t = 0.3s.

In the current study, voltage unbalance factor is considered as the index of unbalance and is defined as follows:

$$VUF = \frac{V_{0rms}^{-}}{V_{0rms}^{+}}.100 \tag{18}$$

Where V_{0rms}^{-} and V_{0rms}^{+} are the rms values of the negative and positive sequence of the DG output voltage, correspondingly.

The three phase negative as well as positive sequence attributes are balanced, so that VUF phase value has independence in its calculation. Due to the effect of compensation, as shown, the VUF values are considerably reduced. VUF of DG2 is slightly greater over DG1, due to asymmetrical line impedances.

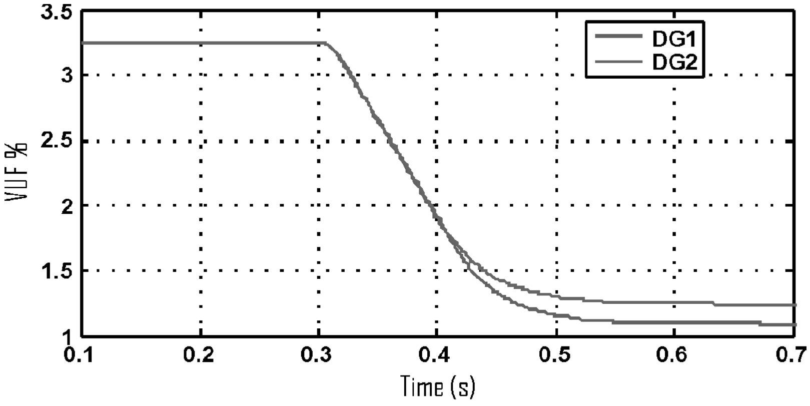

Figure 4: Voltage unbalance factor

Figure 5, Figure 6 and Figure 7, Figure 8 represents the output voltage waveforms of DG1 and DG2, before and after compensation correspondingly. Such figures show the efficiency of this suggested compensation scheme to balance the DG inverter output voltages. In these three phase waveforms in above figures, the colors pink, green and red signifies line voltages (Vab,Vbc,Vca) correspondingly.

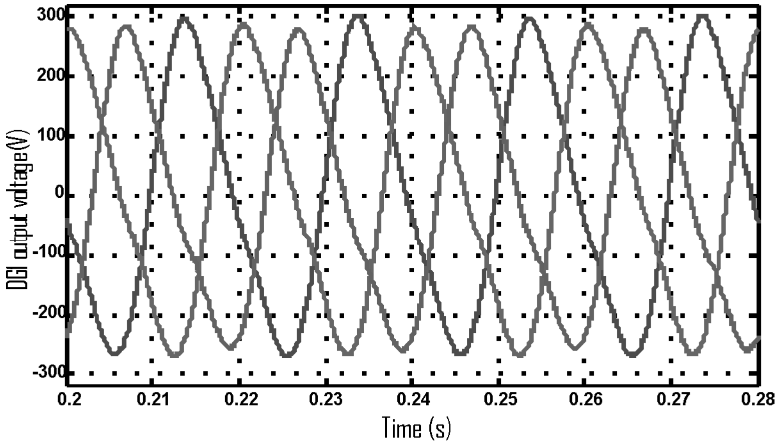

Figure 5: DG1 output voltage (before compensation)

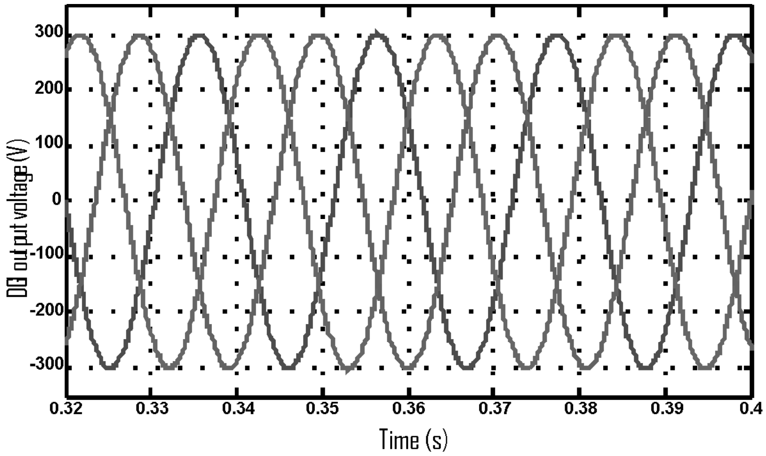

Figure 6: DG1 output voltage (after compensation)

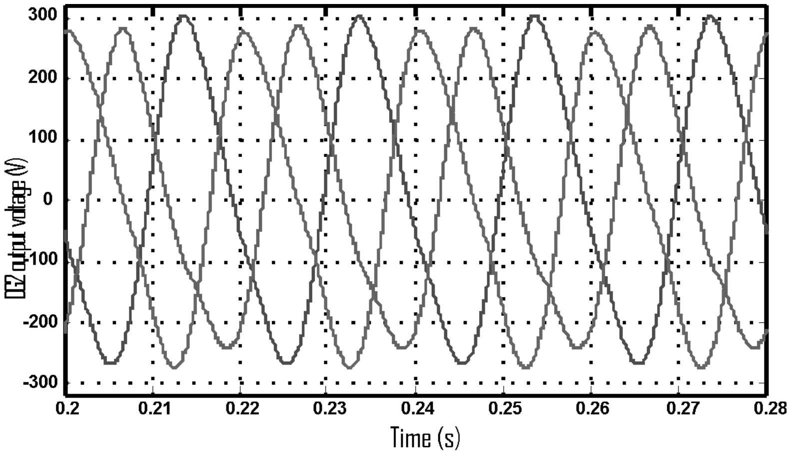

Figure 7: DG2 output voltage (before compensation)

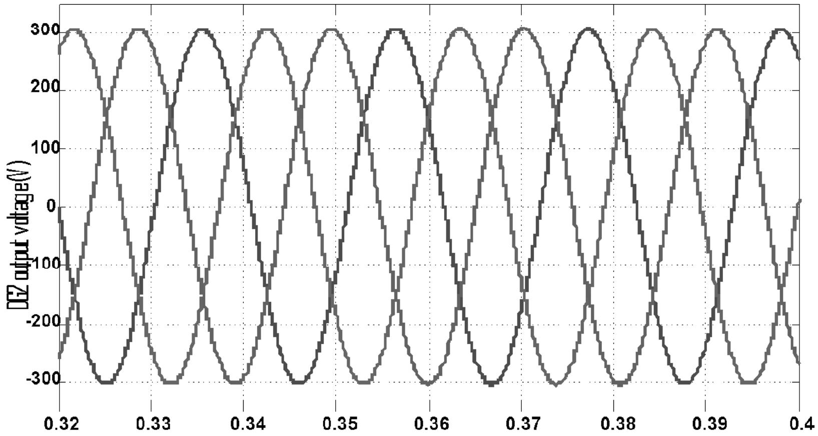

Figure 8: DG2 output voltage (after compensation)

The simulation effects of DG1 3 phase output current prior as well as post compensation are shown in Figure9 and figure10. The consequent waveforms of DG2 are presented in Figure11 and 12. As the load is linked between phase-a and phase-b, the current in these phases are around similar (pink as well as green waveforms),

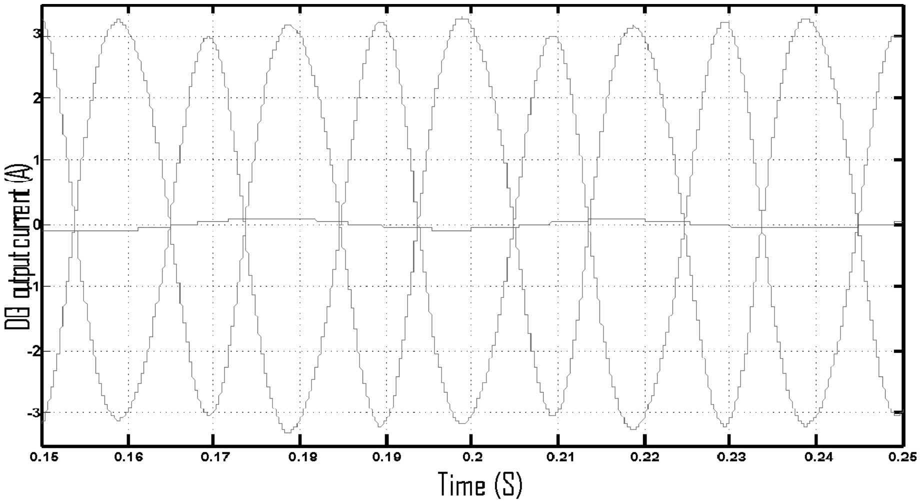

Figure 9: DG1 output current (before compensation)

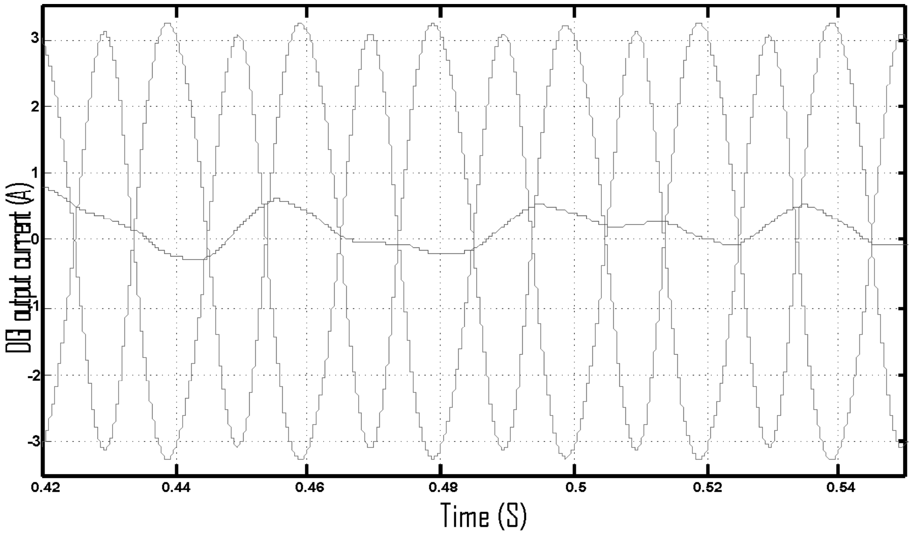

Figure 10: DG1 output current (after compensation)

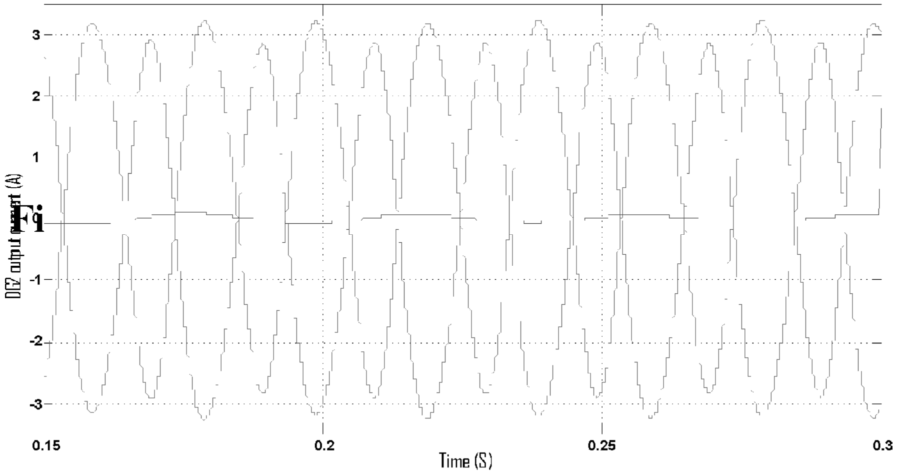

Figure 11: DG2 output current (before compensation)

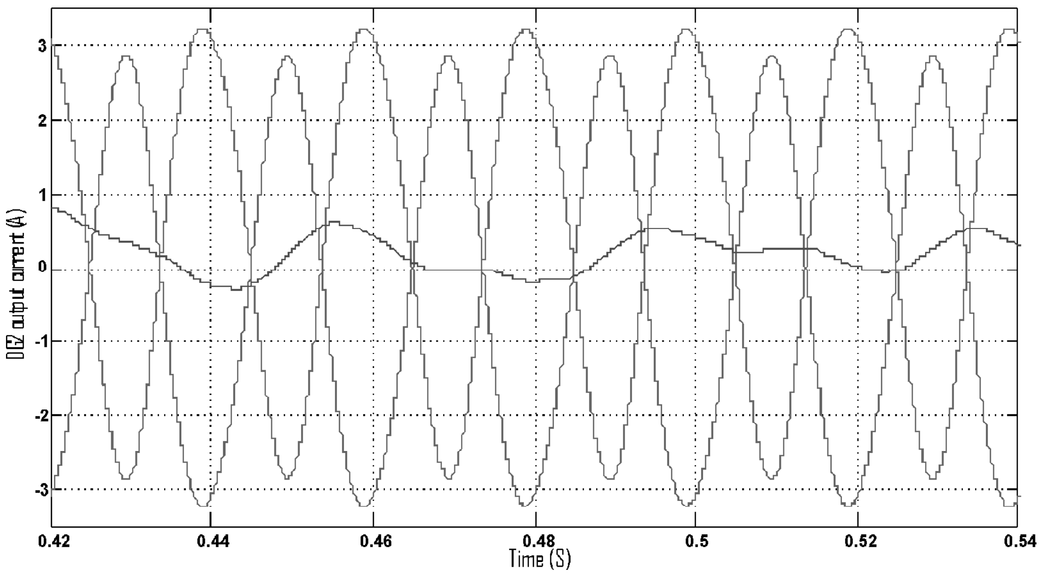

Figure 12: DG2 output current (after compensation)

and the phase-c current (red waveform) is roughly 0. Voltage unbalance is being generated by the unbalance load current. To decrease voltage imbalance, the compensation control action show the way to a slightly increased phase-c current.

The consequence of DGs negative sequence reactive power due to the compensation is shown in Figure13.

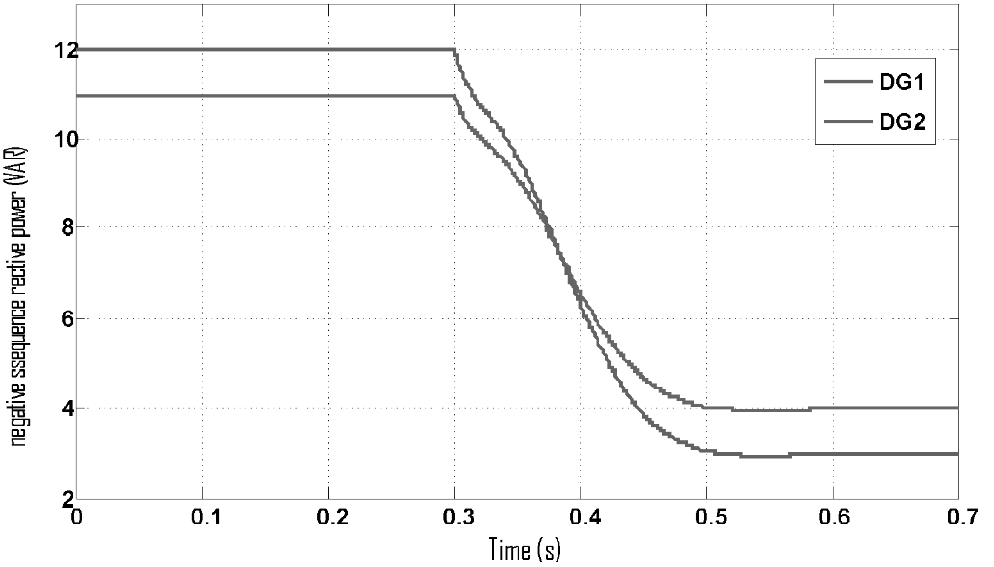

Figure 13: Negative sequence reactive power

Because of the compensation Negative sequence reactive power is reduced. The reduction in this reactive power provides sharing the compensation effect. The simulation consequences of positive sequence reactive power as well as active power sharing among 2 DGs are exhibited in Figure 14 as well as Figure 15 correspondingly. The unbalanced load is entirely resistive, reactive power values are too less.

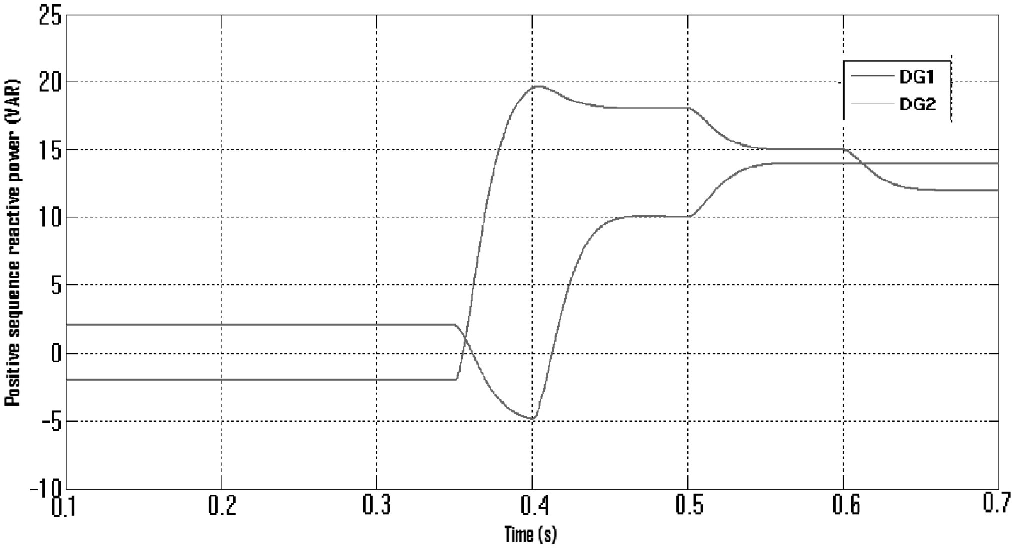

Figure 14: Positive sequence reactive power

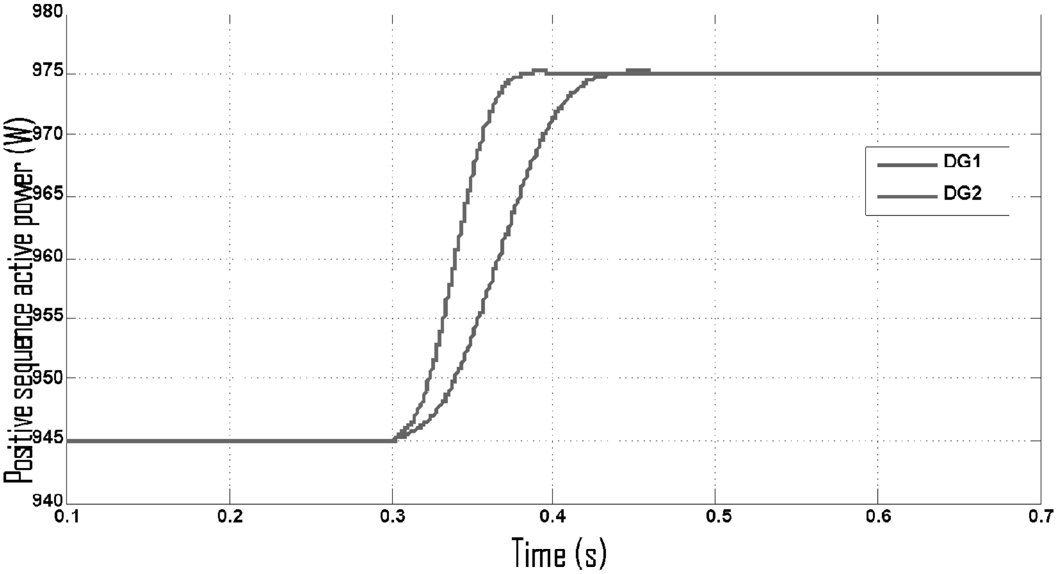

Figure 15: Positive sequence active power

As exhibited in Figure15 active power is shared earlier than compensation as well as after the transient state created by compensation activation, sharing is again attained. Such consequences demonstrate the power control efficiency. Additionally it terminated that the compensation has no negative effect on power sharing.

To obviously demonstrate the compensation effect its control loop is simulated abruptly. However in realistic cases, to evade the transient behavior unbalance compensation gain should be gradually improved which is observed in Figure14 and 15.

The THD of output voltages of DG1 and DG2 after unbalance compensation are exhibited in Figures16 as well as 17 correspondingly. THD of output voltage before compensation is 19.77%. After the implementation of compensation technique THD value is effectively reduced to 5.51%.

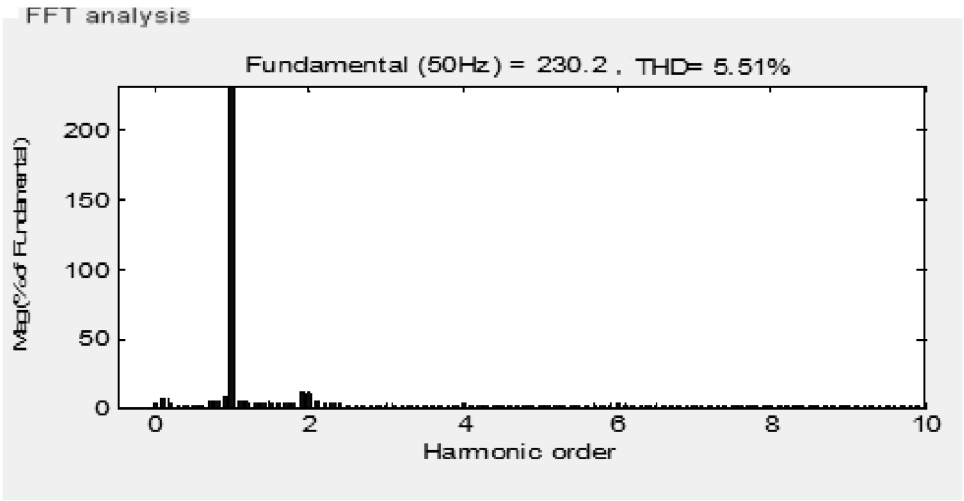

Figure 16: THD of DG1output voltage

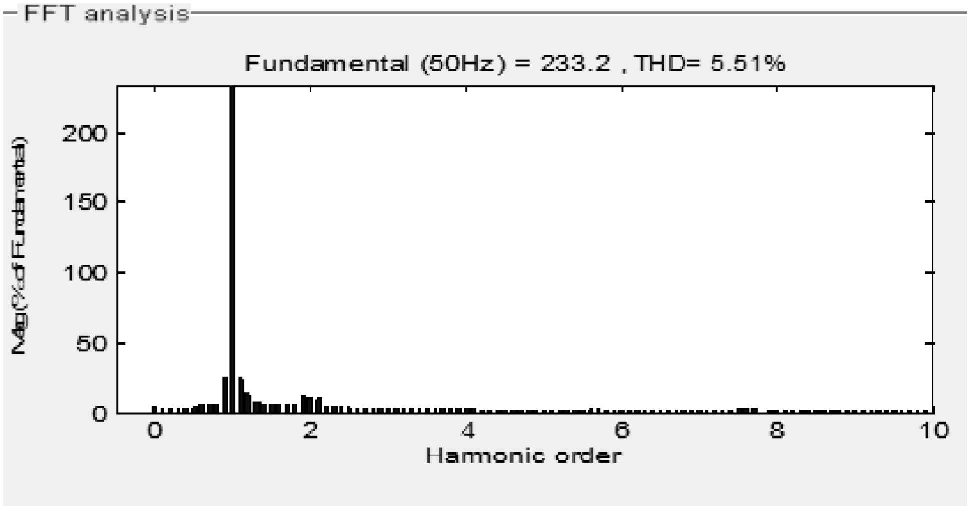

Figure 17: THD of DG2 output voltage

4. CONCLUSION

Here a control approach had been proposed to recompense for voltage imbalance in a microgrid. This concept was based on the DG Interface inverter control. Voltage imbalance and harmonics Compensation in an islanded microgrid was conferred through droop controllers, the negative sequence reactive powers were used to produce the DG inverter output voltage references amplitude as well as phase angle. The negative sequence reactive power had been pertained to voltage unbalance compensation reference. Microgrid harmonics are condensed by compensation of selective main harmonics by means of resonant controllers. The acquired results showed that the voltage imbalance was better compensated by exploiting the control scheme and the compensation effort was appropriately shared among the DGs.

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