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Low-Voltage Ride-Through for a Single-Phase Transformerless PV system using HERIC Topology

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ABSTRACT

In this booming era of renewable sources of energy generation,especially the usage of PhotoVoltaic (PV) grid-connected systems has been shown a substantial growth in the last few decades and may show a further increase in the near future. This upcoming scenario also at the same time raises disquiets about the quality, reliability and availability of the usage power. Transformerless Photo Voltaic (PV) inverters are more commonlyimplemented in order to achieve to higher efficiency and to reduce the cost and carbon emission. But complications may develop in the PV panels-integrated distribution system due to the protection of Anti-Islanding problems which may result in grid disturbances. Secondary services such as fault ride-through are required to support the PV panels system beneath fault under grid condition. In this article, the Low Voltage Ride Through (LVRT) for a single phase transformerless PV system are implemented by using MATLAB/Simulink. Further, the HERIC inverter topology followed by the controllers used for LVRT and the MPPT algorithm are discussed

Index Terms: Transformerless Inverter, PhotoVoltaic (PV), Fault ride-voltage, HERIC topology, AC-AC bypass, MPPT and Perturb and Observe algorithm.

1. INTRODUCTION

A nonlinear extrapolative energy administration approach for a inhabited a rooftop PV scheme for a building and battery energy stowage was described by Chao Sun et al.[1]. An imperative novelty of this document is concluding the gap amongst building energy management preparations, unconventional load predicting methods, and nonlinear battery-operated/PV models. Moreover, we centre on the basis trade-off amongst battery aging and economic function in energy organization. It is expressed as a model predictive controller (MPC) can be used for the energy administration issue.

The organization of a microgrid control with dispersed energy assets associated with a single bus was deliberated by J.B.Almada et al.[2]. The microgrid management scheme utilizes a integrated and investigative method that deliberates the stochastic construction of a PV module power source, the usage of a FC, the SOC of operated batteries, the adjustable load profile, and the flag colour of different electricity tariffs. The control scheme aim is the reliable and monetary by means of energy sources and their amalgamation to power circulation schemes while stabilizing the power quality issues. The replies concerning the control scheme of the inverters related to the disseminated energy resources present in the microgrid are assessed at the time of the grid connection, autonomous operation, and evolution amongst the above-mentioned functioning modes.

In recent years the installation of photovoltaic (PV) systems has been flourishingbecause of therapid development of photovoltaic systems and the reduced cost of PV modules. The basic requirement of the

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grid are given in grid regulations like voltage stability, frequency stability and power quality [3]. When the grid fault are present then it is essential that PV systems should be terminate to strengthen local loads .It is also called as an anti-islanding protection.

An unplanned pv systems connected to grid can create more problems like frequency disturbance, voltage swell , sag voltage interruptions,voltage flickers and power outages during islanding operation mode.Many countries like European, Germany, Italian etc have developed different codes for different voltages (e.g low/medium voltage pv systems) to solve the potential issues ,the generated units should couple to the low voltage grid with the minimal power over and above 1 kW have to drive through voltage faults occurs on the grid[4].

2. PHOTOVOLTAIC GENERATION

The PV cell (array) is explained as a corresponding circuit that comprises of a diode connected in parallel with current source I_{cs} and resistance Rp all in sequences with resistor R_s. R_s models the resistance among the contactor and semiconductor material. The overriding equations (1), (2), (3) and (4) are,

$$V_{dv} = V_{cellv} + I_{pvc} R_{sr} \tag{1}$$

$$I_{pvi} = I_{csi} - I_{si} \left[e^{\frac{(qV_{dv})}{AKT_{pv}}} - 1 \right] - \frac{V_{dv}}{R_{pr}} \tag{2}$$

$$I_{si} = I_{s,r} \left(\frac{T_{pvt}}{T_{rt}} \right)^3 e^{\frac{qE_{bg}}{AK}\left(\frac{1}{T_{rt}} - \frac{1}{T_{pvt}} \right)} \tag{3}$$

$$I_{csi} = \left[I_{s,r} + K_I \left(T_{pvt} - T_{rt} \right) \right] \frac{S_{pvs}}{1000} \tag{4}$$

Where, V_{dv} are the diode voltage and V_{cellv} PV cell voltage, correspondingly; the output current of PV cell is I_{pvi}, and I_{si} is the cell saturation current; q, A and K are an ideal factor, an electron charge, the Boltzmann's constant, correspondingly; I_{sr} is the cell's reverse saturation current at reference temperature T_{rt}; E_{bg} is the Energy band-gap; K_I is the cell's short circuit current temperature coefficient, S_{pvs} represents that the irradiance of the PV. The cell model is raised to a PV arrangement by keeping in mind η_{pv} cells in sequences, thus the hodgepodge power is specified as equation (5),

$$PV_{dv} = \eta_{pv} V_{cellv} I_{pvi} \tag{5}$$

- For brevity, we only abridge the PV model equations (1) to (5). Note that a MPPT algorithm like perturb and observation (P&O) technique is typically engaged to progress PV efficacy.

There are many MPPT methods present to get the maximum output power. In this paper MPPT algorithm like Perturb and Observe technique is used.The P & O algorithm is operated by the occasionally perturbing (decreasing or increasing) current or the terminal voltage and then compare with the output power by the previous iteration of the perturbation cycle [5].

3. NECESSITY FOR LVRT

The necessity of high efficient, reliable, reduced carbon emissions and cost reduction has led to development of innovative inverter topologies. The foremost method is used to improve the efficiency in directionto remove the transformer. The leakage currentsflows because of the capacitance coupling to earth in the absence of galvanic isolation of pv modules. Henceforth the transformerlessc onfiguration needs additional composite solutions, typically resulting in advanced topologyto keep the DC and leakage currents injection beneath current control to comply by safety purpose. Ideal transformerless inverter produces constant common mode voltage. Howeverleakage current is produced , if the voltage varies with the time. For minimizing of this leakage current various transformerless topologies are developed by connecting additional power semiconductor devicesto the single phase full-bridge inverter[6].It is enhanced for the transformerless PV inverters equipment with LVRT control to fulfill the forthcoming requirements reliably and efficiently. Power losses, dynamic responses and Current stresses of transformerless PV configuration inverters are reliant on both LVRT and normal operation mode. Thus, it is essential to explore the performance of PV modules under LVRT.

4. INVERTER

A single-phase PV array inverter is primarily connected to LCL-filter then to the grid which makes the injected current quality. In grid connected pv system. When the transformer is removed , safety concerns arises e.g leakage currents due to the deficiency of galvanic isolations[7]. So The leakage current produces by these transformerless inverters should eliminate or can be reduced by modifying the modulations or adding passive damping components .However, the exchanging of reactive power takes place between the capacitor CPV, core losses present in the output and LCL-filter during every switching period, leading to a low efficiency. Number of transformerless topologies have been improved for increasing the efficiency and reduction of the leakage current, most of topologies which are based on the Full Bridge inverter. The main priority of a transformer less inverter is to evade the generation of changing Common Mode Voltage inverter.

$$V_c = \frac{V_{ao}}{2} + \frac{V_{bo}}{2} \tag{6}$$

$$I_c = C_P \frac{dv_{cmv}}{dt} \tag{7}$$

4.1. HERIC Inverter:

By using Full bridge converter sunways, derives a new topology and recognized as “Highly Efficient and Reliable Inverter Concept” (HERIC), whereas IGBTS with two number are connected as a bypass leg of the AC side and operates at grid frequency [8]. Figure 2.1 shows the HERIC configuration whereas L_{fi}, L_{fg} and $C_{nf}C_{fc}$ are the output filter inductors and DC-link capacitor ,filter capacitor respectively present on the inverter and grid side, The bypass legof the inverter has two important features: the PV module decouplesfrom the grid.High-frequency voltage Components across the PV module inverter are avoided and alsothe exchanging of reactive power between the inductors and Dc link capacitors C_{in} is preventing during the

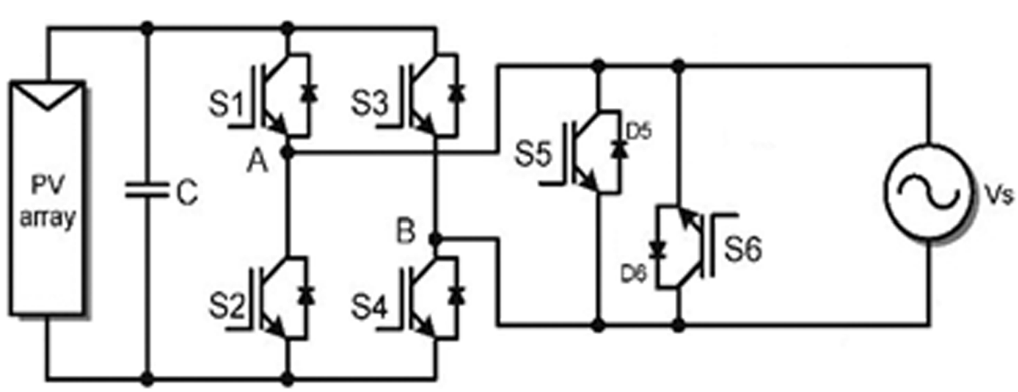

Figure 4.1: HERIC Inverter Topology

Table 4.1
Conduction states for HERIC Inverter

S1	S2	S3	S4	S+	S-	D+	D-	V_{OUT}
OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	0
ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	V_{IN}
OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	0
OFF	ON	ON	OFF	OFF	ON	OFF	OFF	$-V_{IN}$

zero voltage state, so that substantial efficiency increases. During the negative half cycle of converter operation S- remains connected S_2 and S_3 are commutated at switching frequency as it follows in Table 4.1. It means that when S_2 and S_3 are ON an active vector is present, thus the current flows to the load from the from the PV module, when S_2 and S_3 turn off, a zero voltage vector is present across the load, then current flows through S- and D+. During the positive half-cycle S- turns offand S+goes on , whereas IGBTS1 and IGBT S4 commutated at switching frequency which generates both active and zero vectors. When an active vector occurs (IGBT S1 and IGBT S4 are ON), current flows to the gridfrom PV modules, when a zero vector is present, IGBT S1 and IGBT S4 are switches OFF it is freewheeling condition during this period the current flows from S+ and D-.

4.2. Filter Topologies

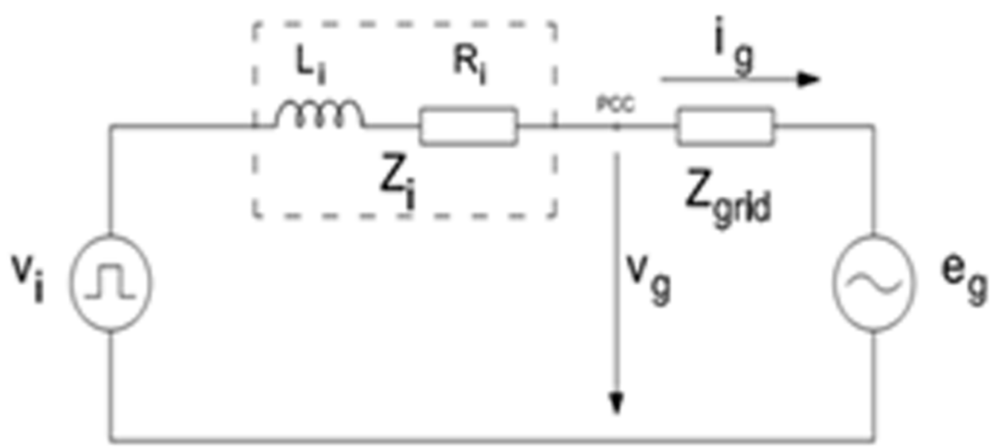

Figure 4.2: Circuit configuration of an L filter

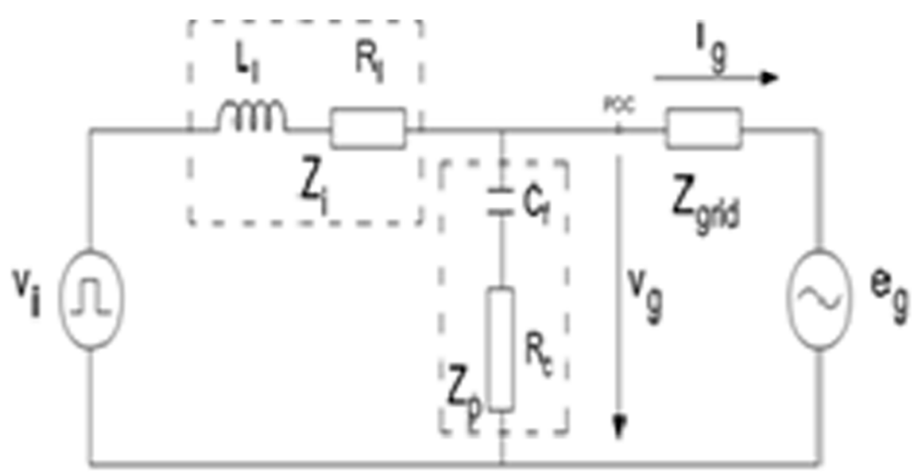

Figure 4.3: Circuit configuration of an LC filter

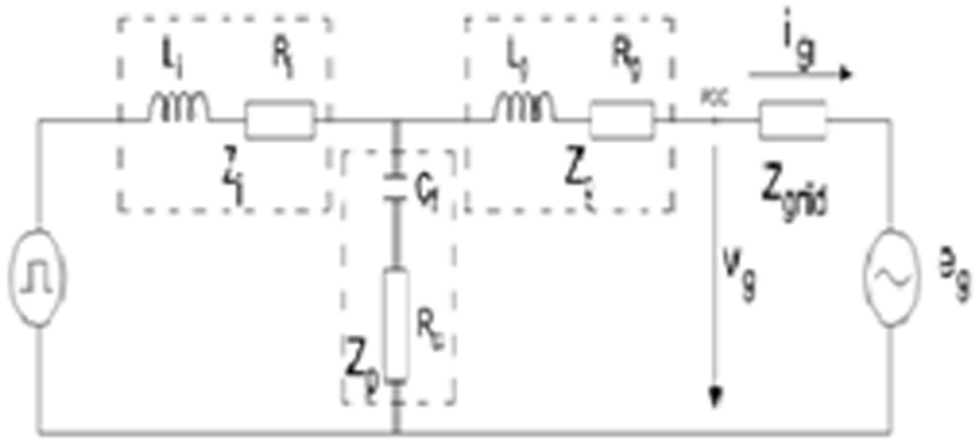

Figure 4.4: Circuit configuration of an LCL filter

4.2.1. L Filter

Fig. 4.2, shows L Filter configuration that consists of an inductor alone in series with the inverter which acts as a filter .In this topology, Z_g = 0, Z_i is finite and Z_p is infinite .The main disadvantage of filter is poor system dynamics due to voltage drop across the inductance that causes large response time. Therefore, a L- filter is used to obtain a good damping.

4.2.2. LC Filter

Fig. 4.3, showsLC Filter configuration comprises of an inductor and a capacitor which is connected to the inverter and a capacitor which acts as a filter .In this configuration, Z_g= 0, Z_i and Z_p is also finite .The value of inductance can be reduced by connecting this parallel capacitor, therefore costs and losses are reduces. By using this large capacitance, other problems also may occur like large capacitance currents at fundamental frequencyand inrush currents or dependendant of the filter on grid impedances for overall harmonic attenuations

4.2.3. LCL Filter

Fig. 4.4 shows LCL Filter configuration contains of two inductors and one capacitor are connected with the inverter and a capacitor which acts as a filter and another inductor connected in series to the grid[9]. With the increase in the size of the capacitance leads to areducethe weight of the filter and cost. It gives the benefit of providing a improved decoupling betweengrid impedance, the filter and a lower ripple free current stress across the inductor.

5. LOW-VOLTAGE RIDE-THROUGH CONTROL

Single-phase transformerless PV module system with overall organized control structure and LVRT capability as shown in the fig 5.1. According to the requirements of the grid, The new generation transformerless PV arrays should focus on the design of grid current shape and also the performance of reactive power injection under fault condition of the grid.In this article current and voltage control strategy are implemented so that current protection and power quality issues of the inverter can be taken care by the inner control loop[10]. An outer voltage control has responsibility of the voltage or power control to producerequiredreference currents for the inner control of the system[11].

The implemented current control approaches like proportional resonant (PR) control, deadbeat (DB) and repetitive controller (RC) are more powerful techniques for tracking sinusoidal signals without steady state errors[12]. The current controller tracking performance can be improved by using PI controller and adding the Harmonic compemsator. Thus itis selected as the inner current control

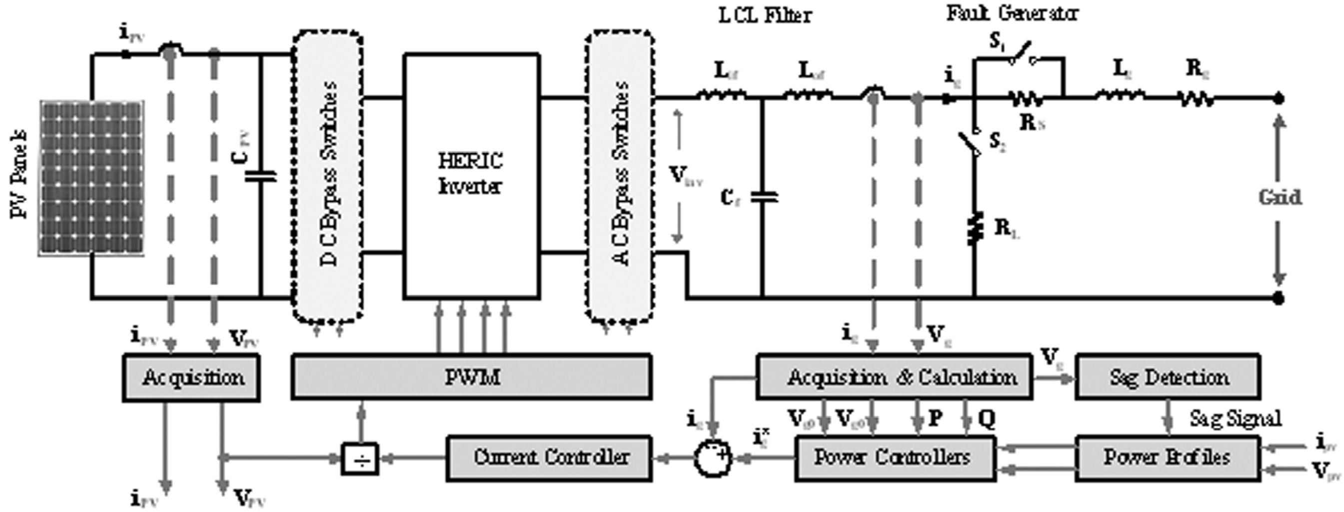

Figure 5.1: Schematic block diagram of LVRT of Single-Phase Transformerless PV Inverter

$$G_i(s) = K_\infty + K_\beta \frac{s}{s^2 + w_0^2} + \sum_{m=3,5,7} \frac{K_{rm} S}{s^2 + h^2 w_0^2} \tag{8}$$

K_∞ = proportional gain, K_β = resonant gain for first order, K_{rh} = control gain for m^{th} order resonant controller

The outer voltage control provides voltage amplitude and frequency required for the grid operation and also produces required reference current, subsequently can be uses inside inner current control loop. Thereforereactive power injection also can be used to this loop to tune the grid current in LVRT operation mode [13]. The quadrature signal can be generated by many methods like the inverse Park transform, Hilbert based method, and the Second Order Generalized Integrator (SOGI).The advantageSOGI generation system is delay-free property and simple implementation and therefore it is used in this article .

6. RESULTS

The structured diagram of LVRT for a Single phase transformerless PV inverter is constructed. The HERIC inverter modeling and Low-Voltage Ride-Through controlling are performed and the resultant figures are plotted as shown below for a system of 1kW.In this project the SOGI-based phase locked loop is used as the synchronization unit. The sag generator is used for generating a voltage fault in the system by using IGBT switches S1 and S2.

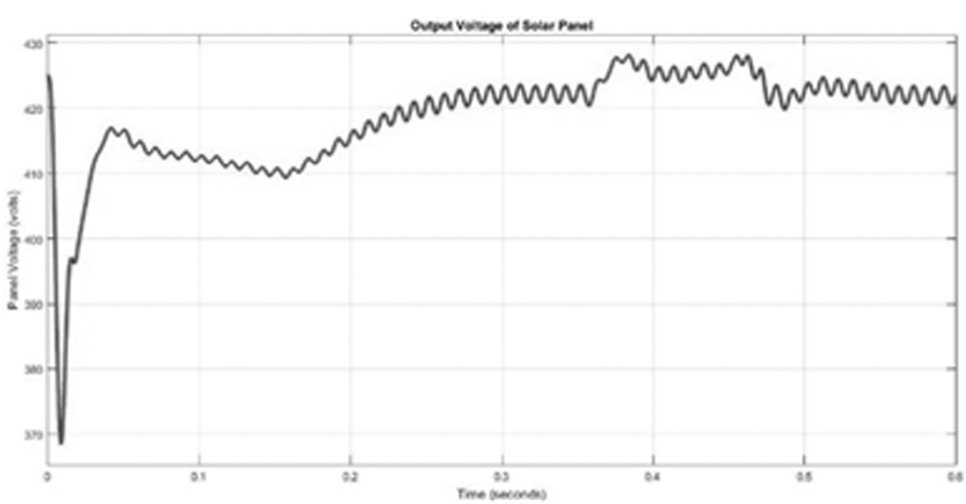

Figure 6.1: Output Voltage of Solar panel

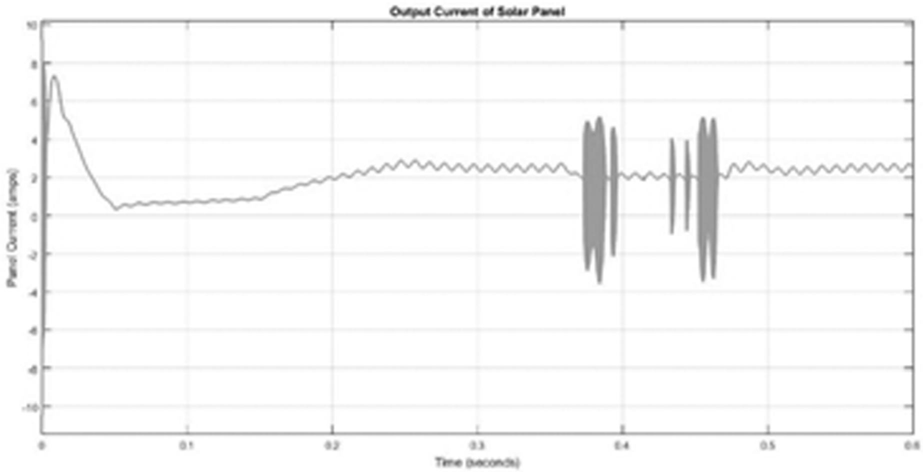

Figure 6.2: Output Current of Solar panel

Figure 6.1 shows us the solar panel output voltage (CA-CS6X-315P), the sudden variation in the voltage in the first 0.1 seconds of the simulation time can be explained by the change in the sun's irradiance.Figure 6.2 shows us the output current of the solar panel, the sudden variation in the current at 0.35 sec and 0.45 sec of the simulation time can be explained due to occurrence of a line to line fault at the grid causing a sudden draw of current.

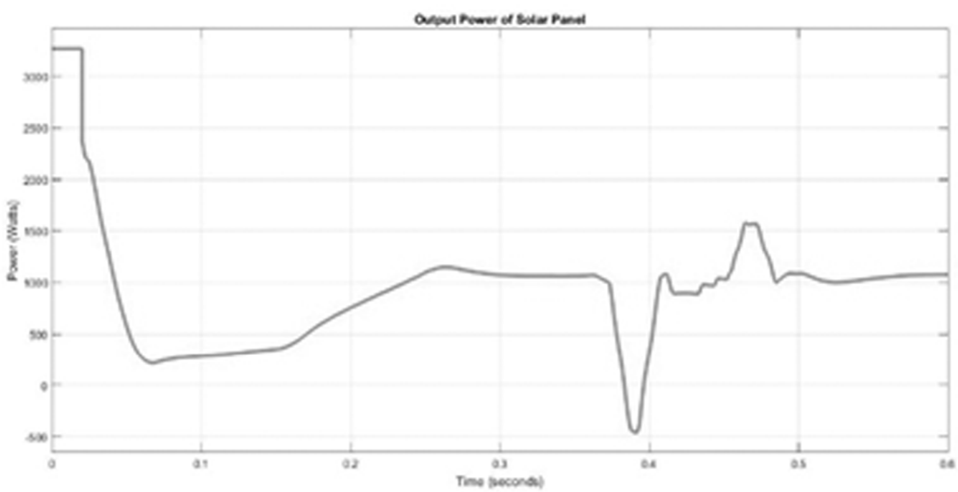

Figure 6.3: Output Power of Solar panel

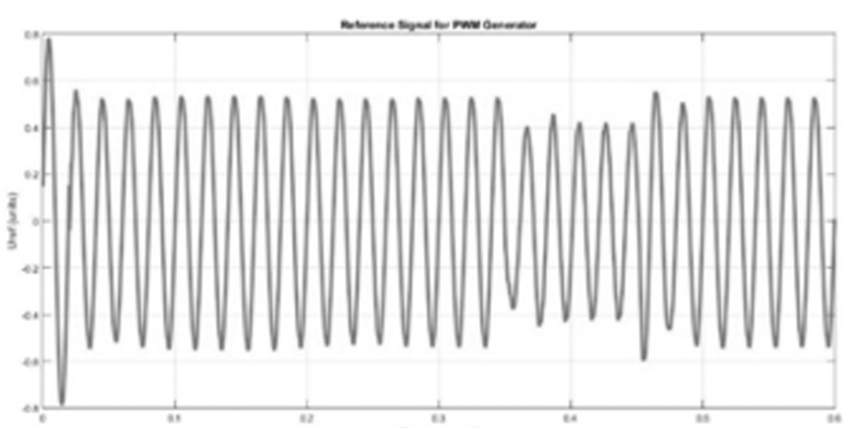

Figure 6.4: Output reference signal for PWM generator

The power outage of the solar panel is shown in figure 6.3 and it can be noticed that it takes around 0.25 seconds to settle to 1KW. The sudden changes reflected in the figure are due to the presence of the fault in between 0.35 to 0.45 seconds.Figure 6.4 is the U_{ref} signal or rather the reference signal generated according to the gird voltage and magnitude to generate pulses with is used to drive the inverter to convert the generated DC power to usable AC power.

As we know that for a Pulse Width Modulation to occur a reference signal (as same form as the required grid voltage) is to be compared to a repeating sequence in order to generate PWM pulses to drive the inverter. Figure 6.5 shows us a clear comparison of these signals.

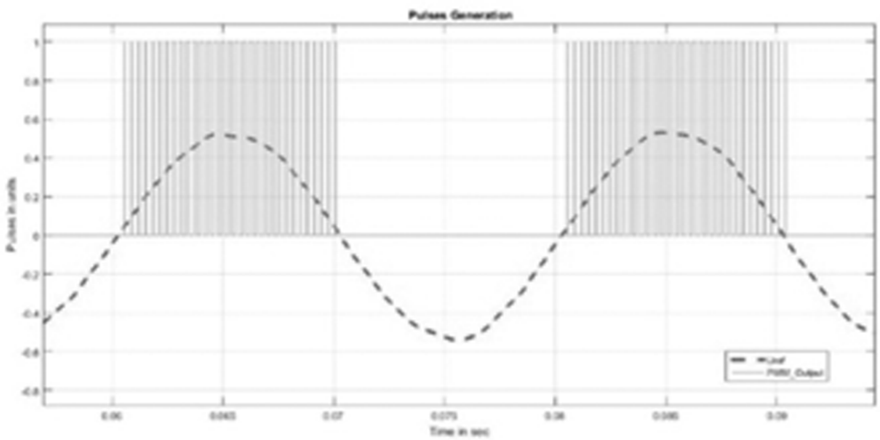

Figure 6.5: Comparison of reference signal to repeating sequence for PWM generation

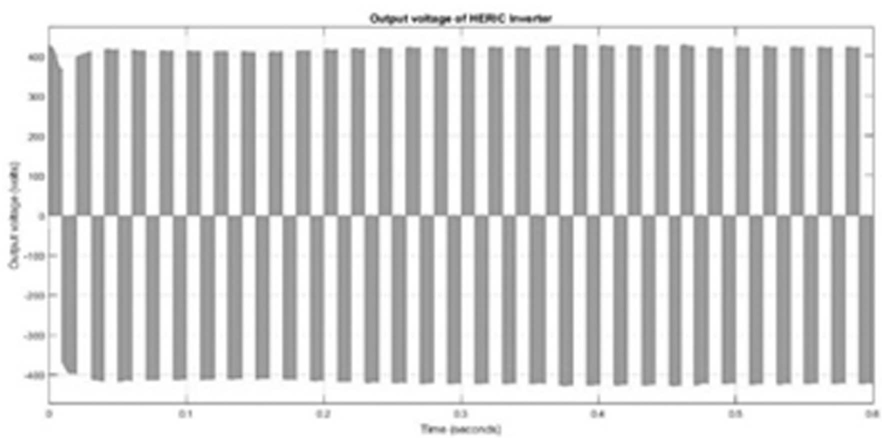

Figure 6.6: Output Voltage of HERIC inverter

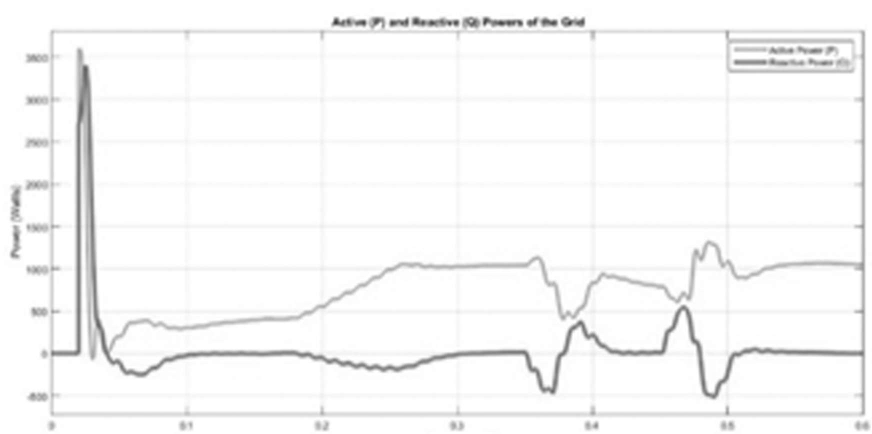

Figure 6.7: Generated Active and Reactive powers of the grid

The output voltage of the HERIC inverter with PWM modulation is shown in figure 6.6 and it is generated by the LVRT control so that the power generated by the solar panel is regulated. An AC bypass branch consisting of two antiparallel IGBT/Diode is used to reduce the thermal stress which my act on the inverter on occurrence of fault.

Figure 6.7 gives us a clear idea of the active power along withthe reactive power of the grid during the run time and the change in powers during the occurrence of powers.Figure6.8 is the simulation result of the gird side voltage during the power transfer from the solar panels to the grid and it can be observed that even though during the occurrence of fault between the period of 0.35 sec to 0.45 sec the voltage dips but does not disconnect the system due to the LVRT control.

Figure 6.9 is the current output on the gird side and it can be seen that during the fault occurrence during the period of 0.35 sec to 0.45 sec of the simulation time period an excess amount of current is drawn irrespective of the sign and considering only the magnitude.

7. CONCLUSION

In this article, a new technique for Single phase transformerless PV inverter based on LVRT control scheme have been proposed. More specifically, the modeling of different components, the control strategies for the single phase conversion and LVRT control strategies have been studied and analyzed. A Single phase

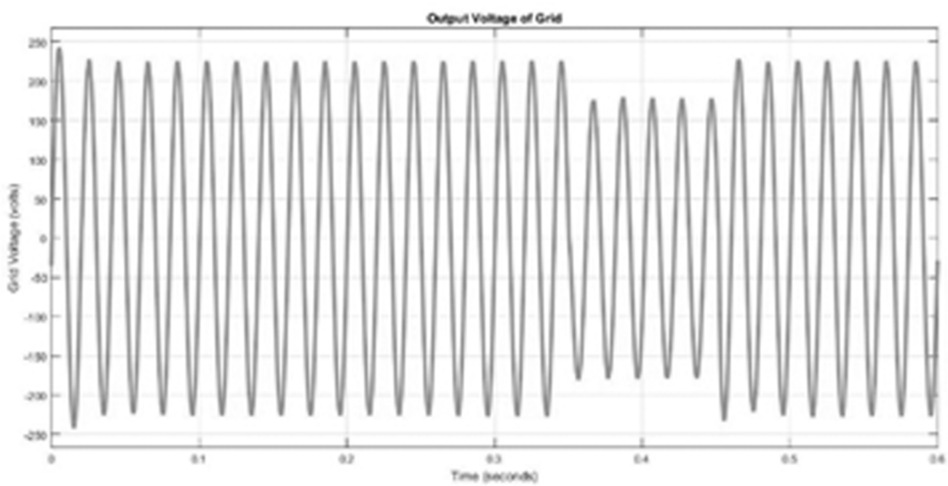

Figure 6.8: Output Voltage of the grid

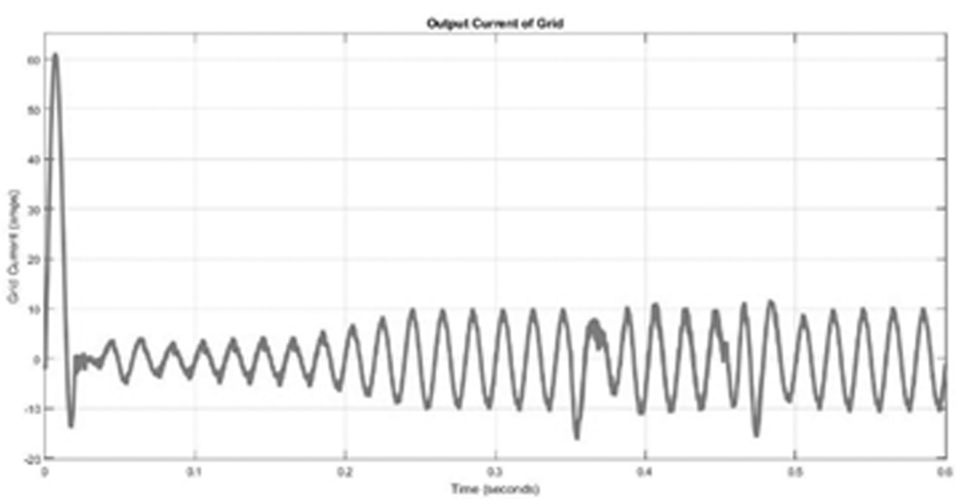

Figure 6.9: Output Current of the grid

transformerless PV inverter equipped with LVRT was developed in a MATLAB/Simulink, which simulates the dynamics of the system during normal and faulty conditions.The study illustrates that higher efficiency can be achieved by the HERIC inverter .The Panel voltage is regulated using a PI controller.The reactive power is controlled by using PI controller. The robustness provided by the SOGI technique for control of the PV system helped in faster retention the system during the faulty conditions and protecting the grid from disconnecting. The simulation results show that the response of the system is fast with the use of LVRT control strategies and provides a better running PV for the domestic purposes

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