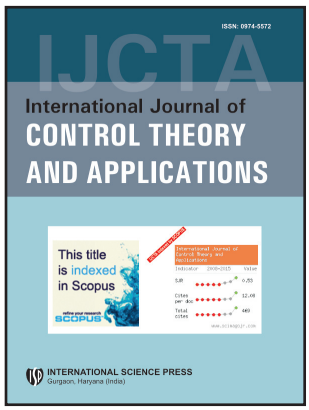

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Design and Performance Analysis of Cascaded H-Bridge Multilevel STATCOM

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Abstract: Two control algorithms are presented in this paper for STATCOM that meets the requirement of load reactive power and correspondingly voltage balancing of isolated dc capacitors for H-bridges. The control techniques used for an inverter in this paper are Sinusoidal Phase Shifted Carrier (SPSC) and Third Harmonic Injected Phase Shifted Carrier(THIPSC). The STATCOM performance for the different load changes is simulated with MATLAB/ SIMULINK environment and the performance parameters such as balancing the DC link voltage, THD for the inverter output currents and reactive power components provided by STATCOM to load are compared for both control techniques of the inverter.

Keywords: Sinusoidal Phase Shifted Carrier, STATCOM, Third Harmonic Injected Phase Shifted Carrier, Cascaded Multilevel Inverter.

1. INTRODUCTION

The static synchronous compensator (STATCOM) is widely accepted as a consistent reactive power controller [1]. The reactive power required by load is supplied by STATCOM [2]. In high power requirements, Reactive Power Compensation is done by multilevel inverters [3]. Cascaded Multilevel Inverter (CMLI) topology has become popular choice for the implementation of high power STATCOM systems. Because of modularity and flexibility CMLI has become most popular [4]. This eliminates a heavy, bulky, and expensive transformer for the cascade STATCOM [5]. Due to disparity in conduction and the losses in the switching devices, the voltages across the capacitor are unbalanced. Maximum research is happening on balancing the voltages across the DC link capacitors in multilevel inverters. Different control techniques using various topologies are described in [5-9].

To maintain balanced DC link voltage in each H-bridge and to supply load reactive power requirements two control strategies are proposed for the five level STATCOM in this paper. The topologies used for the cascaded

multilevel inverters are Sinusoidal Phase Shifted Carrier (SPSC) PWM and Third Harmonic Injected Phase Shifted Carrier (THISPSC) PWM. The Phase Shifted Carrier strategy can lead to the termination of complete carrier and related sideband harmonics up to 2Nth carrier set where N is the total H-bridges in a phase. In this paper the simulation results of multilevel STATCOM for different load changes are presented and these results are compared for two different control strategies.

2. CASCADED MULTILEVEL INVERTER BASED STATCOM

The five-level STATCOM with a cascaded H bridge multilevel inverter is shown in Figure 1. The STATCOM consisting of Cascaded Multilevel Inverter, which is coupled through coupling reactors to a power system. In this strategy two single phase H-bridge inverter cells with capacitors as DC link are joined in sequence to produce five levels of phase voltage. The phase voltage levels are 2N + 1, where N is single phase inverter cells present in a phase and the number of levels in line voltage are 2m − 1, where m is the phase voltage levels.

In the design of STATCOM, the three phase quantities v_a, v_b, v_c, i_{al}, i_{bl}, i_{cl}, i_{as}, i_{bs} and i_{cs} are transformed in v_d, v_q, i^*_{dl}, i^*_q, i_d and i_q in the synchronously rotating reference frame. The mathematical model of the cascaded inverter is converted to the stationary rotating reference frame. Figure 2 shows the control block diagram for the generation of reference voltages to generate switching signals for the inverter. The converter voltage *d*-*q* axes reference components e_d and e_q are measured as

$$e_d = x_1 + v_d - \omega \mathrm{L} i_q \tag{1}$$

$$e_q = x_2 + \omega \mathrm{L} i_d \tag{2}$$

where, v_d is the direct axis component of source voltage and i_d, i_q, i^*_{dl} and i^*_q are *d*-*q* axes components of current for the inverter and the load respectively. The reference frame of synchronously rotating and the source voltage vector are aligned together so that the *q*-component of the source voltage v_q is prepared zero. The control parameters x_1 and x_2 are measured as:

$$x_1 = \left(k_{p1} + \frac{k_{i1}}{s}\right)(i^*_d - i_d) \tag{3}$$

$$x_2 = \left(k_{p2} + \frac{k_{i2}}{s}\right)(i^*_q - i_q) \tag{4}$$

The *d*-axis reference current i^*_d is

$$i^*_d = \left(k_{p2} + \frac{k_{i2}}{s}\right)[(\mathrm{V}^*_{dc}) - (\mathrm{V}_{dc1} + \mathrm{V}_{dc2} + \mathrm{V}_{dc3} + \mathrm{V}_{dc4} + \mathrm{V}_{dc5})] \tag{5}$$

where, V^*_{dc} is the reference DC link voltage and V_{dc1} to V_{dc6} are voltages across the DC link capacitors in each H-bridge. Figure 2 shows the generation of reference signals for PSCPWM. The unit signals sin*wt* and cos*wt* are produced from Phase Locked Loop (PLL) block with source voltages. The reference frame of stationary quantities are converted in to reference frame of synchronous rotating as:

$$e_{ds} = (\cos \omega t) e_d + (\sin \omega t) e_q \tag{6}$$

$$e_{qs} = (\sin \omega t) e_d + (\cos \omega t) e_q \tag{7}$$

From these synchronous rotating reference frame signals, the reference voltages to control the inverter are generated as:

$$v_{ar} = e_{ds} \tag{8}$$

$$v_{br} = -\frac{1}{2} e_{ds} + \frac{\sqrt{3}}{2} e_{qs} \tag{9}$$

$$v_{cr} = -\frac{1}{2} e_{ds} - \frac{\sqrt{3}}{2} e_{qs} \tag{10}$$

3. MODULATION STRATEGIES

Based on carrier arrangements the modulation procedure for multilevel inverters is built. The carrier shifted horizontally is Phase Shifted Carrier PWM (PSCPWM) [10]. Mostly for the cascaded multilevel inverters, PSCPWM is preferred, it gives power dispersal among entire cells consistently and this method is very easy to use individually for all levels of inverters [11]. The PSCSVPWM technique results in the termination of complete carrier and connected sideband harmonics up to 2Nth carrier group, where N is the total H-bridges in each phase. Figure 3 shows the reference and carrier waveform arrangement for a five level SPSC strategy. Triplen harmonics of three-phase PWM inverter will be reduced by selecting pulse number as multiple of 3. Selecting a multiple of 3 is also expedient to use the same triangular waveform can be used as the carrier in all three phases, leading to some simplification in hardware control and implementation. The frequency of switching will be large, to decrease the undesired side things of irregular power flow near switching and to ease minor harmonics in the output voltage.

By adding a third harmonic wave to the fundamental wave of each phase, the three phase inverter modulation index can be increased. The line to line fundamental output voltage will not get effected by this third harmonic component, since between the phase legs the common voltages get cancelled, but the peak magnitude of phase voltages in each phase is reduced, so that without moving into over modulation the modulation index can be increased.

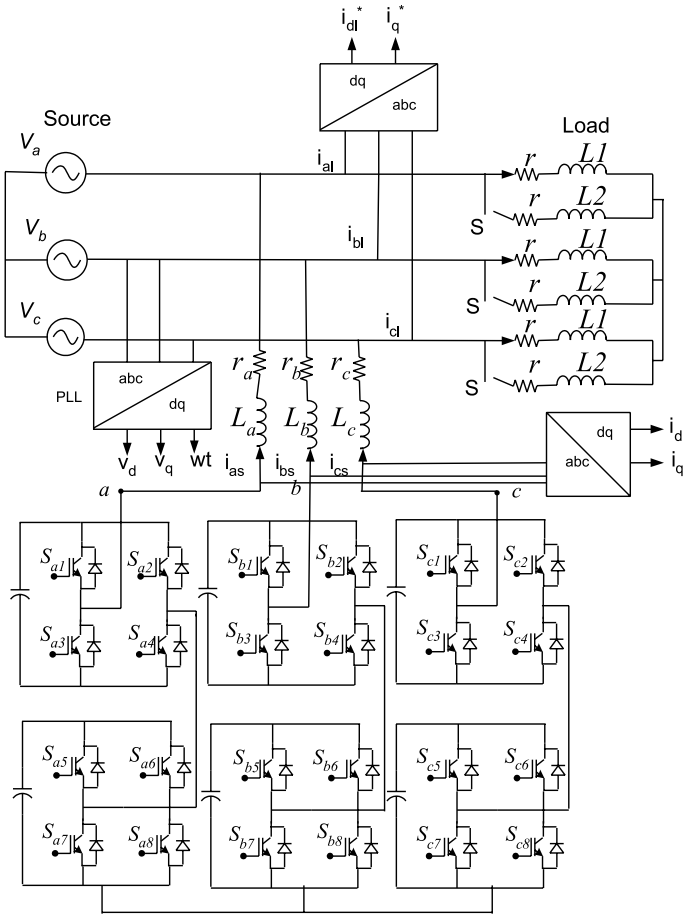


Figure 1: Cascaded multilevel STATCOM

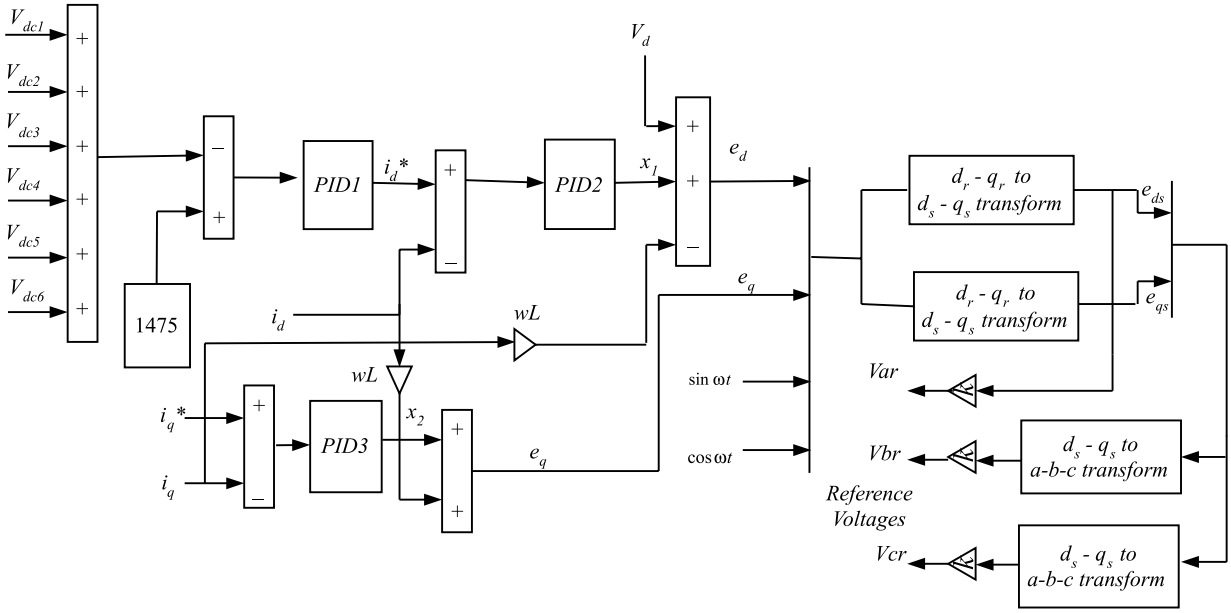


Figure 2: Control block diagram

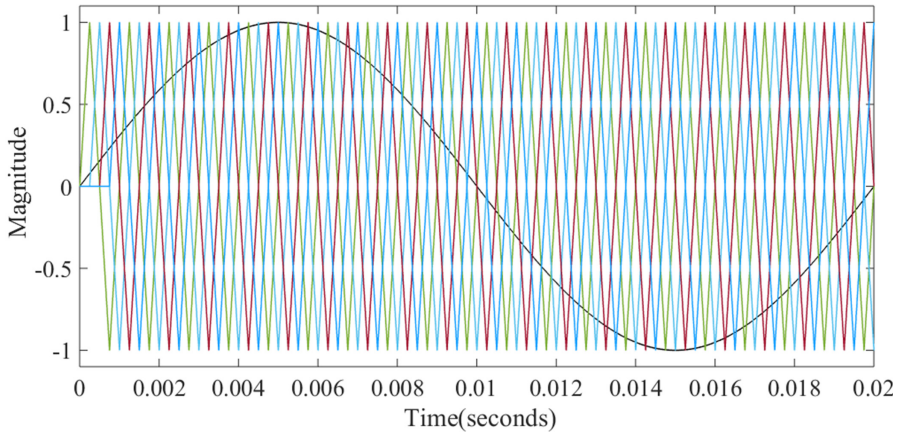


Figure 3: Carrier and reference waveform arrangement for a five level Sinusoidal Phase Shifted Carrier strategy

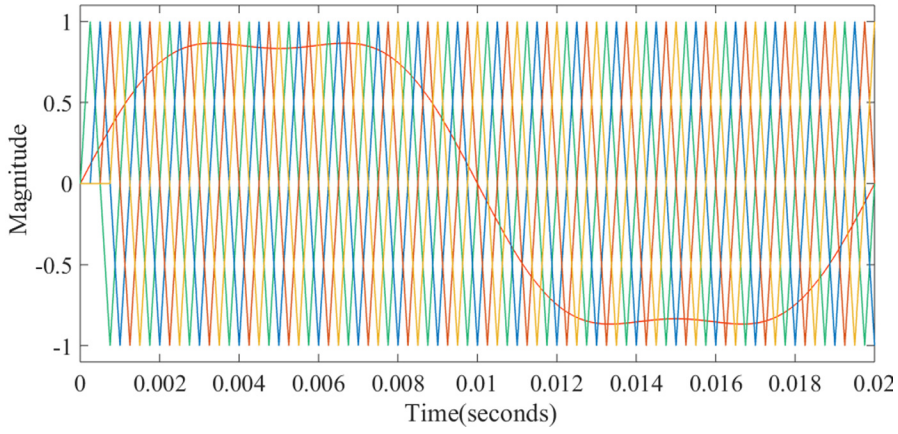


Figure 4: Carrier and reference waveform arrangement for a five level Third Harmonic Injected Phase Shifted Carrier strategy

To maximize the reference waveforms, the magnitude of the third harmonic injected signal is 1/6 and to increase the output fundamental component, the magnitude of fundamental reference waveform is 1.15. Figure 4 shows the carrier and reference waveform arrangement for a five level THIPSC strategy. The reference voltages for THIPSC are:

$$V_a(t) = 1.15 \sin(wt) + (1/6) \sin(3wt) \tag{11}$$

$$V_b(t) = 1.15(wt - 2 \times pi/3) + (1/6) \sin(3wt) \tag{12}$$

$$V_c(t) = 1.15(wt - 4 \times pi/3) + (1/6) \sin(3wt) \tag{13}$$

4. CONTROL STRATEGY

The Figure 4 shows the control block diagram for the generation of reference voltages. The switching frequency ripples in the inverter currents are eliminated by using low-pass filter. From V^*_{dc} and i^*_q loops, the control block generates *d-q* axes reference voltages, e_d and e_q for the cascade multilevel inverter. The inverter is controlled to supply the reactive currents required by load by using these reference voltages. The inverter draws necessary active currents to regulate the dc-link voltage ($V^*_{dc1} + V^*_{dc2} + V^*_{dc3} + V^*_{dc4} + V^*_{dc5}$).

5. SIMULATION RESULTS

The five level Cascaded Multilevel STATCOM is considered for simulation. The simulation is carried out using MATLAB/SIMULINK for different loads and the inverter is controlled with Sinusoidal Phase Shifted Carrier Pulse Width Modulation (SPSCPWM) technique and Third Harmonic Injected Phase Shifted Carrier Pulse Width Modulation (THIPSCPWM) technique. The system parameters are shown in Table 1 and PI controller parameters in voltage control loop and current control loop are shown in Table 2.

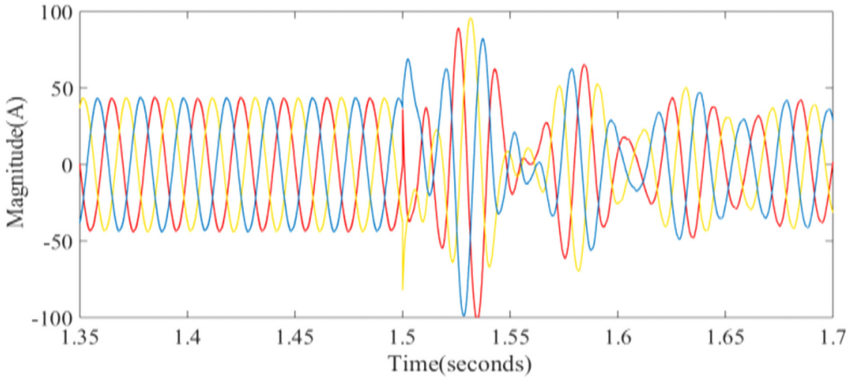
Table 1
Simulation System Parameters

Type of Parameter	*Value of Parameter*
Capacity	25.8 KVAR
Supply Voltage	415 V RMS(Phase-Phase)
DC link voltage	250 V for SPWM 150 for THISPWM
Load Parameters	R = 4.6 Ω, L = 12.4 mH R = 4.6 Ω, L = 5.01 mH (for half load)
DC link capacitance	5 mF
Fundamental frequency	50 Hz
Switching frequency	1200 Hz
STATCOM Interfacing resistance	0.13 Ω
STATCOM Interfacing Inductance	2.19e-3 H

Table 2
Parameters of PI Controllers

PI Controller	*Control Variable*	*Proportional Gain*	*Integral Gain*
PI1	Voltage	0.07	0.2
PI2	Voltage	0.08	0.2
PI3	Current	4	6

The Figure 5 shows the response of STATCOM for various performance parameters such as source current, inverter current, DC link voltage, Reactive components of load, inverter currents and Harmonic analysis of Inverter output current for the variation of load from RL to RC at 1.5 sec with Sinusoidal Phase Shifted Carrier PWM technique. It is observed that the STATCOM works perfectly to a reference DC link voltage of 1475 V, this voltage is equally distributed among all the DC link capacitors and it is balanced for all types of load changes. The reactive components of current required by the load and the reactive components of currents supplied by the inverter are the same even if the load is changed suddenly. The harmonics are very less in the output current no harmonics are present below 20 kHz frequency due to SPSC technique. But during the change of load the source current and inverter current magnitude values are almost double the normal value.



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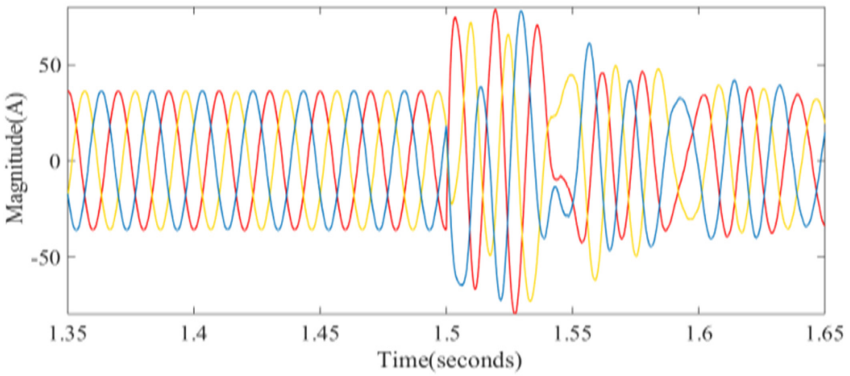

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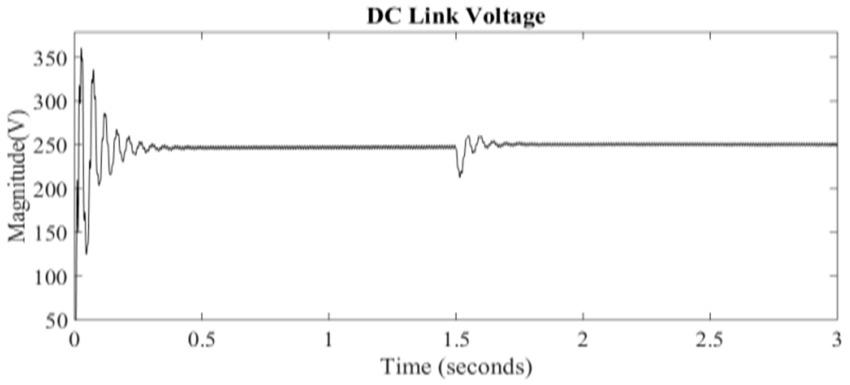

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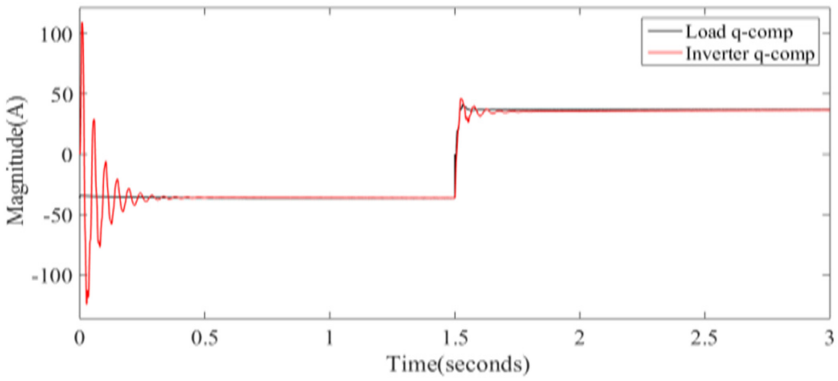

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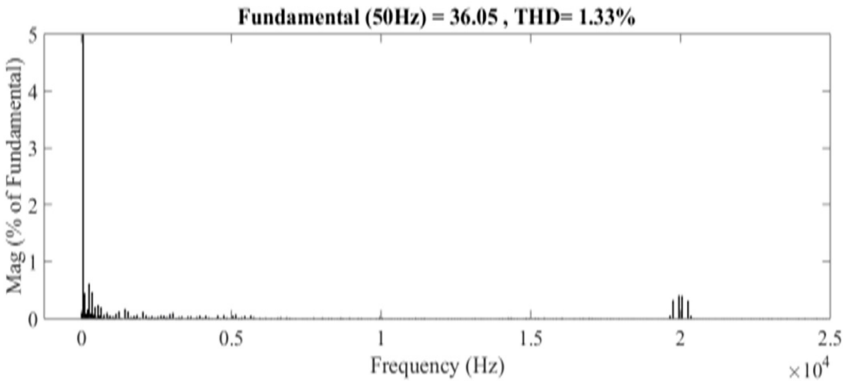

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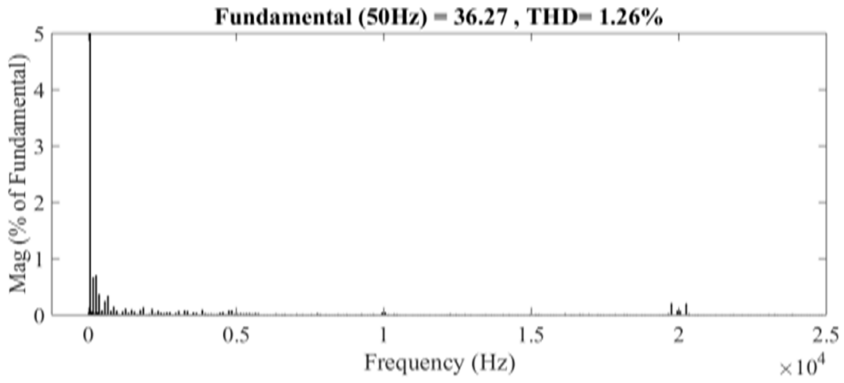
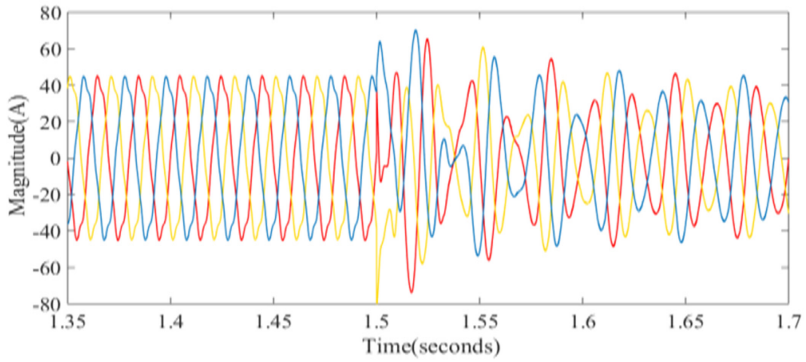


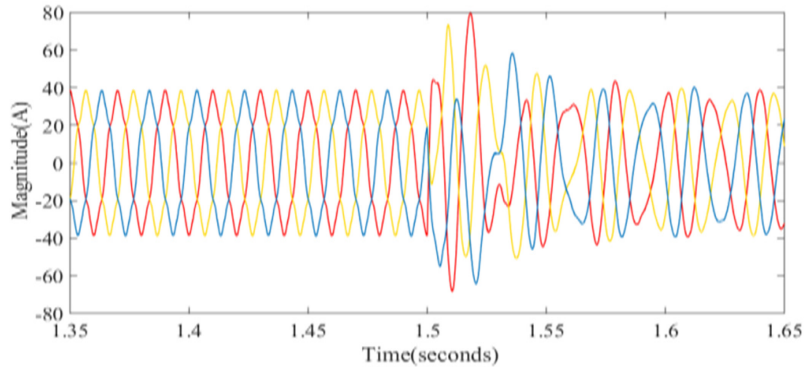
(f)

Figure 5: STATCOM response for variation of load from RL to RC at 1.5 sec with Sinusoidal Phase Shifted Carrier PWM: (a) Source Currents, (b) Inverter Currents, (c) DC Link Voltage, (d) Comparison of load and inverter *q*-components of Currents, (e) Current Harmonic spectrum of Inverter for RL load, (f) Current Harmonic spectrum of Inverter for RC load

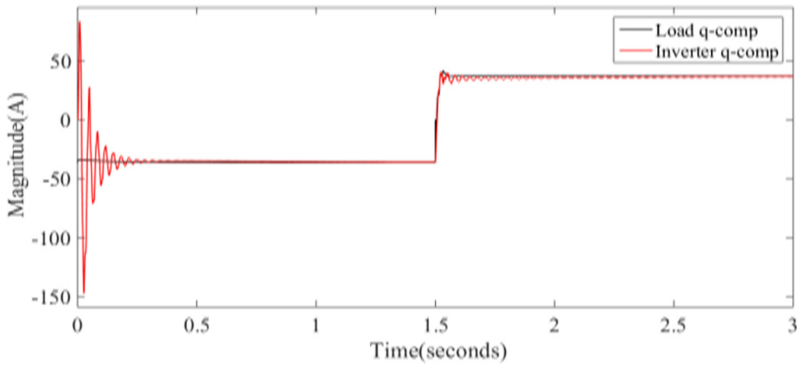
Figure 6 shows the response of STATCOM for various performance parameters such as source current, inverter current, DC link voltage, Reactive components of load, inverter currents and Harmonic analysis of Inverter output current for the variation of load from RL to RC at 1.5 sec with Third Harmonic Injected Phase Shifted Carrier PWM technique. It is observed that the STATCOM works perfectly to a low reference DC link voltage of 900 V, this voltage is equally distributed among all the DC link capacitors and it is balanced for all types of load changes. During the change of load the variation in source and inverter currents are less but the harmonics in inverter current are high with respect to SPSC technique.


Magnitude(A)
Time(seconds)

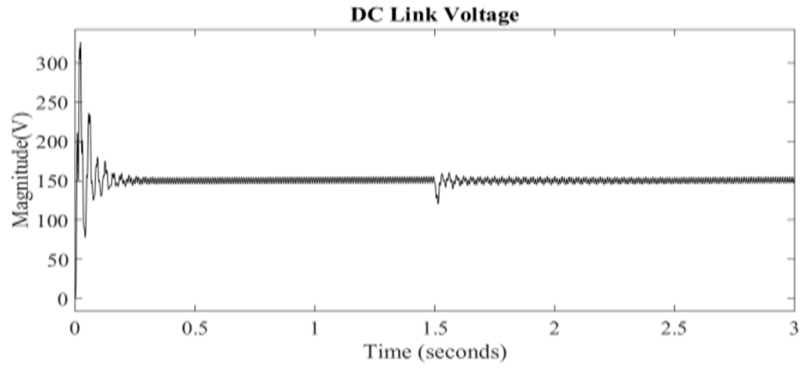
(a)


Magnitude(A)
Time(seconds)

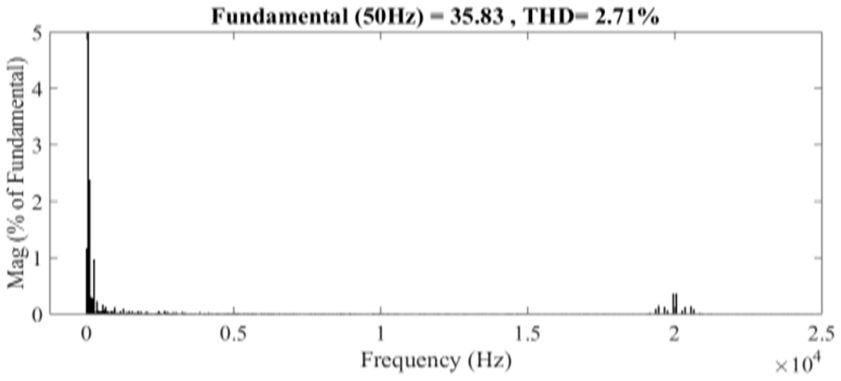
(b)


Load q-comp
Inverter q-comp
Magnitude(A)
Time(seconds)

(c)


DC Link Voltage
Magnitude(V)
Time (seconds)

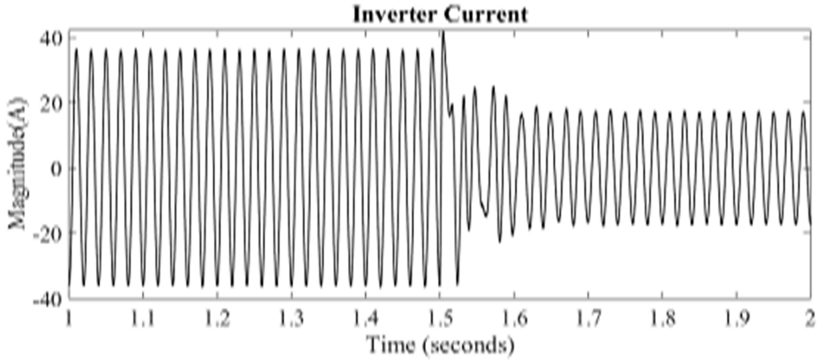
(d)



(e)

Figure 6: STATCOM response for variation of load from RL to RC at 1.5 Sec with Third Harmonic Injected Phase Shifted Carrier PWM: (a) Source Currents, (b) Inverter Currents, (c) DC Link Voltage, (d) Comparison of load and inverter *q*-components of Currents, (e) Current Harmonic spectrum of Inverter

Figure 7 shows the response of STATCOM for the change of load from full RL to half RL at 1.5 sec with Sinusoidal Phase Shifted Carrier PWM technique. It is observed that STATCOM works perfectly if the load is changed from full RL to half RL and the harmonics present in the inverter output current are very low these are 1.33% for full load and 1.86 % for half load. Figure 9 shows the inverter output line voltage for all the control techniques. The numbers of levels in the line voltage are $2m - 1$, where m is number of levels in phase voltage. Here the numbers of levels in line voltage are nine for a five level phase voltage inverter.



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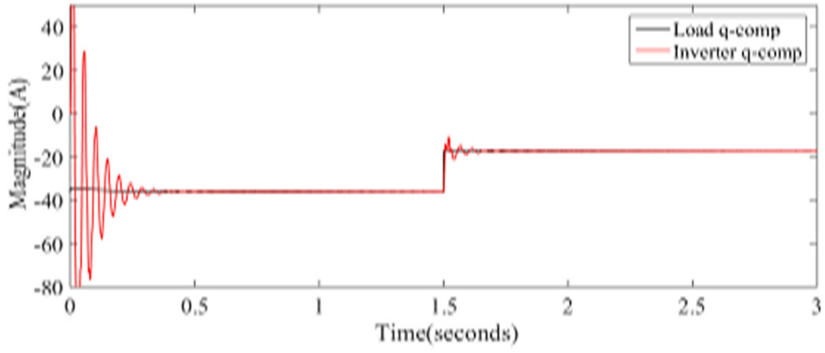
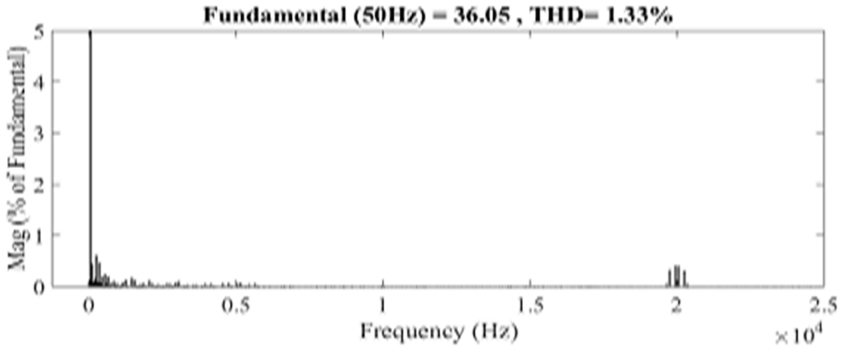


(b)



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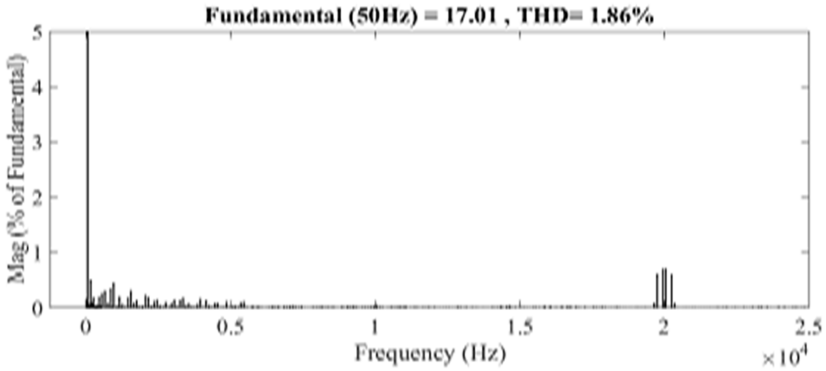

(d)

Figure 7: STATCOM response for variation of load from RL to half of RL at 1.5 sec with Sinusoidal Phase Shifted Carrier PWM: (a) Inverter Current, (b) Comparison of load and inverter *q*-components of Currents, (c) Harmonic spectrum of Inverter Current for full RL load, (d) Harmonic spectrum of Inverter Current for half RL load.

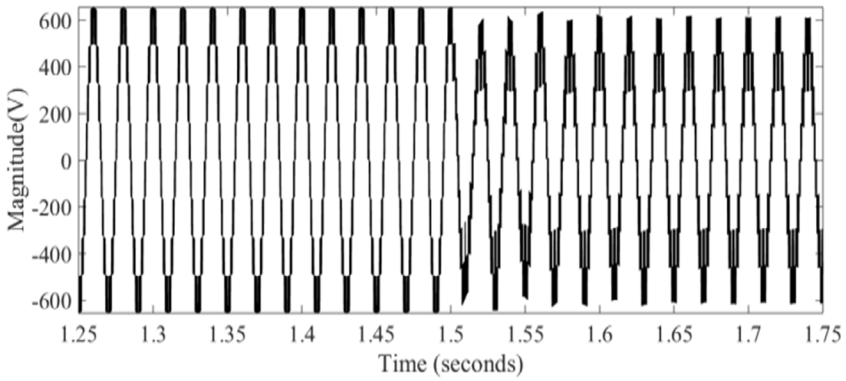

Figure 8: Inverter output line voltage

6. CONCLUSION

The appropriate topology for reactive power compensation in STATCOM is cascaded H-bridge multilevel inverter. This paper presents two novel control strategies for inverter to supply reactive power requirements for load and DC link voltage balancing. By these control strategies, the dc-link voltage of the inverter is controlled at their respective values when the STATCOM mode is converted from inductive to capacitive. The DC link voltages of the inverter are kept balanced in all the conditions, and the reactive power that is produced by the STATCOM is equally distributed among all the H-bridges. In SPSCPWM control technique the harmonics in

output current of the STATCOM are very low these are around 1.26%, and the performance of the STATCOM is good for all types of load changes.

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