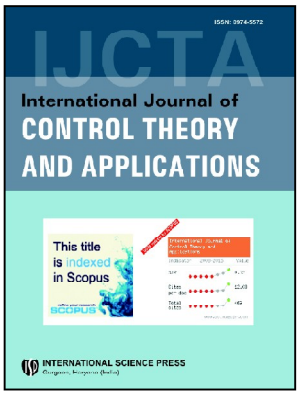

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Design of Low Power Reversible 8-Bit Adder/Subtractor Using Single Electron Transistor for Nanoprocessors

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Abstract: Digital computers perform variety of information tasks. Among the functions encountered are the various arithmetic operations. The most important arithmetic operation is the addition of binary digits. A complementing adder is a combinational circuit that performs the arithmetic operations of addition and subtraction with binary numbers depending on the control input is designed. The reversible logic, the most emerging technology is used to develop the adder and extended to the transistor level by single electron transistor for nanoprocessors, one of the low power nano devices. DKGP reversible gate can be modeled as a full adder and full subractor. Connecting 8 full adders in cascade produces a binary adder for two 8-bit numbers. The subtraction circuit is included by providing a complementing circuit to the 8-bit adder circuit constitute complementing adder. The circuit is simulated using ORCAD and the results are proven that the complementing adder using SET dissipate highly considerable low power related to the CMOS.

Index terms: Adder/Subtractor, CMOS, DKGP reversible gate, Single electron transistor

I. INTRODUCTION

The adder is a fundamental arithmetic block and plays a vital role in all arithmetic operations. It has three inputs: the addend a, the augend b and the carry-in c_i; and two outputs: the sum s and the carry-out c_o. The adder circuit is a crucial component for all other digital circuits. Power dissipation is one of the major anxiety in present day technology. Low power adder/subtractor lead to compactness in size of digital circuits and increase in execution speed which in turn efficient throughput. Reversible logic, a booming technology, offers less information loss related to the irreversible logic. Charles Bennet proposed a theoretical background which proved that reversible general purpose computing devices can be constructed [1][2]. It provides a way to construct reversible logic circuits. Logical reversibility means that after completion of a computation, it is possible to retrace every step and reconstruct data which was used in every step. Thus, reversible logic circuits offer an another possibility that allows computation with very small energy dissipation. In this paper, the 8-bit adder/subtractor block is developed on reversible logic, that is, to the gate level, it is technologically advanced to the transistor level by using one of

the low power and high speed nanodevices known as single electron transistor(SET) and simulated using ORCAD. The comparison on power dissipation has been done between reversible 8-bit adder/subtractor using SET and conventional CMOS.

II. SINGLE ELECTRON TRANSISTOR

The elementary device in which the effect of Coulomb blockade can be realized is the so-called single-electron transistor. It consists of two electrodes called as drain and the source, connected through tunnel junctions to one common electrode with a low self-capacitance, called as the island. The electrical potential of the island can be tuned by a third electrode, known as the gate, which is capacitively coupled to the island[7].

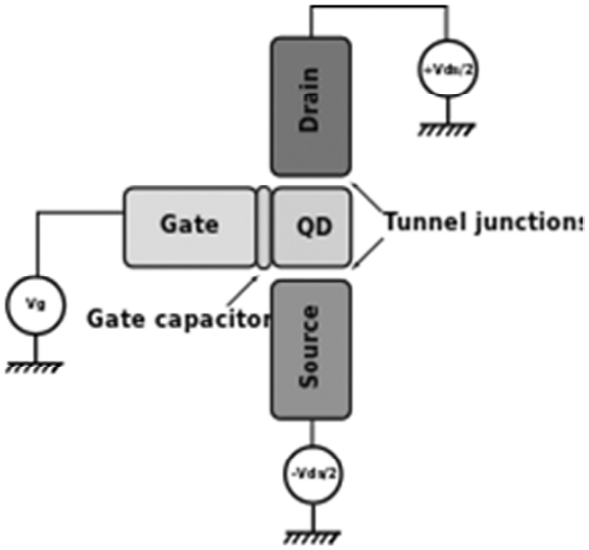

Figure 1: Construction of SET

SET operating at the quantum/nanoscale that have switching properties are controlled by the removal or injection of a single electron; a device through which only one electron can be transferred at a time. One of the most interesting challenges of microelectronics is the vision of realizing a switching device that can be controlled by single electrons[4]. This had been realized by using the concept of coulomb blockade and electron tunneling that used to develop Single Electron Transistors (SET) . At temperatures below 1 K, current cannot pass through the island with low bias voltage. This effect is known as the Coulomb blockade, due to the repulsive electron–electron interactions on the island. Coulomb blockade is the repelling energy of previous electron present in the island to the next electron coming towards the island[3]. The concept of Coulomb blockade talks about the phenomenon that tunneling through an island may be inhibited at low temperatures and small applied voltages. The reason is that the addition of a single electron to such a system requires an electrostatic charging energy. Since power consumption is proportional to number of electrons transferred across the junction, it consumes less power [3].

III. A REVERSIBLE DKGP GATE

Many reversible gates are available which have been analyzed for various applications if digital circuits[8-11]. A 4* 4 reversible DKGP gate can work as a reversible Full adder and a reversible Full subtractor. It consists of four inputs and four outputs. The implementation of full adder and full subtractor from DKGP gate is shown in Figure-3 and 4, respectively. If the input A=0, the proposed gate performs as a reversible Full adder and if the input A=1, then it performs as a reversible Full subtractor [5]. There are low power compressors using DKGP gate in order to reduce partial product addition is designed [6].

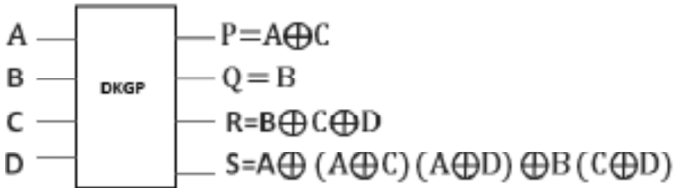

Figure 2: A DKGP gate

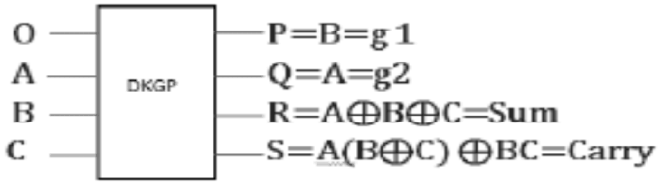

Figure 3: DKGP gate as a full adder

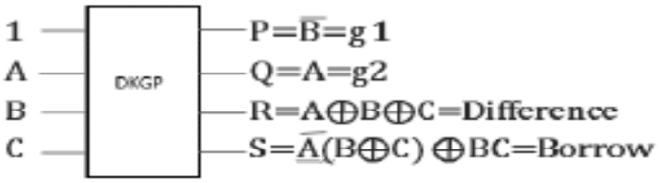

Figure 4: DKGP gate as a full subtractor

A. CMOS implementation of a full adder using DKGP gate:

The reversible full adder using DKGP gate has been implemented in CMOS.

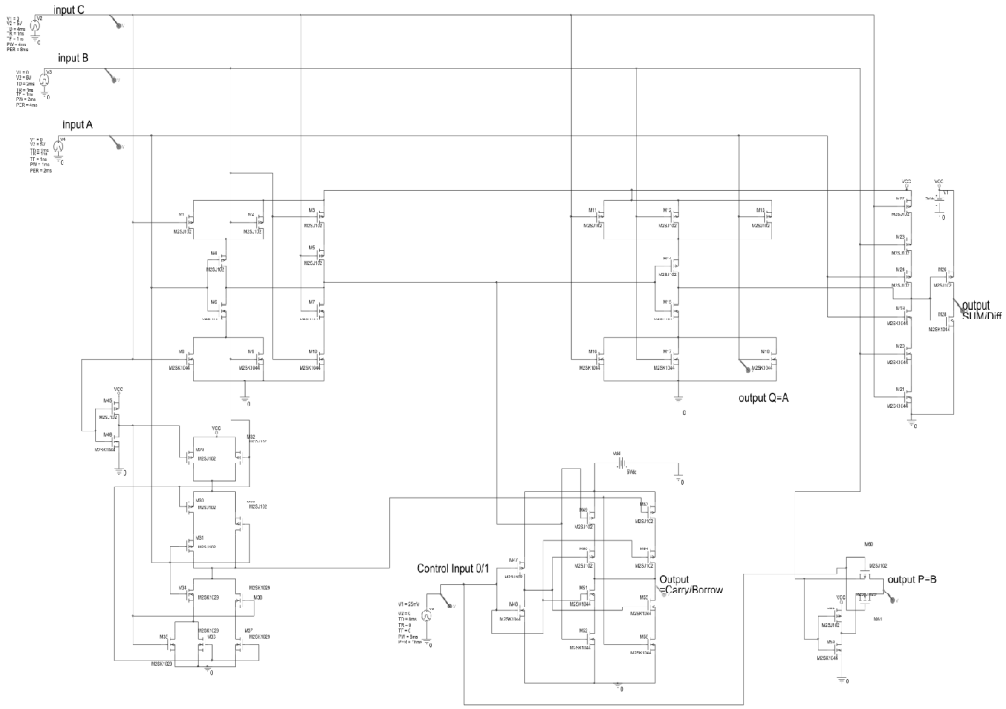

Figure 5: CMOS implementation of DKGP gate

B. SET implementation of a full adder DKGP gate:

The reversible full adder using DKGP gate has been implemented in SET.

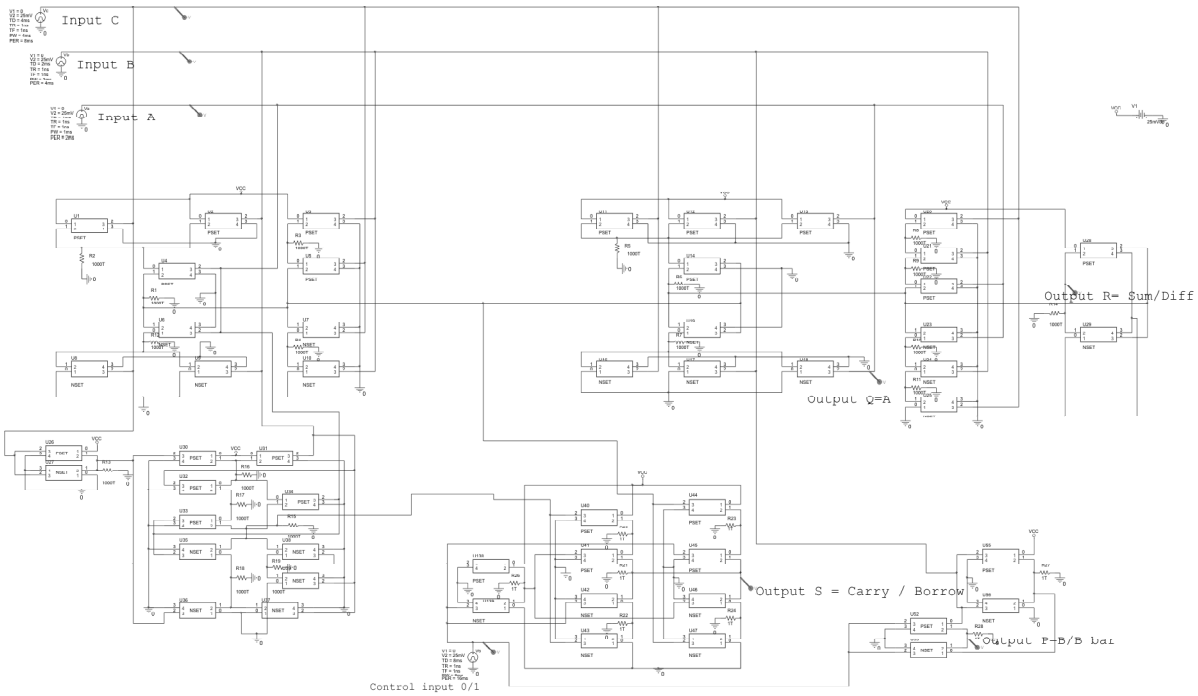

Figure 6: SET implementation of DKGP gate

IV. REVERSIBLE 8-BIT COMPLEMENTING ADDER IN CMOS AND SET

There are several adder circuits have been constructed for low power digital circuit design[12-16]. The 8-bit complementing adder can work as both adder and subtractor depending on the control input. It consists of eight full adders which are connected together to form a 8-bit reversible adder/subtractor block.It has two 8-bit input, that is, A1-A8 and B1-B8 and one control input , 0 or 1.the outputs are sum, S1-S8 and carry out, S9. This adder/ subtractor block constructed from full adder using DKGP gate so called reversible 8-bit adder/subtractor. Then the 8-bit reversible adder/subtractor are implemented in transistor level using CMOS and SET.

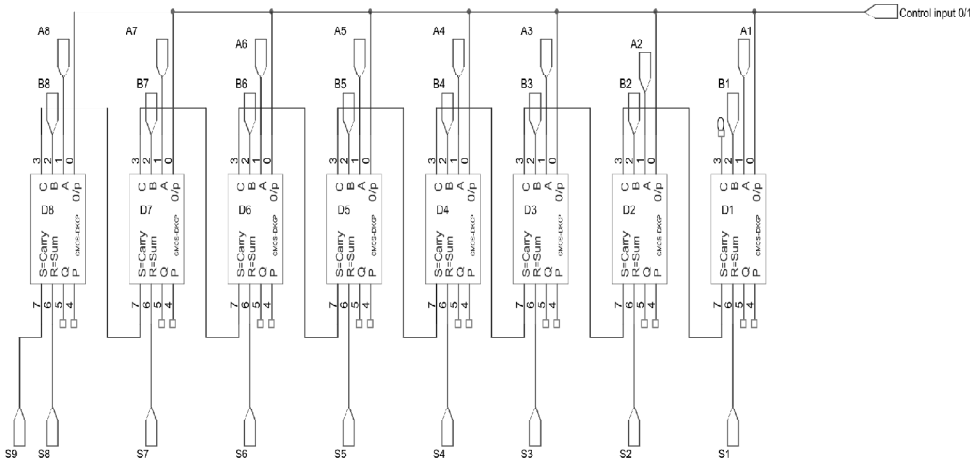

Figure 7: A 8-bit reversible adder/subtractor using CMOS

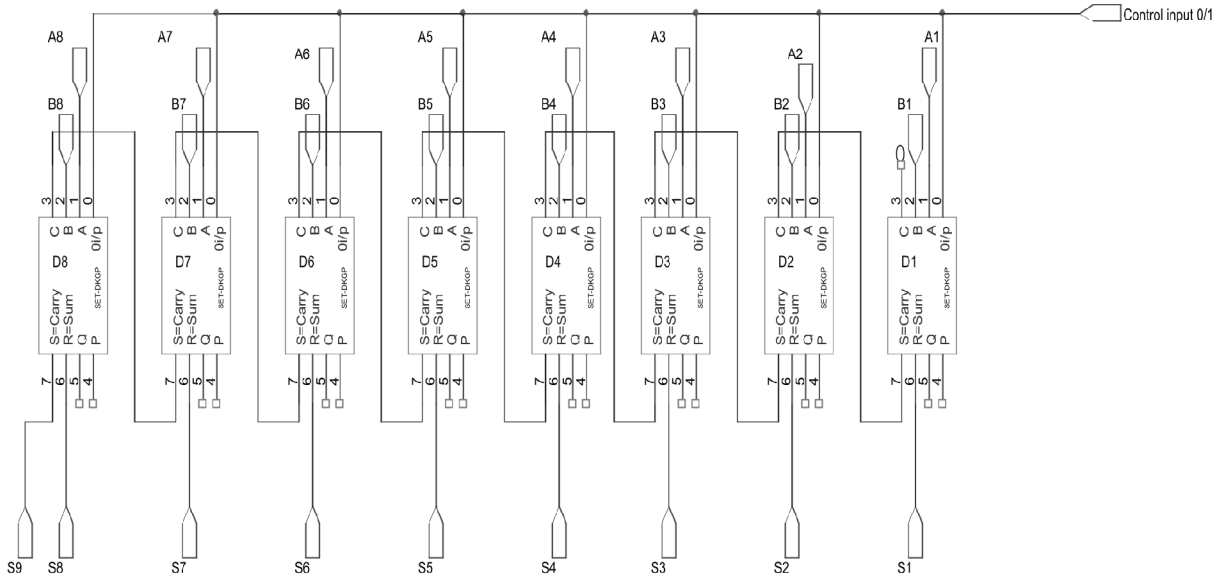

Figure 8: A 8-bit reversible adder/subtractor using SET

V. SIMULATION RESULTS

The reversible 8-bit adder/subtractor using CMOS and SET has been simulated using ORCAD tool and the results are obtained which proved that the 8-bit adder/subtractor using SET dissipates remarkably less power distinguished from conventional CMOS. This low power reversible 8-bit adder/subtractor block can be used in nano ALU for forthcoming high speed processors.

Table 1
Comparison of Power Dissipation Between Cmos and Set

	Power dissipation	
	CMOS	*SET*
Reversible 8-bit adder/subtractor	8.03 mW	0.0826pW

VI. CONCLUSION

The results proved that one of the low power nano devices, the single electron transistor(SET) dissipates remarkably less power compared to the conventional CMOS which in turn achieved power savings. Anyhow, the practical implementation of SET requires parameter dispersion considerations and fabricated-related analysis. Reversible logic helps to retrace the inputs from the destination nodes. The use of reversibility can be applied in testing of VLSI/NANO circuits. In summary, the low power 8-bit adder/subtractor block has potential application toward future digital circuit implementation and it is promising in future nanoscale information processors

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