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Comparison of various techniques used to obtain optimal floorplan and their impact on quality of results

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ABSTRACT

In this paper, we addressed the various technique designers follow to design the floorplan. The number of transistors are on a rise (Moore's law) and metal scaling is poor. High density of transistors demand high routing resources. Over congested design can affect the performance and even lead to high numbers of shorts and open or to unrouteable situation. Therefore one has to redesign and start from beginning. To avoid such condition and lower the design time cost, one needs to take precaution from beginning and has to select right tactic with respect to congestion and routing resources. This experiment shows comparison between the three methodologies used by designer to reach to optimal design

Keywords: ASIC Application specific integrated circuit ,QOR quality of result ,TAT Turn around time,WNS worst negative slack, physical design,Congestion

1. INTRODUCTION

In present scenario for the case of high performance circuit with the ASIC methodology, by taking into the account of Moore's law as the stepping stone is highly complex. In physical design flow, floorplan laid down the foundation of chip and is one of the most important step for achieving high quality layout Quality of result (QOR) of design intensively dependent on floorplan. Floor planning is iterative and time consuming step. One cannot ignore its importance, as designer invest most of his time in exhaustive iteration to obtain the optimum design results. Designer constantly monitors the congestion, worst negative slack, utilization of chip after each iteration

2. BASICS OF FLOORPLAN

Core boundary: An optimum floorplan gives a good result in terms of area, congestion, timing, power. The floorplan stage defines the shape and size of the chip or Block .Mainly top level design have square or rectangular shape but block level design can also be rectilinear in shape .Boundary refers to the area of the chip whereas the core boundary refers to the area where standard cells and IPs/Macros are placed. Power resources can be routed outside the core area. In case of top levels IO pads and IO buffers can be placed outside the core area.

Aspect ratio: defines the ratio between height and width of the chip which determines the shape of the chip /block. Aspect ratio of 1 gives the square shape of the chip. Mainly die boundary and core boundary are defined in top level constraints.

*Core Utilization***:** is the ratio of [standard cells area + hard macro area]/ total core area

*I/O placement or Pin placement***:** For interaction of chip with outer world, the I/O pads In case of top chip and the pins/ports in case of block are placed along the side of chips. Along with each I/O pad or Pin

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buffers are placed so as to improve the strength of the signal coming from or going back to the outer world. Def file contains all the information about the position of the pins. Along with buffer cells Decap cells are also used to compensate the IR drop through nets. One can use tool or TCL script to place pins for design

Macro placement: Macro placement is one of crucial step in floor planning .Depending upon the position of the macros, the standard cells are placed in the core. If two macros have interaction between their logics, one should try to keep those two macros nearer to each other. It is advised to use placement blockages where two macros are very close to each other to avoid the tool to place standard cells between those macros so as the congestion should be avoided in that particular region . If placement blockage is not used then it should be made sure that one VDD and one VSS strap should pass through the macros , so as to provide power between the two macros .

Different types of blockages which can be used to avoid tool to place the cells in desired location are

- Standard cell blockages: It doesn't allow tool to place standard cells in the desired area where these blockages are implemented.
- Non buffer blockages: The tool allows only buffers to place in the desired area where these blockages are set true.
- Blockages under Power lines: It is advised to put blockages below power straps to avoid the congestion issue in the particular area .If there is specific area in the design which contributes large no of DRCs then, it is advised to put Blockages in that area to avoid the congestion which can lead to the DRCs

During the placement of the Macros one should follow the basic Macro placement rules like Flylines should be used to check the connectivity of Macros with rest of macros ,standard cells and Ports, Try to place cells nearer to each other which are interacting .Always consider the power and ground straps while placing macros. It can help in clubbing the macros. Create a separate power mesh for Macros to avoid IR drop. Refraining placement of Macros in front of I/O pad to avoid detouring of net. Try to place macros in continuous manner to get contiguous core area

- Space between two macros can be calculated using

  {(no of pins * pitch) +space}/ number of metal layers in horizontal or vertical direction

Orientation of macros can be done to minimize the distance between the pins of macros. Place the macros around chip periphery and try to avoid placement of macros in center of chip

Inputs for floor planning stage:

- Synthesized netlist (.v)
- Logical and physical libraries
- TLU+ files
- Design constraints (SDC)
- Technology file (.tf)

Outputs from Floor planning stage:

- Macro placement
- Standard cells area
- DEF file
- I/O pad or port placement

*Design specification***:** The design consists of 80 macros .The challenge with design was that macros of different size and shape along with some macros consist of pins more than 500 pins .the die size is 400 *2000 micron square with operating frequency of 450 MHz . 2248 no of ports were there along with 0.5 million standard cells in the design.

3. TRADITIONAL APPROACH

Start floorplanning with setting the placement strategies and use placement commands to place macros in the desired location in design .Several iterations are required for macros placement to optimize and achieve optimal design

Initialize the floorplanning with traditional strategy shown in flow diagram. In this approach to analyze the connectivity on the base of flylines and net connectivity and arrived to floorplan shown in figure 2.

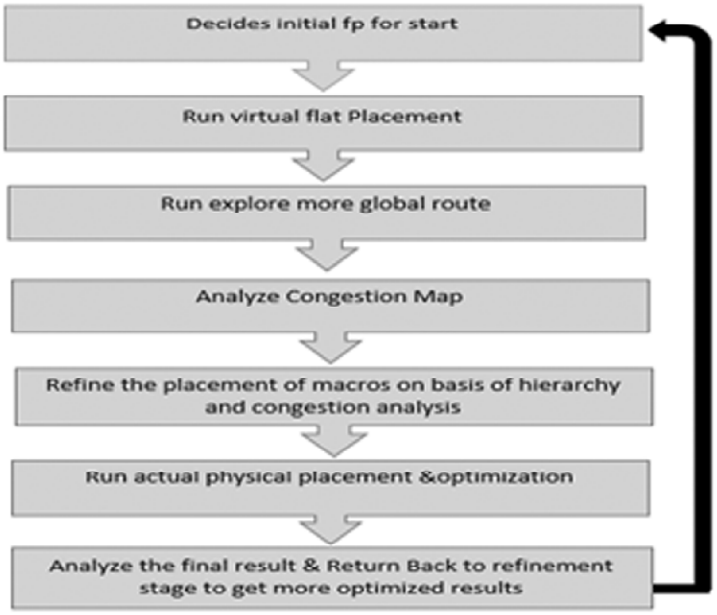


Figure 1: Traditional flow diagram for floorplan

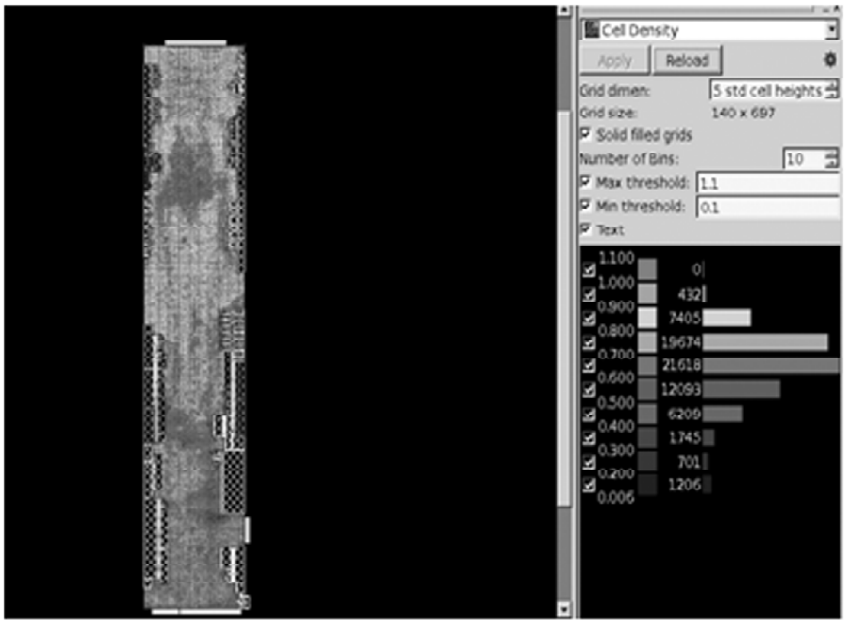


Figure 2: 1st Experiment cell density map

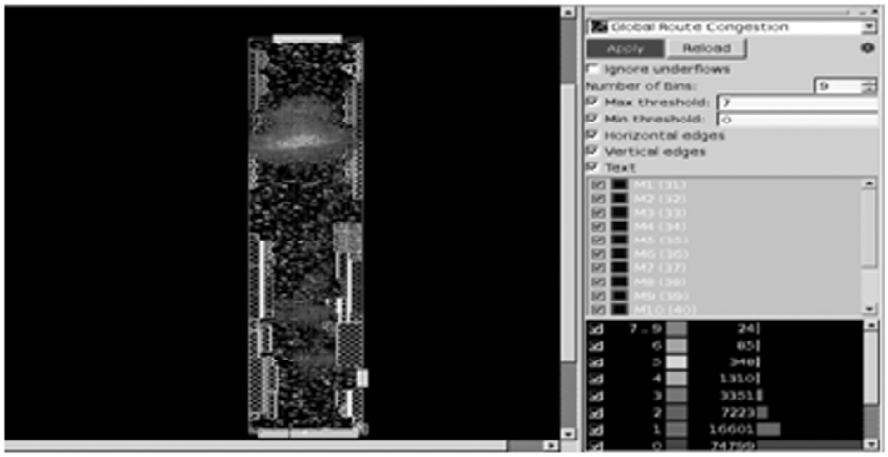


Figure 3: 1st Experiments congestion map

The results of this experiment has very high congestion in the design as shown in figure 3.

In detailed analyses of 1st experiment

WNS: 0.33 TNS: 192.48

Congestion: 2.25 % Utilization: 63.10%

Highly congested design results in higher number of DRC violation and also results in large numbers of shorts and open. Under the same scenario the routing net will also detoured and will affect the timing. Therefore to avoid this condition one needs to use the other way of designing.

4. USING PLAN GROUP

In 2nd approach, strategy used plan groups, which groups the macros of same hierarchy and also can subdivide the bigger hierarchies. This approach provided detailed analysis about hierarchy and their standard cells also this approach helps us to determine the hierarchy as how they are connecting with other hierarchies. This strategy lead us to the lower congestion and symmetrical design with reduced wire length.

The floorplan shown in figure is less congested than the previous approach and it also has better timing behavior.

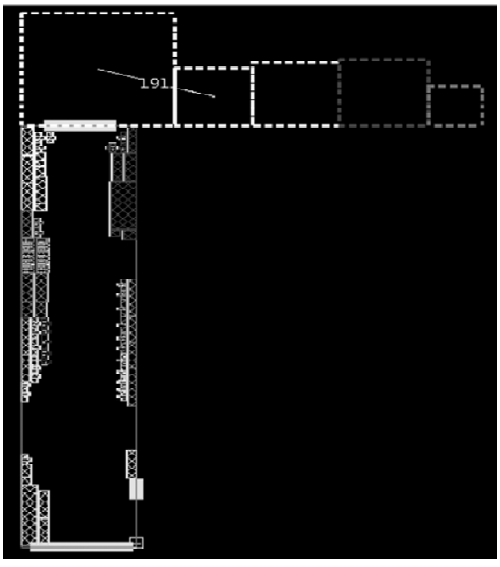


Figure 4: Plan groups of different hierarchies

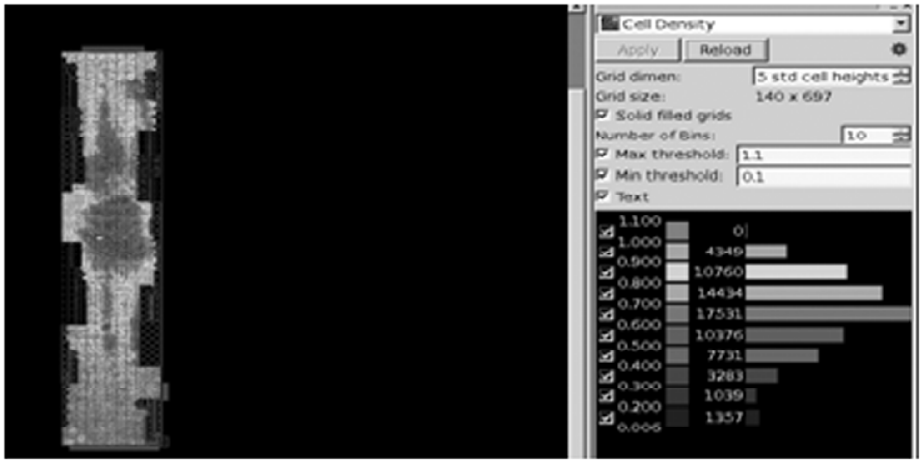


Figure 5: 2nd Experiment Cell density Map

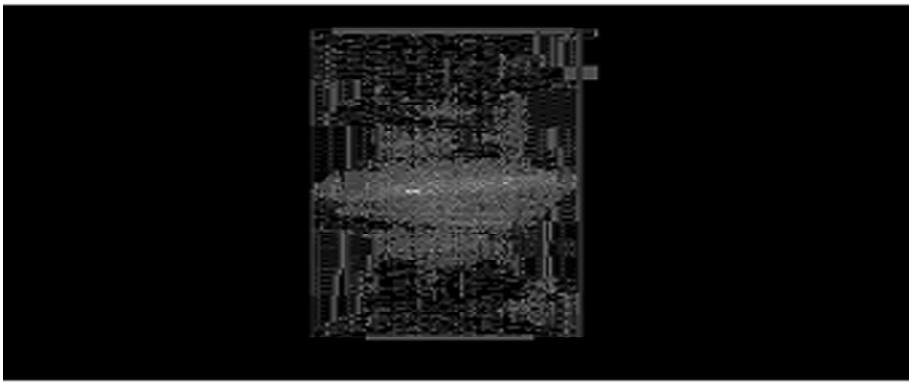


Figure 6: 2nd experiments Congestion map

The results are better in terms of congestion and WNS from the previous ones

WNS: 0.19 Congestion: 1.25 %

5. USING DFA

In 3rd approach to reach the optimal floorplan we use DFA Data flow analysis. This approach helps us to reduce the work load and work hours. DFA is very handy tool in Macros intensive Designs. DFA consists of automatic placement properties to create_fp_placement command and also provides analysis results. Along with the capability to edit the existing plan, it also helps us to decides, one is the optimum place for different elements of the plan

With the help of GUI, the physical designer can apprehend the data flow analysis very easily. DFA consists, some very prominent tools which helps us to understand interaction between different hierarchies . Array editing tool and Advance macros to macros and macros to I/O flyline analyzer helps to achieve the accurate results

One can analyze the macros to macros and macros to I/O connectivity to Higher levels of abstraction and can deep dive to come to Optimal scenario .pink flylines indicate the macros to macros connection, white flylines shows the standard connection, path and strength of connection and yellow flylines indicates the connectivity with the I/O ports DFA allows users to split the big hierarchies into sub hierarchies and can also split sub hierarchies into their child hierarchy's .This splitting of hierarchies helps to analyze the design and mainly focus on main hierarchies. Cell density of floorplan attained by DFA tool is shown in figure 8.

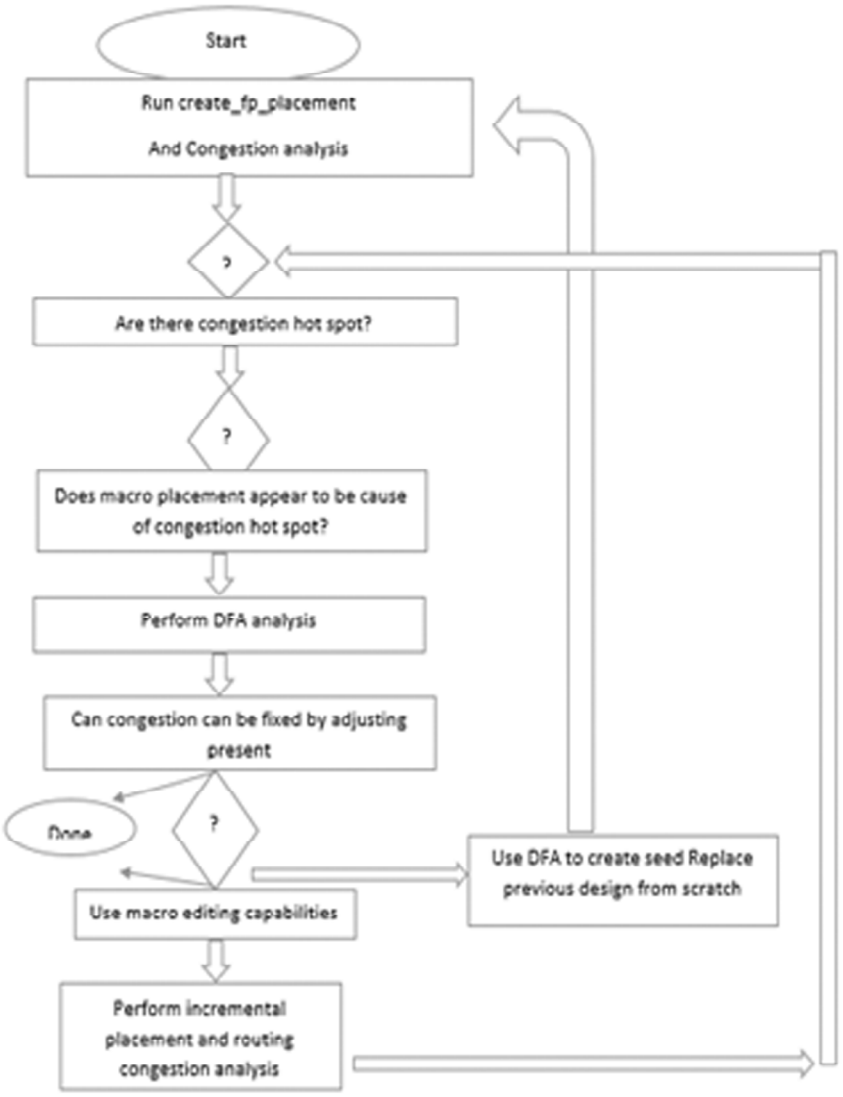


Figure 7: DFA flow diagram

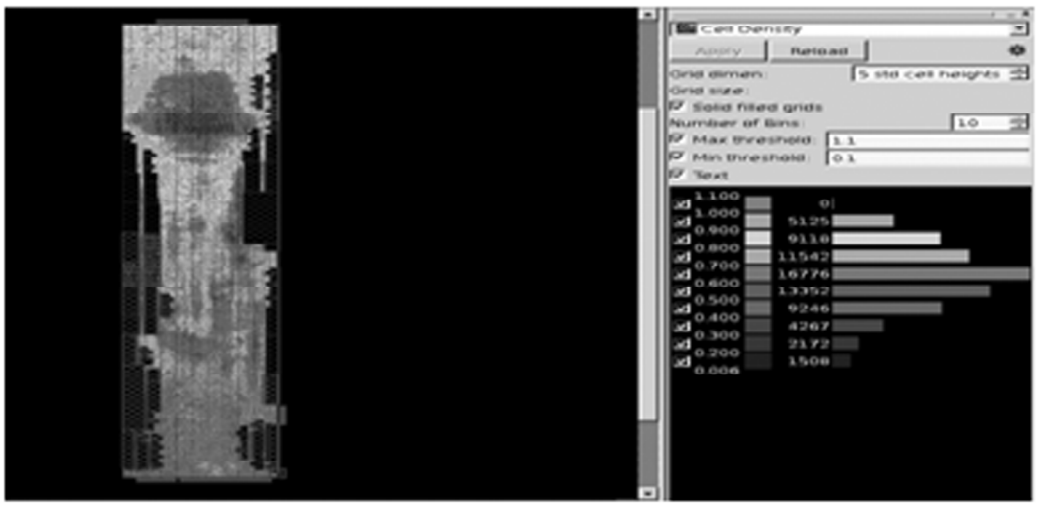


Figure 8: 3rd Experiment Cell density map

The DFA tool resulted in floor plan which is the best in all other approaches with good WNS and congestion results:

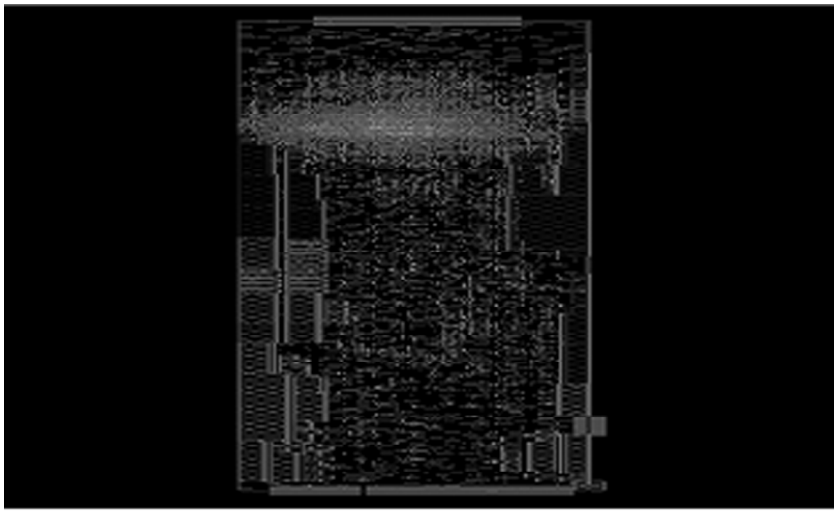


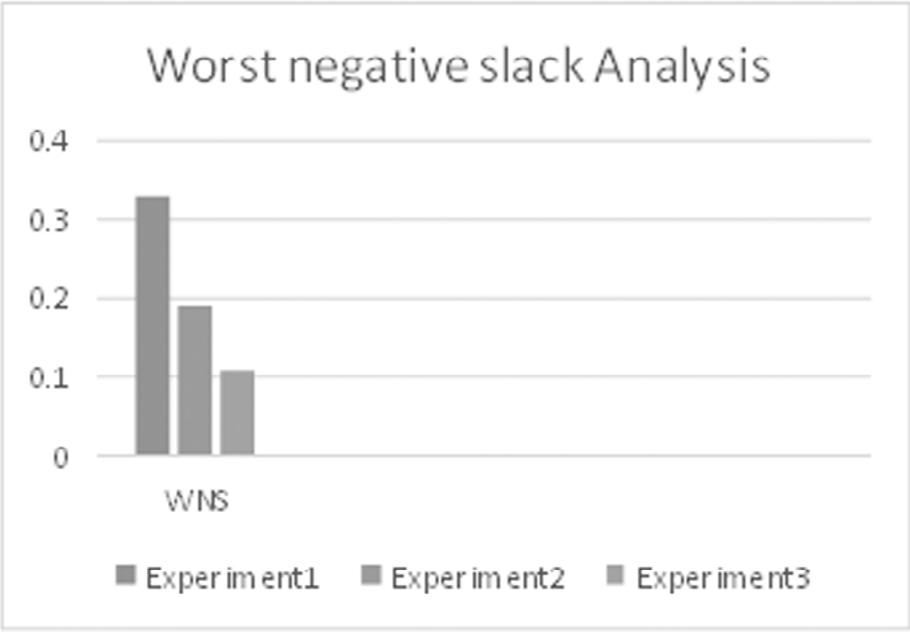
Figure 9: 3rd Experiment congestion map

6. RESULT AND CONCLUSION

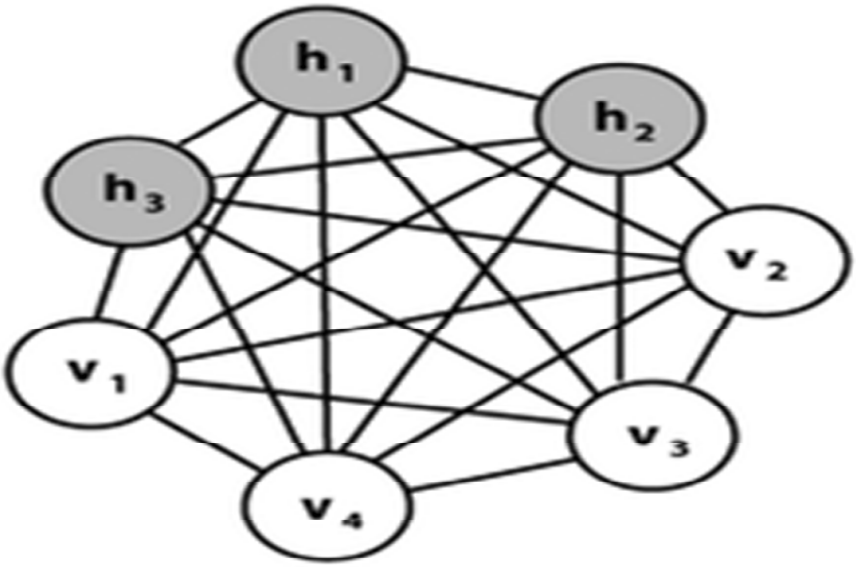
On comparative analysis of all approaches, controlling factors like WNS, congestion and TNS decides floorplan is to carry to further steps or it needs modification in current design. Here in 1st approach our strategy was to just place macros randomly resulting higher WNS and congestion number. Therefore to improve the quality further to improve the quality of result, in 2nd strategy we have grouped the hierarchies by using ICC hierarchy browser and identified the high level connection and hierarchy's size, number of

Table 1
Results of Experiments

Experiment	*WNS*	*CONGESTION*	*Std. cell utilization*
Expr1	.33ns	2.25%	63.10%
Expr2	.19ns	1.25%	64.34%
Expr3	.11ns	1.19%	63.78%



Graph 10: Variation in WNS with Different strategy



Graph 11: Variation in Congestion with different Strategy

standard cells of different hierarchy and most importantly , how different hierarchies are interacting with each other. The numbers were motivating, we achieved more organized design with less congestion but WNS was still a cause of worry as no improvement is seen .Wire length was still long ,buffer chains were getting inserted in input and output paths.To further optimize the design our 3rd approach i.e. DFA (data flow analysis) resolved the problem of interaction of macros with input ports and output ports DFA tool's analysis and editing the design helped in getting the best possible location for macros and it has resulted in no hierarchical split which further reduced the wire length and WNS and it finally resulted in the congestion.

Above experiment has been conducted using the different strategy, one can improve quality of results and turnaround time of chip using DFA tool.

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