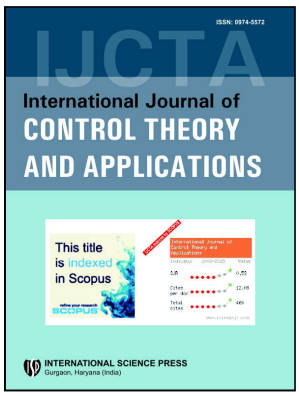

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Design of Low Power Amplifier for Neural Recording Applications using Inversion Coefficient Methodology

Bellamkonda Saidulu[1] and Arun Manoharan[2]

[1] *School of Electronics Engineering VIT University, Vellore, Tamilnadu, India, Email- bellamkonda.saidulu@gmail.com*
[2] *School of Electronics Engineering VIT University, Vellore, Tamilnadu, India,* Email- arunm@vit.ac.in

Abstract: Preamplifier block is the preliminary stage of Analog Front-End (AFE) design in implantable neural recoding system. Preamplifier is the crucial block, which determines the overall performance of the neural recording system. The key design parameters of neural recording system are high gain, submicron level power and noise. The challenge for the analog design engineers is to design an optimized preamplifier to integrate large number of front-end amplifiers on a single on-chip. This work, focuses on design of optimized power and noise preamplifier using a sizing methodology to meet the demands and also for IoT based neural recording system. We proposed an Inversion Coefficient (IC) methodology for single stage Telescopic OTA with improved current mirror structure. This methodology helps in sizing the MOSFETs to prove low power and low noise designs. The simulation results are carried out for power, noise, gain with V_{DD} of 1.5V, TSMC 180 nm Technology in Cadence environment. The Results show the gain is 78 dB, Input referred noise 640nv/sqrt(Hz), 1.44 µW power consumption without degradation in stability.

Keywords: Low noise amplifier (LNA), Neural recording system, Subthreshold, Telescopic Cascode, NEF, Saturation, Inversion Coefficient (IC).

1. INTRODUCTION

At present, the doctors and clinicians aspire for cutting-edge smart health monitoring system for an accurate diagnosis. Fully implantable neural recording systems require low power, low noise with smaller area [1]. A neural amplifier is one of the most important components of implantable neural recording system which amplifies the micro level neural signals more than a hundred times in amplitude. Neural signals have amplitude of 5µ-500µV with a background noise level of 5µ-10µV. For this requirement, neural amplifiers should possess high gain ($100*V_{in}$), low power and low noise operation. Power and noise are key parameters, which determine the Figure-of-merit of the neural amplifier. The various classifications of neural signals based on different signal bandwidth ranges are supposed to record the signals for diagnosis for different diseases with different gains which lead to more power consumption [2]. Low power dissipation is a common constraint to all portable designs and should be in compliance with energy harvesting techniques. This could be possible with low bias currents and supply voltage with optimized sizing of each MOSFET. State-of-the art neural amplifiers have

reached at nano range input referred noise and micro level power consumption. L.Liu [3] reported a neural amplifier with current reuse technique for low input referred noise and high current efficiency for improving the power dissipation of 800nw and an input referred noise of 5.71μV_{rms}. Zhang [4] reported a closed loop complimentary input amplifier which has noise of 3.2 μV_{rms} and the cost of 12μW power consumption with 1V supply. Kim. Jungsuk [5] reported an ultra low power neural amplifier with capacitive feedback topology. This work used a single path amplifier to get benefit of low power consumption and achieved 220nW power consumption and14.5μV_{rms} was input referred noise. These works reveal a trade-off between noise and power along with better performance in individual design parameters. V. Majidzadeh [6], presented a neural amplifier with partial shared structure in multi electrode array. The objective of work was low power, area efficiency and improved NEF with acceptable input referred noise. They achieved with the results of 7.92 μW power consumption, NEF 3.35 and input referred noise 3.5 μV_{rms}. Recent work [7] reported with low power, low noise with g_m/I_D design methodology and achieved results of 3.2 μV_{rms}, 1.92 μW input referred noise and power consumption respectively with V_{DD} of 1V. Yang-Guo [8] presented in his work about low power and low noise bio-amplifier. He also designed a circuit with sub-threshold and self-biased technique and achieved 720nW power consumption and 4.3 μV_{rms}, with 1.8V. In this study, we have proposed a single stage Telescopic OTA with Inversion Coefficient Methodology.

This paper is organized, as follows section I describes the challenges and the issues of neural amplifier design. Section II describes the proposed methodology for OTA design. Section III describes the analysis and the results. Section IV provides the conclusion.

2. INVERSION COEFFICIENT (IC) METHODOLOGY

The rapid development in this application has resulted in an increase with respect to area, complexity and consumption of the power in analog circuit designs fabricated in CMOS IC Technology. Analog CMOS design system requires specifications and various topologies with the interconnection of MOS transistors. The Analog designer should be aware of selection of drain current, channel width and length for every MOS Device in a circuit. Inversion Coefficient (IC) is a method which provides a numerical measure of MOS inversion level. If inversion coefficient value is less than 0.1, it is a weak inversion. If the value is between 0.1 and 10, it corresponds to moderate inversion. If the value is above 10, it corresponds to a strong inversion [9]. The selection of MOS drain current, inversion coefficient and channel length are desired tradeoffs lead to optimized design.

$$IC = \frac{I_D}{I_{DSspec} \cdot \frac{W}{L}} \tag{1}$$

2.1. MOS in Weak Inversion (WI)

Weak inversion happens when MOSFETs are operating at low effective gate-source voltages ($V_{eff} = V_{gs}-V_{th} < -72mV$). Gate-source voltage V_{gs} should be less than the threshold voltage (V_{th}) at least by 72mV for bulk CMOS process at 300K. In weak inversion, channel formation is very weak and current dominates with diffusion process. MOS which operates in weak inversion, drain current and Transconductance is proportional to the exponential of gate-source voltage. Drain current in MOS for EKV model is given by

$$I_D = 2n\mu C_{ox} U_T^2 (W/L)\left(e^{\frac{Vgs-V_T}{nU_T}}\right) \tag{2}$$

W, L are the effective channel width, length.

μ is the Channel carrier mobility.

C_{ox} is the gate oxide capacitance per unit area.

I_D is given for MOS saturation when $V_{DS} > V_{DS,\ sat}$. In weak inversion,

$V_{DS,sat}$ is approximately $4U_T$ (U_T=26mV) i.e. 104mV.

Subthreshold factor n, existed in equation (2) EKV and other MOS models. 'n' represents a loss of coupling efficiency between gate and channel. It relates to capacitive voltage division between gate voltage and silicon surface potential resulting from gate oxide, depletion and interface capacitances. Subthreshold factor, n in weak inversion is approximately 1.4-1.5 for bulk, given by

$$n \approx 1 + \frac{C_{dep}}{C_{ox}} \tag{3}$$

and also slope factor n is a function of the gate voltage(Vg) given by

$$n(Vg) = 1 + \frac{g_{mb}}{g_m} \tag{4}$$

MOS Transconductance in weak inversion is given by

$$g_m = \frac{I_D}{nU_T} \tag{5}$$

Transconductance efficiency, g_m/I_D in weak inversion is given by

$$\frac{g_m}{I_D} = \frac{1}{nU_T} \tag{6}$$

From equation (4), (5) MOS Transconductance is equal to product of Transconductance Efficiency and drain current is given by

$$g_m = \left(\frac{g_m}{I_D}\right).I_D \tag{7}$$

In weak inversion, Transconductance and Transconductance efficiency are not dependent on MOS sizing and process parameters except Subthreshold factor. The weak inversion operation requires a large aspect ratio (W/L) and it has limitation on poor bandwidth due to large gate area (W*L) and high gate capacitances.

2.2. MOS in Strong Inversion (SI)

MOS operates in strong inversion with high effective gate voltage ($V_{EFF}=V_{gs}-V_{th}$>225mV) i.e. 225mV larger than V_{th} for typical bulk CMOS process at room temperature. The drain drift current dominates with strong channel inversion in the channel. In strong inversion drain current is proportional to the square of the effective gate-source voltage (V_{EFF}). Drain current is approximated from EKV MOS model is given by

$$I_D(SI.no.vel.sat) = \frac{1}{2}\left(\frac{\mu Cox}{n}\right)\left(\frac{W}{L}\right)(Vgs - Vth)^2 \tag{8}$$

MOS Transconductance in strong inversion is given by

$$g_m(SI.no.vel.sat) = \frac{2I_D}{V_{EFF}} \tag{9}$$

Transconductance efficiency is

$$\frac{g_m}{I_D}(SI.no.vel.sat) = \frac{2}{V_{EFF}} \tag{10}$$

g_m depends on DC biasing I_D, V_{EFF} and independent of MOS sizing and process parameters. g_m/I_D is depends only on effective gate voltage. As V_{EFF} is increases Transconductance efficiency will be reduced and drain-source voltage is increases are the disadvantages of MOS in strong inversion is shown in Fig. 1.

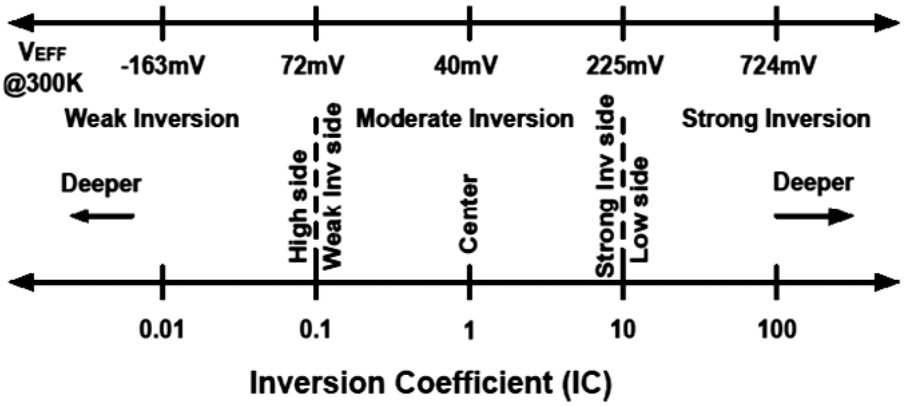

Figure 1: Inversion Coefficient (IC) versus Effective gate-source voltage (V_{EFF}) in all region of operations.

2.3. MOS in Moderate Inversion and All region of operation

MOSFET has two physical regions of operations i.e. weak and strong inversion is shown in Figure 2. There is a transition region called Moderate Inversion (MI) between these regions with significance of diffusion and drift

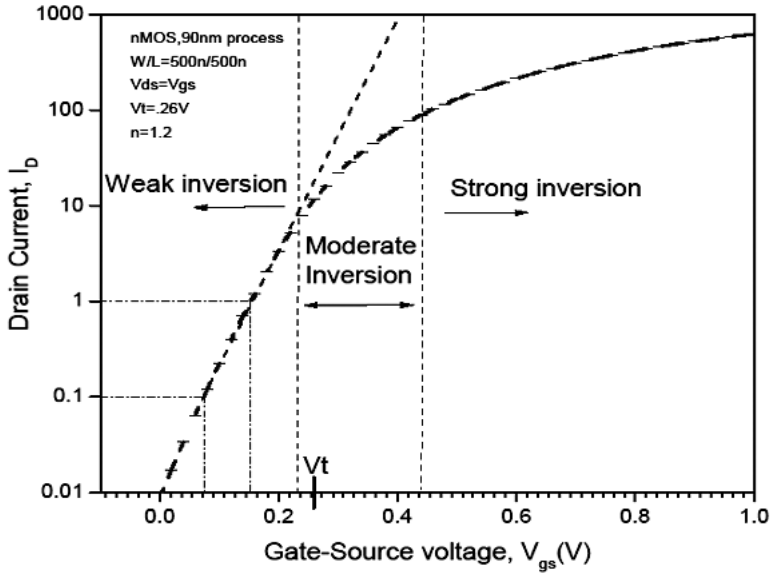

Figure 2: Drain current versus gate-source voltage
CMOS process in Weak, Moderate, Strong inversion

currents. Moderate inversion is more preferable, which provides high g_m/I_D, low V_{DS} than strong inversion and smaller gate capacitances, high bandwidth compared to weak inversion.

2.3. Procedure for Technology Specific Current (I_{DSspec})

Wilfredo and roth [12] presented an algorithm with flow chart to find Technology specific current (I_{DSspec}) for BSIM3 and PSP models. Also, presented for any MOS model characterization, the designer can always set the aspect ratio (W/L) to unity. Power consumption relates to high speed and low noise requirements. Power consumption can be minimized with selection of proper operating points for input transistors. This can be achieved by taking up a design procedure to derive the speed and high gain in asymptotic method. This Simulation setup with voltage biasing of MOS terminals has been fixed V_{ds} is large enough to keep transistor in saturation and a variable DC source for sweeps Vgs from low to V_{DD}. This characterization setup is to plot the Transconductance efficiency (g_m/I_D) and Drain Current (I_D) Fig. 3.

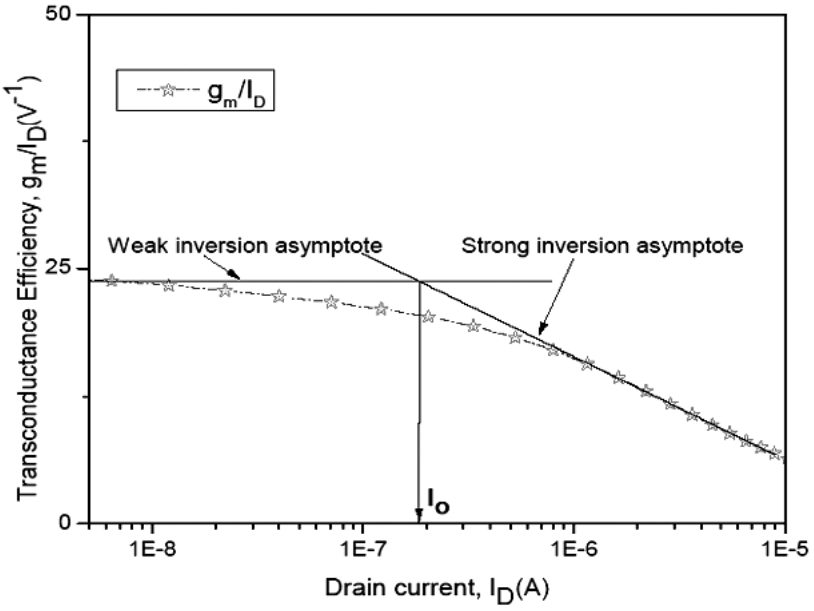

Figure 3. Measurement of Technology specific current from Transconductance efficiency and Drain current plot for NMOS transistor V_{DD}=1.5V, W=L=0.5µm.

On one hand the Fig. 3 points the weak inversion horizontal asymptote can be extended from the region where Transconductance efficiency approaches to V_{th} limit. On the other hand, strong inversion asymptote on a logarithmic scale has slope of -1/2 representing ideal "square law" region of Transconductance efficiency curve with assumption of no Velocity saturation effects. The slope of -1/2 is valid for long channel MOS device in saturation region which does not exhibit velocity saturation effects [11]. The weak inversion and saturation asymptote intersects at a point is defined as the center of moderate inversion region (IC=1) at $I_D = I_{dsspec.}$ The procedure for determination technology specific current is given by Binkley based on I_{dsspec} search algorithm.

Analog designer can determine every transistor size based on specifications of circuit design by selecting channel length (L) and inversion coefficient (IC) from MOSFET Operating plane presented by Brinkley [9]. The Transconductance of input transistors of amplifier is derived by specifications i.e. speed, GBW and noise. For amplifier, the GBW is given by

$$GBW = \frac{g_m}{2\pi C_L} \quad (11)$$

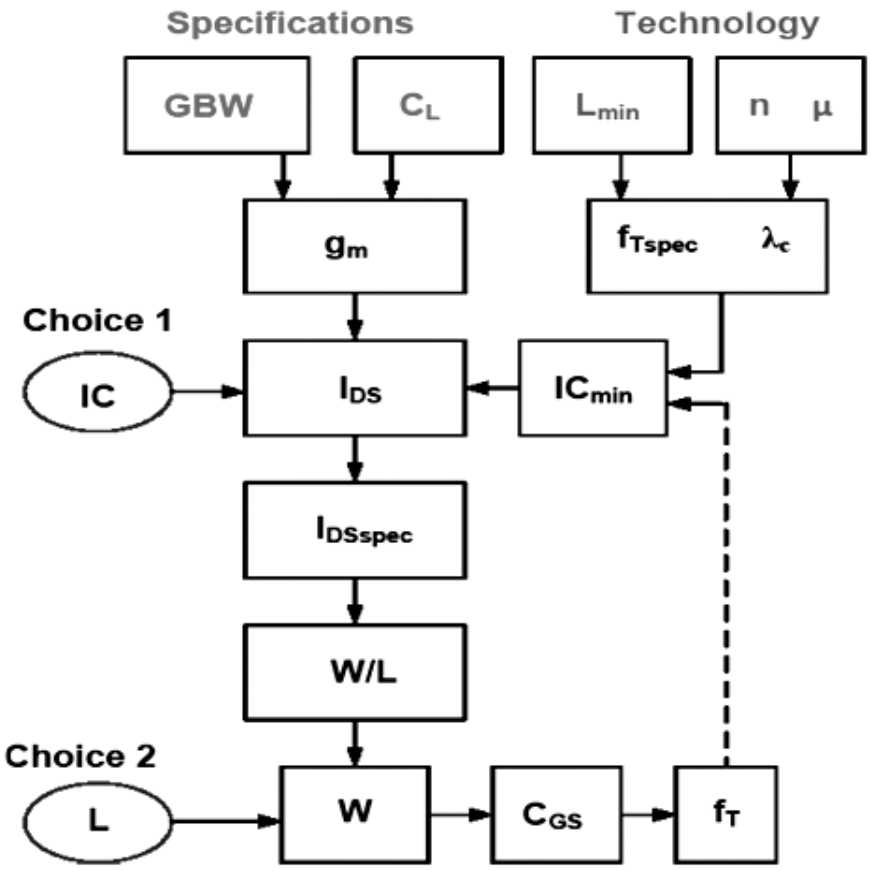

Figure 4: Design flow for optimization with length and Inversion coefficient

The above equation (10) is an important expression which is applicable to single stage amplifiers having single and high impedance node [13]. This node provides high gain and large voltage swing and also C_L is connected from node to ground which relates to GBW of amplifier is shown in equation (7). The bias current I_{DS} is derived from g_m and aspect ratio (W/L) from the current in Fig.4. For each transistor two biasing choices can be considered in the signal path i.e. inversion coefficient (IC) and channel length (L). Choosing IC is the choice of low current consumption g_m/I_D should be higher and it should provide I_{DSspec} and W/L. Choosing channel length as choice, channel length must be taken four to five times of L_{min}. This choice gives width (W), which allows the calculation of gate-source capacitance (C_{GS}) is about WLC_{OX} and it relates to transit frequency (f_T)

$$f_T = \frac{g_m}{2\pi C_{GS}} \tag{12}$$

3. SIMULATION RESULTS

3.1. Small Signal Analysis

Consider single stage telescopic OTA (Figure. 5) and derived small signal parameters are given below. Figure 6 and Figure 7 are shows the achieved simulation results of gain, phase and Input referred voltage noise and tabulated in Table1.

$$A_V = G_m.R_{out} = \frac{V_{out}}{V_{in}} \tag{13}$$

$$V_{out} = I_{out}.R_{out} \tag{14}$$

$$I_{out} = g_{m1,2}.V_{gs}$$

$$\begin{aligned} R_{out} &= (g_{m4}.r_{o4}.r_{o2} \,//\, g_{m6}.r_{o6}.g_{m8}.r_{o8}) \\ R_{out} &\cong g_{m4}.r_{o4}.r_{o2} \end{aligned} \tag{15}$$

$$A_V = \frac{V_{out}}{V_{in}} = g_{m1,2}.(g_{m4}.r_{o4}.r_{o2}) \tag{16}$$

$$w_{p1} = \frac{1}{R_{out}.C_{out}} = \frac{1}{g_{m4}.r_{o4}.r_{o2}.(c_{gd6} + c_{db6} + c_{gd4} + c_{db4} + C_L)} \tag{17}$$

$$w_{p2} = \frac{1}{R_{diodeload}.C_{diodeload}} = \frac{1}{(g_{m5}.r_{o5}.r_{o7}).(c_{gd5} + c_{db5} + c_{gd3} + c_{db3} + c_{gd7} + c_{para})} \tag{18}$$

$$\overline{V_{n,in}^2} = 2\left[\frac{4k_B.T.\gamma}{g_{m,a1}}\left(1 + \frac{g_{m,d1}}{g_{m,a1}} + \frac{R}{\gamma}\right) + 2\left(\frac{k_p}{C_{ox}.L_{a1}.W.f} + \frac{k_F.g^2{}_m}{C_{ox}.L.W.f}\right)\right].\frac{1}{f} \tag{19}$$

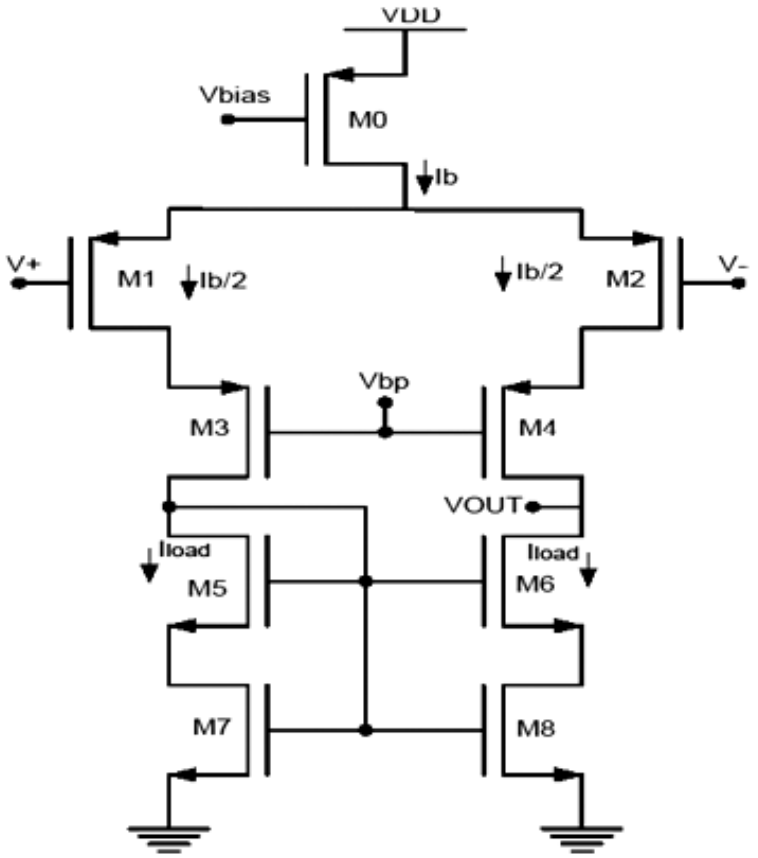

Figure 5: Schematic of Proposed OTA

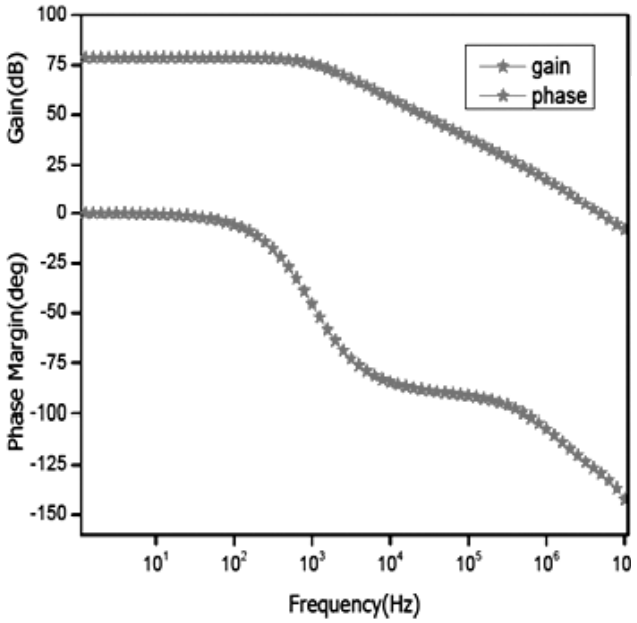

Figure 6: Gain and Phase

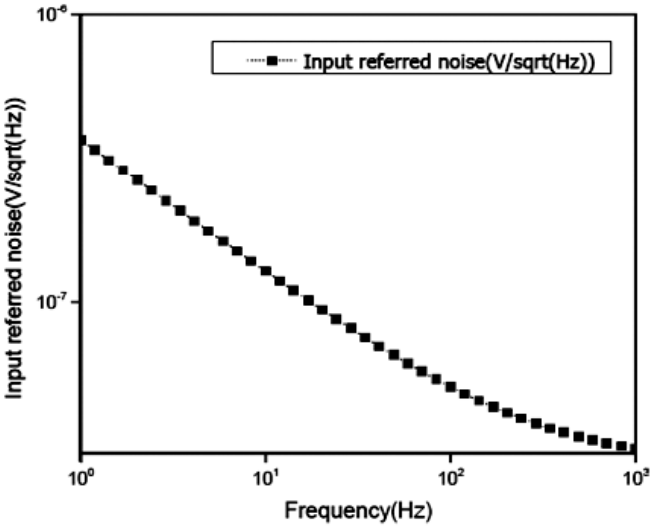

Figure 7: Input referred voltage noise

Table 1
Simulation Results of Proposed OTA

Parameters	*This work*
Technology	180 nm
Supply voltage	1.5 V
Bias Current	960 nA
Gain	78 dB
Input referred voltage noise	640nV/sqrt(Hz)
Power Consumption	1.44 µW
NEF	1.9
$NEF^2.V_{DD}$	4.33

4. CONCLUSION

This work proposes the power efficient, low noise OTA with self-cascode composite current mirror. The proposed system targets the gain and bandwidth requirement of bio-signals which are >40dB and <300 Hz respectively. This design is used to diagnose chronic diseases such as Epilepsy Seizure, Alzheimer's etc. using EEG recording systems. The Optimized trade-off between power, noise and the transistor design parameters like IC, aspect ratio (W/L), I_D are optimized for low power. The proposed circuit is designed and is simulated in TSMC 180nm Cadence environment and yields 78 dB gain, phase margin 48°, power consumption 1.44 µW and input referred noise 640 nV/sqrt(Hz). The Inversion Co-efficient methodology based design is best suited for low power design. The proposed OTA makes portable and smart health monitoring applications (IoT) more durable and suitable.

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