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# Design and Implementation of Ultra Low Power, Ultra Wide Band Low Noise Amplifier

**Chenna Reddy Peddasomappagari* and P. Aruna Priya****

***Abstract :*** We presents a design methodology and implementation of an 11-14GHz ultra-wideband (UWB) and ultra-low-power (ULP) reliable Low-Noise Amplifier (LNA).Exploiting Negative feedback advantage of providing stability, feedback series inductance technique is followed to exaggerate bandwidth, noise performance and stability of the LNA. The main variation here employed is the source degeneration inductance to resonance the intrinsic frequencies to increase the frequency. The ULV circuit design challenges are discussed and a new biasing metric for ULV and ULP designs in deep sub-micrometer CMOS technologies is introduced. A new biasing metric, has been implemented that provides substantial ease in the design analysis and implementation. Series inductive peaking in the feedback loop, a 0.4 V, 3.6-mAmp current budget, reuse scheme broadband LNA is implemented in a 45-nm submicron CMOS technology. Simulation results show 5.2-dB voltage gain, 11–14GHz bandwidth, 6-dB NF, 5U associated power gain,S11< -12dB of absolute impedance matching, are simulated using Agilent Advanced Design Systems .

***Keywords :*** Current reuse technique,45-nm,submicron technology, series inductance peaking, low- noise amplifier (LNA), Source and Load rolet stability factor(K), resistive shunt feedback, ultra-low power (ULP), ultra-low voltage(ULV),ultra-wide band (UWB).

## 1. INTRODUCTION

Following the concepts of ultra-scaling technology, also popularly known as submicron technology to attain high frequency of operational bands has became the only distinguished option for Wireless Sensor Networks. The shrinking of the size of CMOS however reduce the power consumption with tradeoff of operating speed and conversion losses. Health care, environmental monitoring, industrial settings, and agriculture. The nature of these applications imposes severe restrictions on the power consumption of a WSN node. As a result, ultra-low-power (ULP) RF front-end circuits are required to maximize battery lifetime and to allow operation from energy harvested from the environment.

While operation from a low supply voltage is desirable in systems powered by energy harvesting minimize conversion losses, due to second order effects. Consequently, circuits operating from very low supply voltages have become very notable and are under active research [1]–[5].

Along with the above design challenges and the limitations of nanoscale CMOS technologies like, higher output conductance, velocity saturation, and mobility degradation, the high transit frequency, $f_T$, of short channel effect in CMOS and BICMOS technologies is a major trade off factor with power consumption to design and employ CMOS RF low power circuits.

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A broadband low noise amplifier is vital component in the family of RF circuits front end design. The wide band LNA should meet the draconian constraints and requirements. Any fault in holding these requirements lead to premature failure of LNA device.

This compromise was first highlighted in [6] in which a biasing metric is introduced for low-power RF design. While useful, this biasing metric does not include the effects of the output conductance, $g_{ds}$ and the drain–source voltage $V_{DS}$ on the intrinsic gain, both of which are becoming very important in ultra-low voltage (ULV) and ULP designs. To overcome these issues, this paper suggests a scopious biasing metric that is feasible for ULV and ULP low noise designs and manifest it's applicability by designing an ULP, ULV ultra-wideband low noise amplifier (LNA).

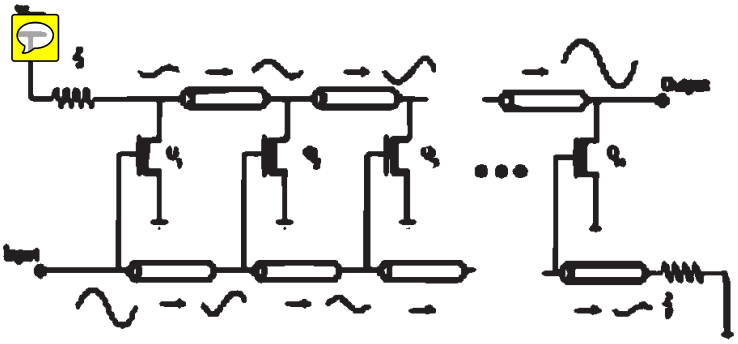

**Figure 1: Distributed n-stage Amplifier LNA**

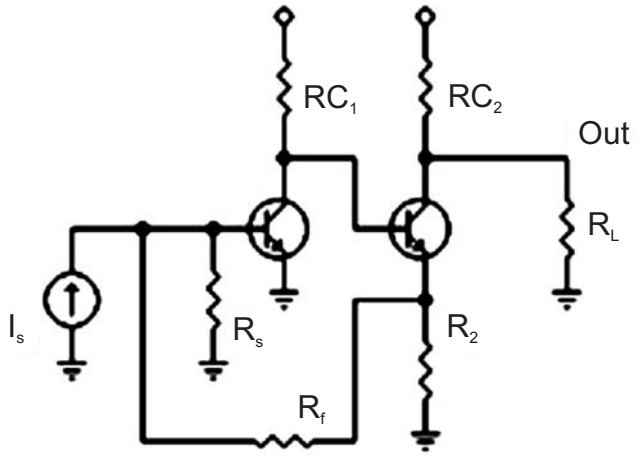


**Figure 2: Cacoded Shunt Feedback LNA**

The LNA is the first volant component in the front-end of the receiver, and is generally considered as one of the most power famish blocks. The high power consumption all is because LNA must provide simultaneous wideband impedance matching, high gain, low noise, high both end stability and high linearity, all of which require exemplary high power and high supply voltages. These mixed specifications have made the design of low-power and low voltage UWB LNAs a challenging research topic.

There are many distinctive techniques to design wide- band LNAs. All show their own pros and cons but usual familiar approach is to employ distributed amplifiers [7]–[9] as shown in Fig. 1, while providing high bandwidths that can span into the multi-gigahertz range amidst results in very high power consumption and large area intake with N-cascoding stages still with lower efficiency.

The resistive shunt feedback architecture is another workable solution for wideband LNA design. This involves placing a feedback resistor around a common source amplifier to realize a wideband 50-*K* input terminal match impedance as shown in Fig. 2 [16]–[19]. Despite, there is a tradeoff between input matching and the NF of the LNA, and satisfying both the parameters results in high power consumption [17]–[21].

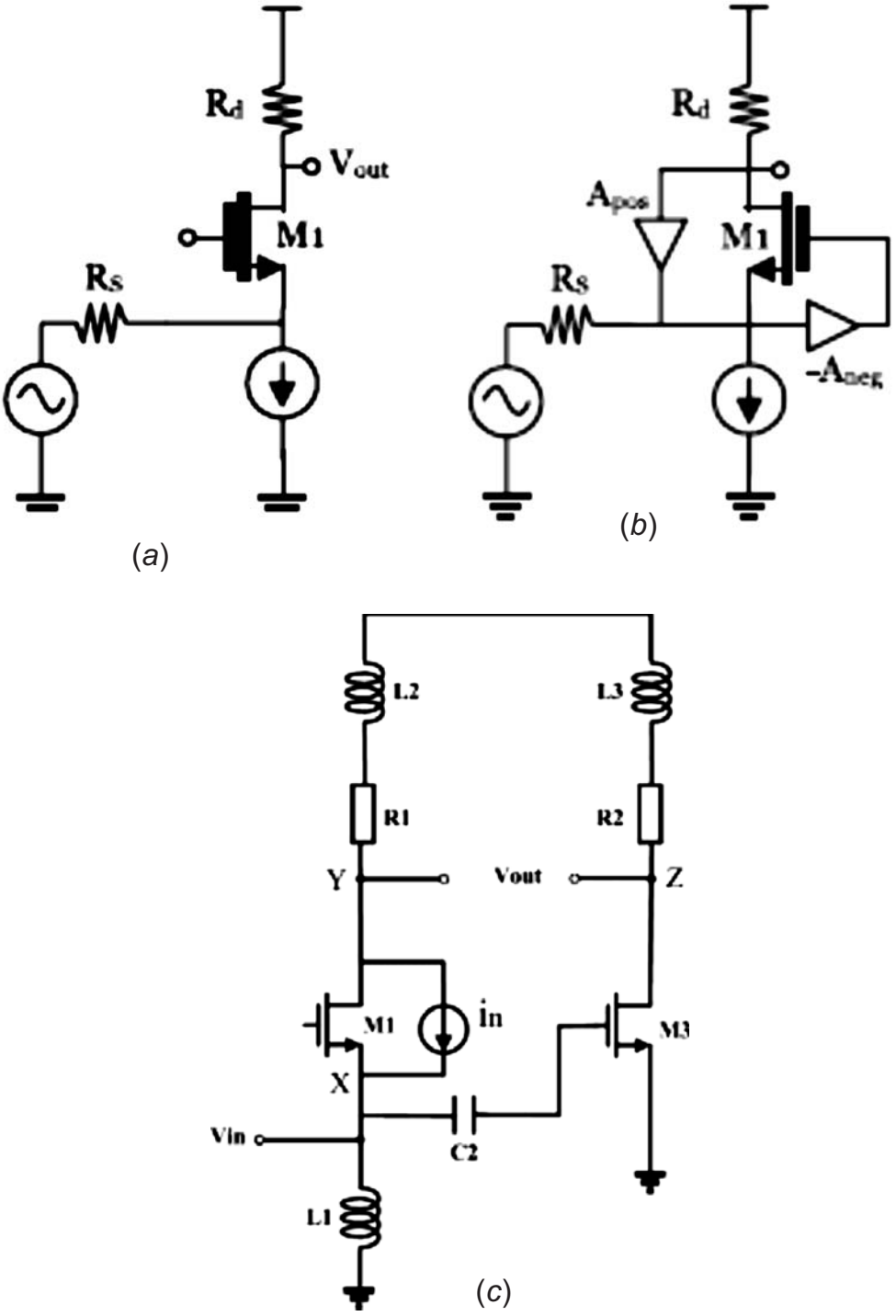


**Figure 3: (*a*) Common Gate LNA. (*b*) Mixed design of feedback and forward path. (c) Noise Cancellation Scheme**

Another design approach is to use a common gate (CG) transistor as the input stage as illustrated in Fig. 1(*a*). The desired input impedance of a CG input stage is achieved by adjusting the bias current, aspect ratio, and overdrive voltage such that $1/g_m$ is close to the termination impedance $Z_0$. Typically, single-ended $Z_0$ is 50 ohm, and hence a $g_m$ of approximately 20mS is required. Despite of wideband matching, this scheme faces two major problems. The input matching requirement of $g_m R_s = 1$ for CGLNA bounds its noise factor at $F = 1+ \gamma/\alpha$, where $\alpha = g_m/g_{d0}$. Clearly, α should be increased to decrease F. This seems unfeasible because α is constrained at the device level. Two schemes that have been used to improve CG stage circuit performance in reference with noise figure are noise cancellation and source degeneration. A conventional noise cancelation technique in LNAs is demonstrated in Fig. 1(*c*). Noise cancellation schemes have been shown to enhance the NF,

but this comes at the cost of higher power consumption due to extra stages and high supply voltages [11]–[13]. A mixed design of feedback and feedforward techniques, shown in Fig. 1(*b*), has been used to break the tradeoff between NF, gain, and input matching [14], [15], however, the extra stages add parasitic capacitances and limit the bandwidth of operation. These examples show that reaching a low-power and wideband solution with a CG input stage is a challenging task.

As a result, neoteric circuit design techniques are necessary to mitigate the power consumption.

This paper illustrate and depicts the challenges encountered while designing ULPLV circuits, and introduces an extended ultra low power and low voltage (ULPLV) biasing metric to optimize transistor performance. A combination of circuit techniques that are suitable for ULPLV designs are presented, and a broadband resistive-feedback inductance peaking LNA in a 45-nm CMOS technology is designed using these techniques and its measured performance is compared with state-of-the-art works. The principles in the proposed low voltage and low-power design methodology presented here can be readily adapted and applied to other RF circuits.

The following paper is organized as follows. First, ULP model challenges are discussed in Section II. The Proposed ULV, UWB LNA design schematic is presented in Section III. Section IV depicts the circuit stability, Noise Figure (NF) and current budget simulation analysis of the proposed ULP,UWB LNA. Finally, Section V summarizes this paper.

## 2. ULTRA LOW POWER MODEL CHALLENGES

Modern technology needs the requirement high speed and high frequency applications. But both of them come with trade off to each of their own. If not, to satisfy both leads to increase in enormous power consumption. So the only feasible approach is to scale down the aspect ratio of MOS device. Thus scaling substantially decreases the required supply voltage.

But with rapid scaling in integration of devices and reduction of supply voltage is possible to a level of threshold voltage level. Any variation in setting down have great impact on inversion coefficient, linearity, flicker noise, intrinsic gain.

### A. Inversion coefficient

Trans-conductance is the change in the drain current divided by the small change in the gate/source voltage with a constant drain/source voltage. Typical values of *gm* for a small-signal field effect transistor are 1 to30 milli-siemens.

The ratio of trans-conductance to the supply drain voltage is known as Trans-conductance Efficiency. The trans-conductance efficiency shows various steady and exponential characteristics depending on a coefficient called as inversion coefficient which represents the level of MOS inversion[22]. The trans-conductance efficiency shows exponential behavior in sub-threshold region also called as weak inversion region (WI).MOS device operates with low voltage supply in WI. Weak inversion corresponds to IC < 0.1. But it affects the unity current gain cut off frequency. As there is need to operate at high frequency, therefore this region is not well suited.

In Medium inversion (MI) region gate voltage reaches the threshold voltage. Medium inversion region corresponds to 0.1 < IC < 10.

Greater change than threshold results in strong inversion region (SI) which provides steady variations due to gate to drain supply voltages and provides better matching. Strong inversion region corresponds to IC > 10.

$$IC = I_D/I_0.S$$
$$= \exp((V_{gs} - V_{T0}) / nU_T)) \quad (1)$$

and

$$I_D = 2nm_0C_{OX}(W/L)(U_T)^2 \exp((V_{gs} - V_{T0}) / nU_T)) \quad (2)$$
$$I_0 = 2nm_0C_{OX}(U_T)^2 \quad (3)$$

Where IC is Inversion Coefficient

$I_D$ is drain soure current [A]

$I_0$ is technology current [A]

S is transistor size aspect ratio

$n_0$ is substrate factor

$m_0$ is field mobility factor [mA/V$^2$]

$C_{OX}$ is gate-oxide capacitance [Ff/mm$^2$]

$U_T$ is thermal voltage [mV]

From 1 and 2, Transconductance efficiency

$$g_m/I_D = 1/(n.U_T.(\sqrt{(IC + 0.5\sqrt{(IC)} + 1)) \quad (4)$$

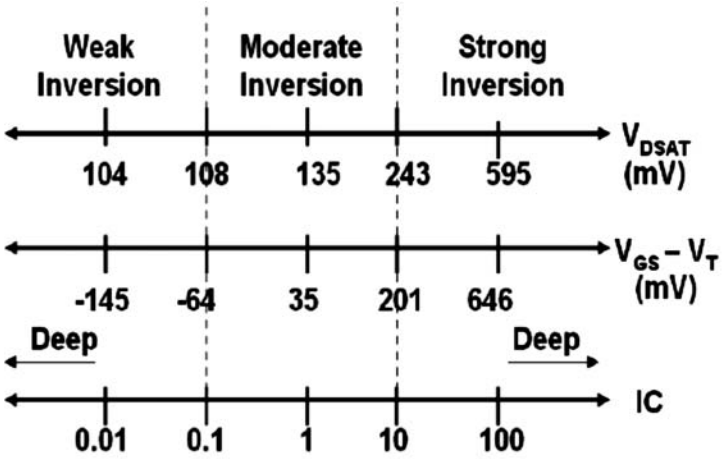


**Figure 4: IC versus ($V_{DSAT,}$ $V_{eff}$)**

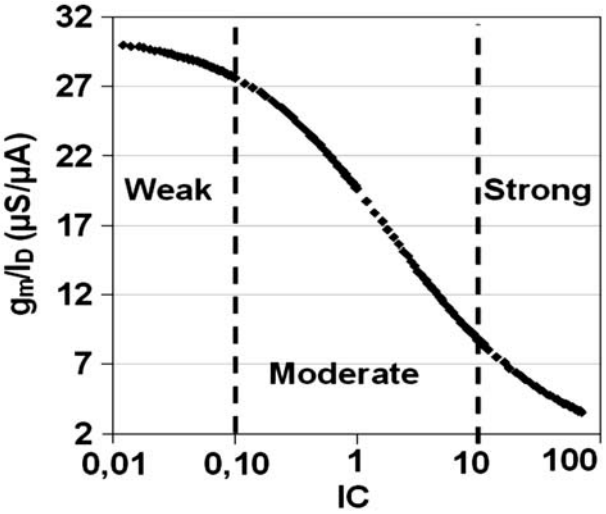


**Figure 5: Trans-conductance Efficiency versus IC**

## B. Linearity

The linearity of LNA is also gets reduced with usage of ultra low drain supply voltages. The nonlinear behaviour of a MOS device can be expressed interms of Vgs and $V_{ds}$ by a taylor series.

$$I_{ds}(V_{gs},V_{ds}) = g_m V_{gs} + g_{ds} V_{ds} + \acute{g}_m(V_{gs})^2 + \acute{g}_{ds}(V_{ds})^2 + \acute{\acute{g}}_m(V_{gs})^3 + \acute{\acute{g}}_{ds}(V_{ds})^3 \quad (5)$$

In the above expression of terms, it can be known that $\acute{\acute{g}}_m$ is the strongest contributor the third order harmonic distortions $\acute{\acute{g}}_{ds}$ also varies with $V_{ds}$ and decreases rapidly with decrease in supply voltage resulting non linearity of LNA[24].

### C. Dynamic range

Dynamic range is limited by low power supply in analog/RF circuits and offers reduced voltage headroom for cascode structures. So new techniques are required to obtain the same performance while using low power supply voltages.

### D. Transit Frequency

A very common and other important characteristic parameter that effects the gain and $NF_{min}$ proportionally is the transit frequency. This is the frequency at which the extrapolated gain $h_{21}$ of small signal for short channel devices, the carriers enter into velocity saturation. After the velocity of carriers is saturated the device no longer depend on the channel length.

## 3. PROPOSED ULV, UWB LNA DESIGN SCHEMATIC

The proposed ultra low power, ultra wide band LNA is a combination model that exploits the features of current reuse scheme, series gate inductive peaking and resistive feed-back shunt for low power consumption, input matching and to provide high wide-band frequency generation.

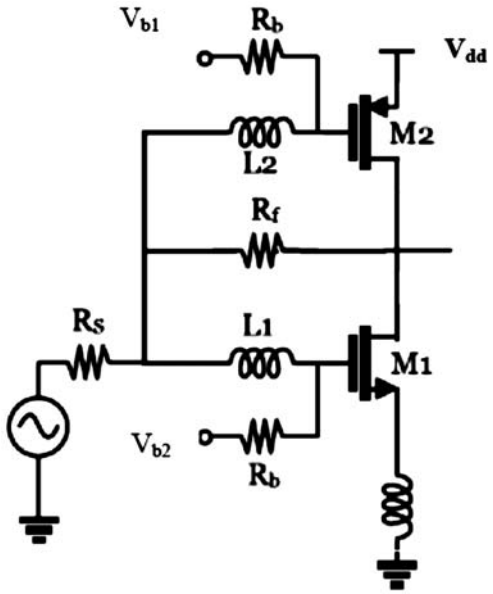


**Figure 6: Proposed Current reuse source degeneration, resistive shunt feedback LNA with inductive series peaking in the feedback loop**

Resistive shunt feedback ($R_f$) is a viable option for UWB LNA design. It provides wideband input matching with the aid of a feedback network. In this protoplast design, the bias voltages $V_{b1}$ and $V_{b2}$ were used to tune the gate voltages of M1 and M2 such that to give flexible control over LNA, providing dc feedback to make ensure that the drain voltages are midrail.

### A. Low-Power, Low Voltage RF Design Biasing Metric

As earlier said reference[6] had not included the intrinsic gain and output trans-conductance effects, this mitigation of advantage overcome by including the remaining by exploiting the following biasing metric for BSIM model,

$$\text{Biasing Metric}_{(\text{ULP, ULV})} = (g_m/I_D)\cdot(g_m/g_{ds})\cdot f_T. \quad (6)$$

In Weak Inversion (WI) region, $g_m = I_D/nU_T$

Hence, $$\text{Biasing Metric}_{(\text{ULP,ULV})} = 1/((nU_T)^2.g_{ds}).f_T \quad (7)$$

The above biasing metric is very novel in giving an optimistic value of current budget for the proposed design. The biasing metric by view can be familiarly defined as the product of trans-conductance frequency, intrinsic gain, transit frequency.

### B. Overdrive Gate–Source and Drain–Source Saturation Voltage

The required overdrive gate-source and drain-source voltage saturation voltages for different inversion regions are given below.

In general, Overdrive voltage ($V_{od}$) = $V_{gs} - V_{th}$, using (1)

$$V_{od} = nU_T . \ln(\sqrt{IC}) \quad (8)$$

The drain–source saturation voltage which is paramount to ascertain that the contrivance is partial in saturation is defined by[23]

$$V_{ds,\,sat} = 2U_T(\sqrt{IC} + 0.25) + 3U_T \quad (9)$$

## 4. PROPOSED CIRCUIT DESIGN ANALYSIS AND SIMULATION

The above is the proposed ultra low power, ultra wide-band Low Noise Amplifier(LNA) schematic. The MOS devices employed are BSIM model in 45nm CMOS technology. Both terminals of the schematic are terminated with a matching a impedance of 50 ohms as it represents the resistivity of the cable wire used for communication of signals.

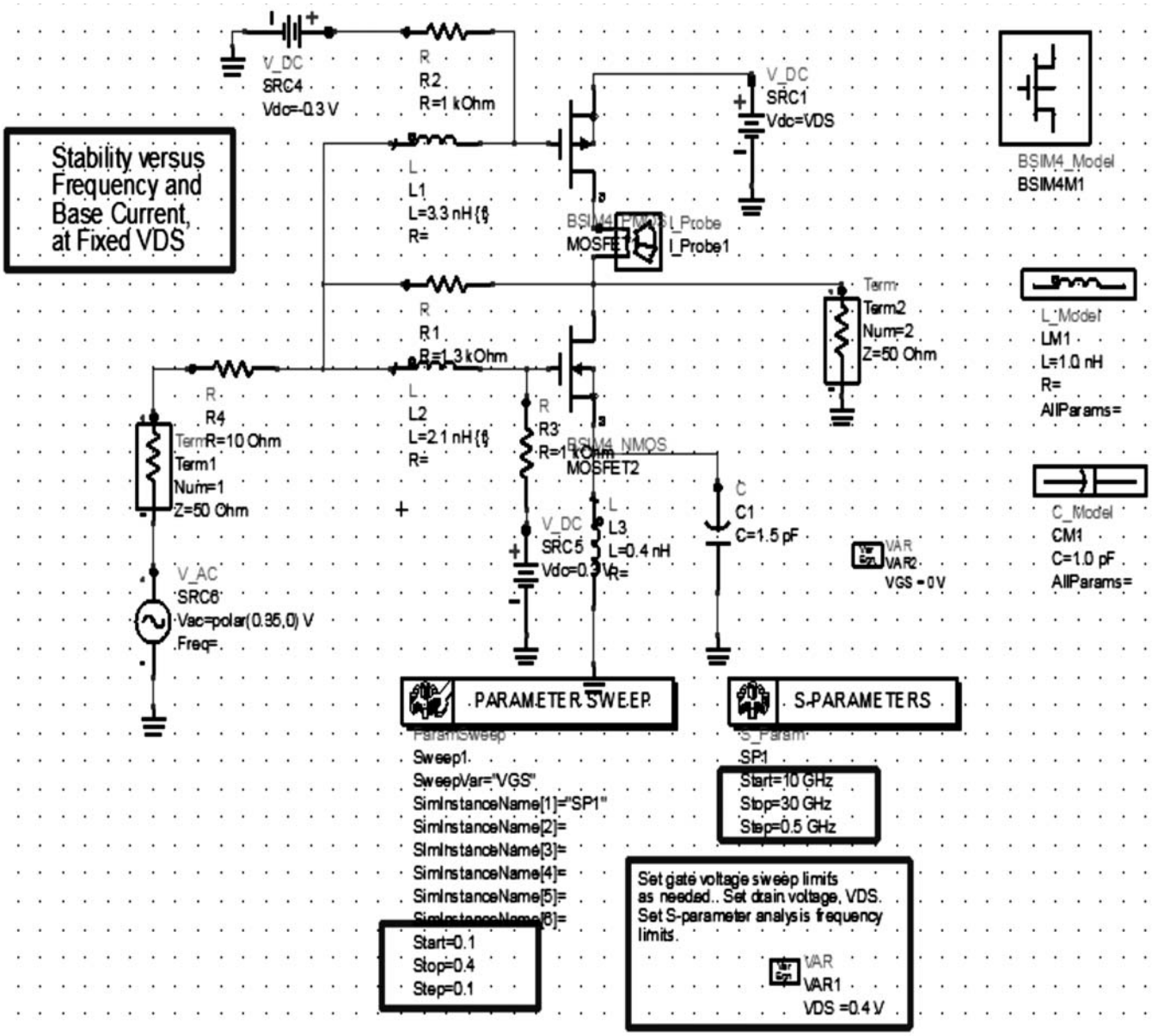


**Fig. 7. Proposed Model Schematic of LNA in ADS.**

**Table 1**

**Device Dimensions**

| *Component* | *Value* |
|---|---|
| $M_1$(NMOS) | 45nm / 14.8μm |
| $M_2$(PMOS) | 45nm / 28μm |
| $R_1,R_2,R_3$ | 1KΩ |
| $L_1,L_2,L_3$ | 3.3nH,2.1nH,0.4nH |
| $C_1$ | 1.5pF |

The dimension of the active and passive components of the LNA device are shown in the above table.

## A. Scattering(s) Parameters Simulation

**Scattering(s) parameters** describe the electrical comportment of linear electrical networks when undergoing sundry steady state stimuli by electrical signals.

**The following information must be defined when specifying a set of S-parameters :**

1. The frequency
2. The characteristic impedance (often 50 Ω)
3. The allocation of port numbers
4. Conditions which may affect the network, such as temperature, control voltage, and bias current, where applicable.

**Input Reflection Coefficient ($S_{11}$)**

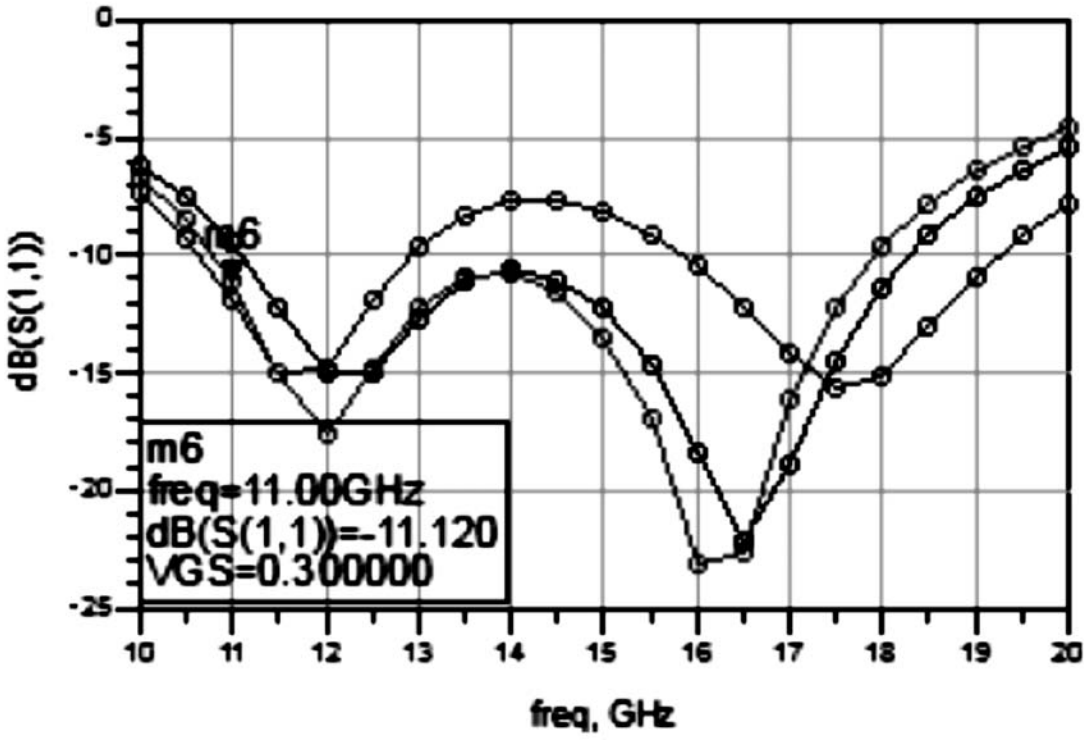


**Figure 8: $S_{11}$ versus Frequency**

**Reverse Voltage Gain($S_{12}$)**

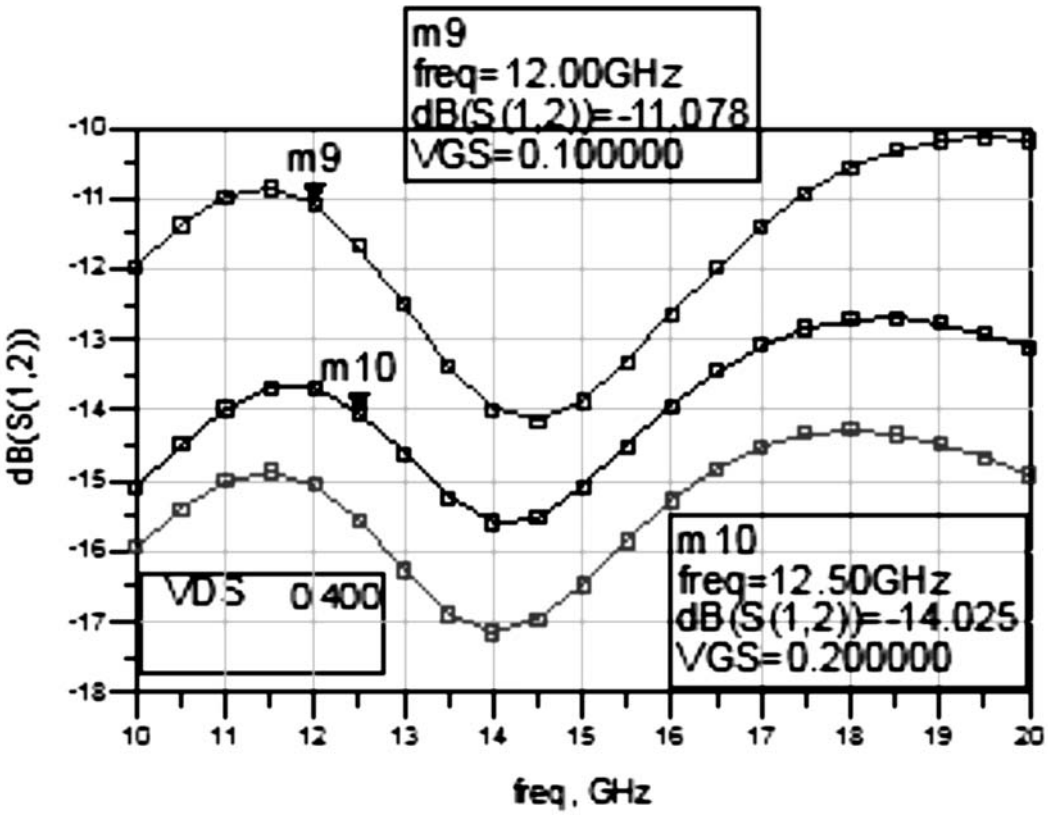


**Figure 9: $S_{12}$ versus Frequency**

**Forward Voltage Gain ($S_{21}$)**

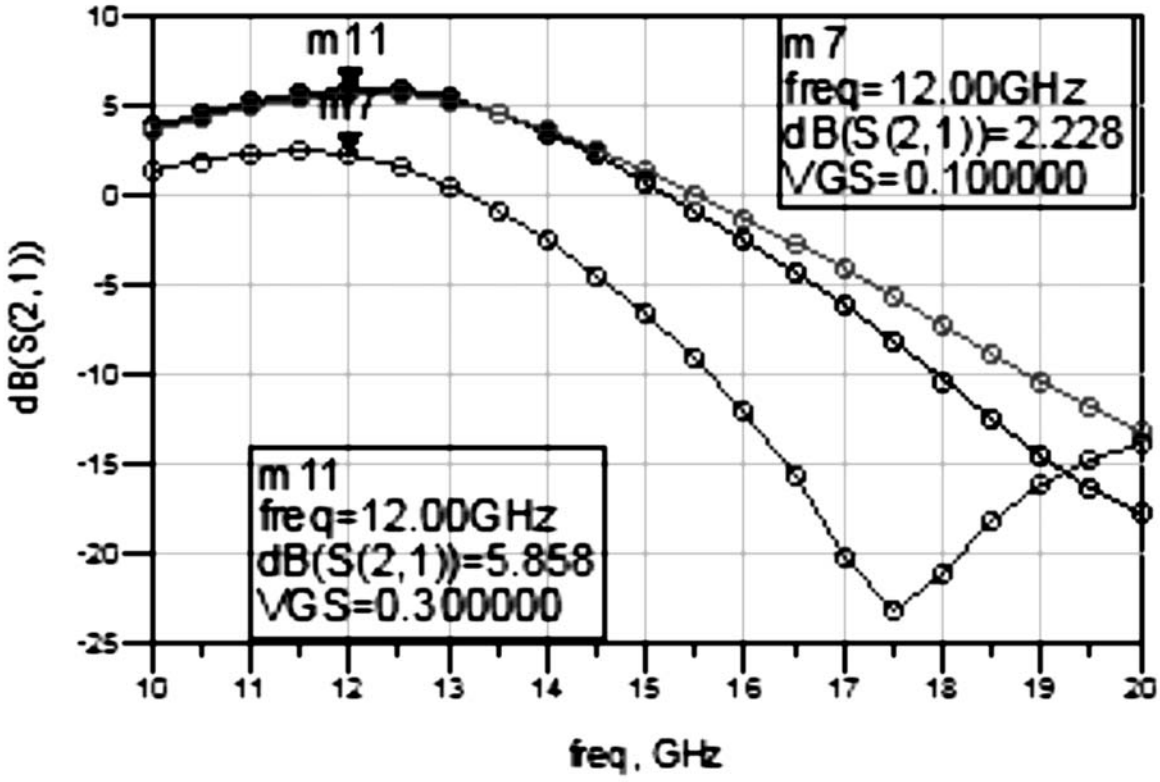


**Figure 10: $S_{21}$ versus Frequency**

**Output Reflection Coefficient ($S_{22}$)**

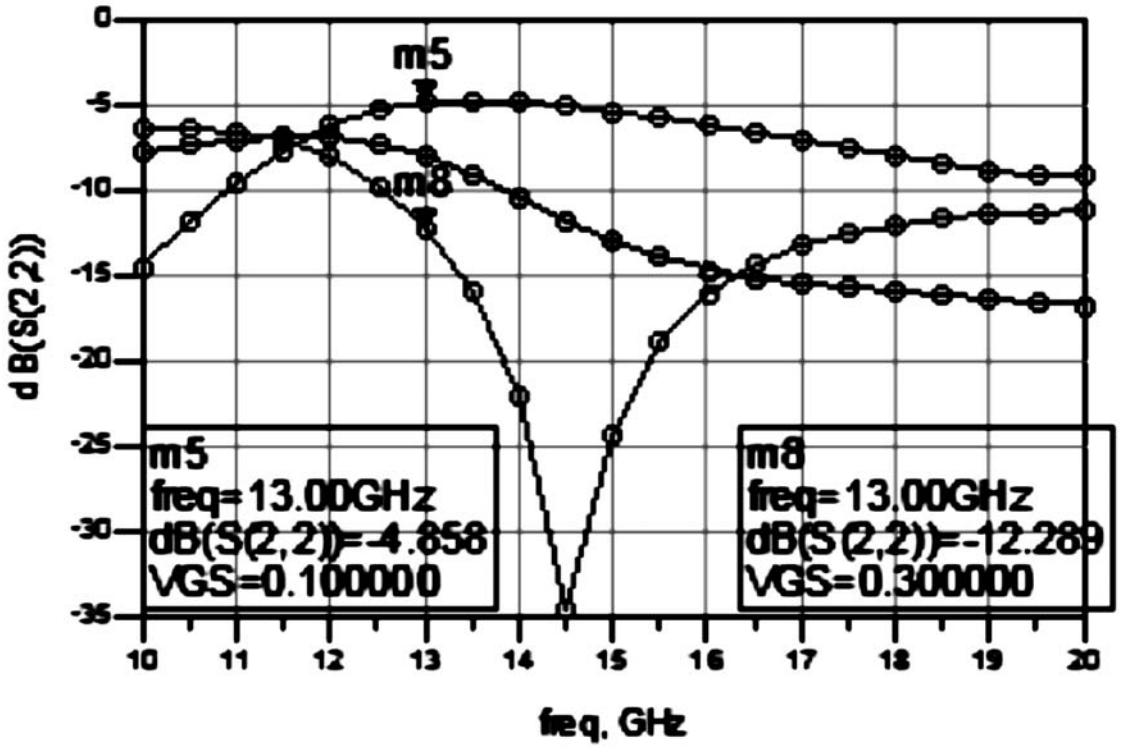


**Figure 11: $S_{22}$ versus Frequency**

In the above all scattering parameter, have justified their minimum value to make an LNA to be operated in the respected wideband thought for.

## 5. CIRCUIT STABILITY & NOISE FIGURE SIMULATION ANALYSIS OF THE PROPOSED ULP, UWB LNA

In the proposed design, we had used shunt feedback resistance to provide a wide-band operation. A current reuse scheme is also employed for low power consumption. Mainly the series inductive peaking and source degeneration inductors have been added in order to cancel the parasitic intrinsic capacitances and if more required that to resonate them. Thus the source degeneration inductor resonate the capacitance to enhance the bandwidth and forward gain. The only drawback of source degeneration is as it adds little noise on beyond the operating inversion region frequencies[20].

### A. Noise Figure(NF)

The main noise sources in this LNA are the channel noises of M1 and M2 and the thermal noise of the feedback resistor, $R_f$ . The noise factor of the LNA by neglecting the little noise produced by source degeneration inductance can be expanded as below,

$$NF \sim 1 + (R_f/Rs)(1+ g_{mt}R_s/1-g_{mt}R_f)^2 + (gg_{mt}/aR_s)[(R_s + R_f)/1 - g_{mt}R_f]^2 \quad (10)$$

In the above expression of NF, the second term is due to the feedback resistor, $R_f$ ,and the third term is the noise contribution of the transistors. The minimum noise figure of the proposed LNA is shown in fig. 12.

### B. Stability Factor(K)

The LNA should provide stability both at source and load with maximum impedance matching unconditionally, generally known as Rolet's stability factor(K). The stability factor(K) of the LNA with respect to two terminal source and load should be >1 unconditionally, are shown in fig. 13, 14.

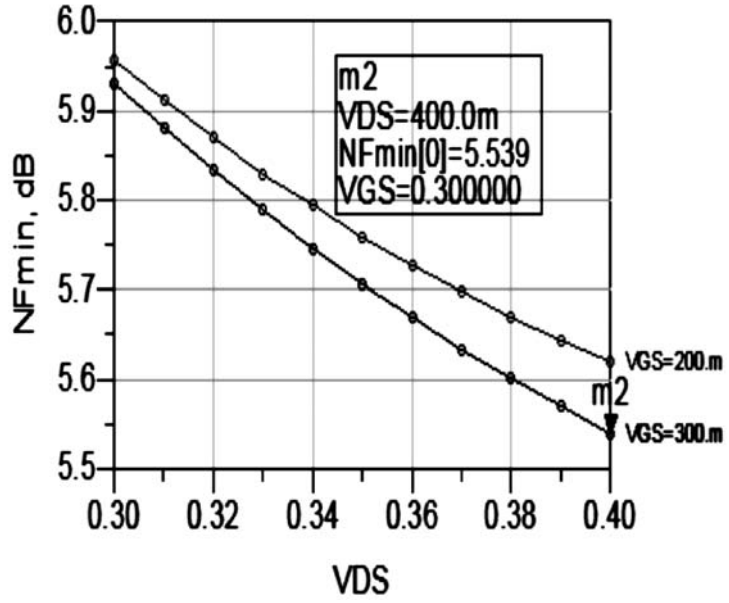


**Figure 12: Minimum Noise Figure versus VGS and VDS**

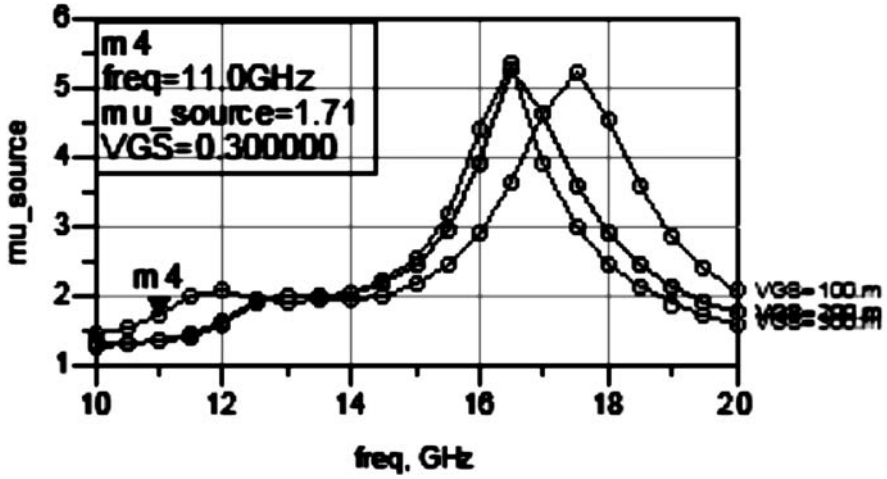


**Figure 13: Geometrically-Derived Source Stability Factor**

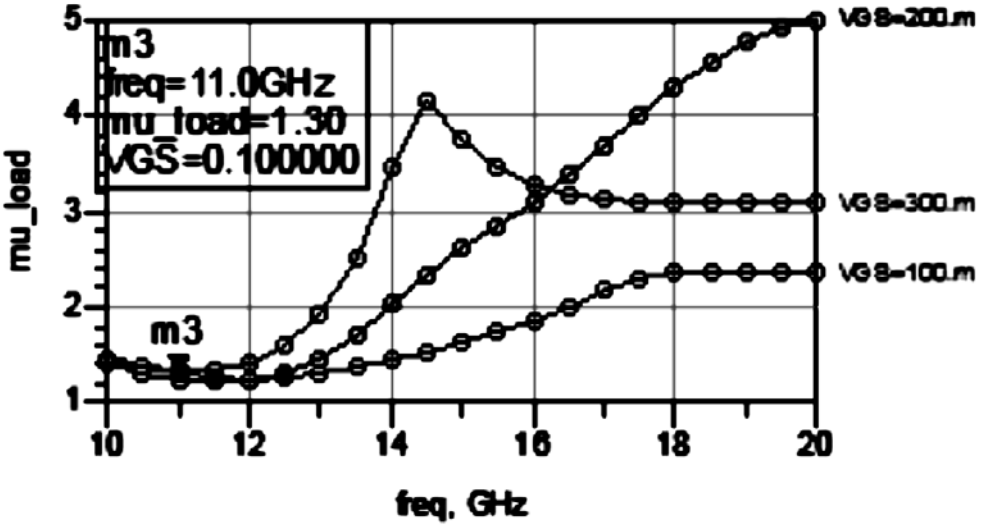


**Figure 14: Geometrically-Derived Load Stability Factor.**

Finally the combined source and load, Rollet stability factor(K) is given as

$$K = (1 - |S_{11}|^2 - |S_{22}|^2 + |D|^2) / (2|S_{12}S_{21}|)$$

Where $D = S_{11}S_{22} - S_{12}S_{21}$

And shown below in the fig. 15.

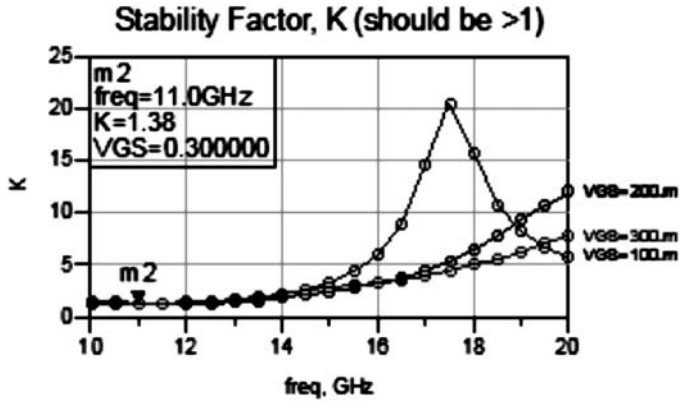


**Figure 15: Stability Factor(K) versus Frequency.**

## C. Current Budget

The independent drain-source current that is needed for a biasing voltage at a constant supply voltage for operating at a band of frequency is shown below in fig. 16.

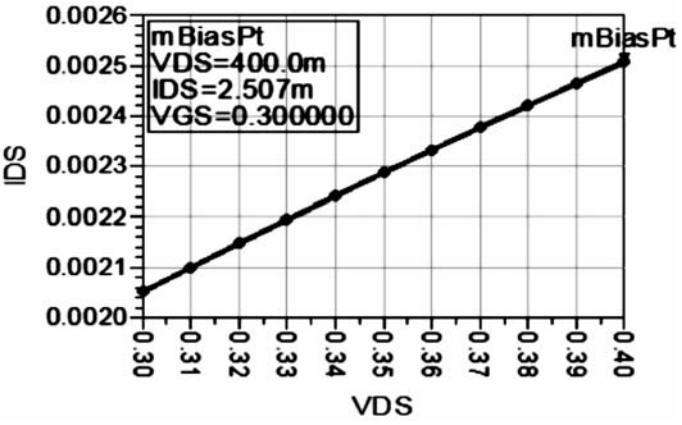


**Figure 16: Current drawn($I_{DS}$) versus Supply Voltage($V_{DS}$)**

**Table 2**

**Performance Summary and Comparison with State-of-the-arts LNAS**

| *Parameter* | *This Work* | *[14]2009 ISSCC* | *[33]2011 E. Lett.* |
|---|---|---|---|
| 3-dB BW(GHz) | 11-14 | 0.3-0.92 | 2.6-10.5 |
| Power(mW) | 1 | 3.6 | 0.99 |
| Supply(V) | 0.4 | 1.8 | 1.1 |
| $S_{11}$(dB) | < – 11 | < – 9** | < – 10 |
| $NF_{min}$(dB) | 5.5 | 3.6 | 5.5 – 6.5 |
| Stability(K)* | > 1.38 | – | – |
| Technology | 45nm | 0.18mm | 0.18mm |

*Indicate both combinational source and load stability factor.

**Estimated from the curves.

## 6. CONCLUSION

An ULP, ULV wideband CMOS LNA is proposed and designed based on an extended biasing metric for low power and low voltage circuit design. The LNA presented here achieves the lowest power consumption and employs the lowest supply voltage with minimum current budget, when compared with other works. The main highlight of this LNA is it posses both the source and stability factor(K) of > 1.38 in operating band of 11-14GHz. A current-reuse scheme to lower the power consumption, source degeneration to enhance frequency resonance along with inductive series peaking in the feedback path to increase the bandwidth, are analyzed and employed in the LNA. The LNA operates over the bandwidth of 11–714GHz and achieves a voltage gain of 5.8 dB, a minimum NF of 5.5 dB, and a standard stability factor >1, while consuming only 1 mW from a 0.4-V supply voltage.

## 7. ACKNOWLEDGMENT

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