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A Study on SKB Tree Representation for MSV Floorplanning

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ABSTRACT

Technology shrinking made notable impacton Power Consumption in design of System-on-Chip(SOC).Multiple Supply voltage(MSV) is one of the technique used for reducing Dynamic power and it will satisfied timing constraint after the voltage assignment of the cells.SKB-tree has good property deals with previous work problems like fixed-outline floorplan- ning,voltage island driven floorplanning ,IR-drop and by it constraint fixed-outline floorplanning without zero death space and gives better result compared to other floorplanning.In this paper the number of voltage islands are kept constant and density of elements in the voltage islands are changed for the performance evaluation. The results shows that change in density has an impact in power dissipation but not in the delay.

Keywords: Low power VLSI, Multiple supply voltage, floorplan- ning, SKB tree

I. INTRODUCTION

Designing complexity in SOC has increased by new mod- ern technology mostly used is MSV (multiple supply volt- age)due to this two issue should by handle properly they are fixed-die region and multiple supply voltage blocks.die shape is determined before the floorplanning .In the cost function contains different factor such as area and wire-length it increase the difficulty of the convergence of the program .the power management leads to higher power densities has become a challenge. [7]. The figure1 shown below the structure of core consists of voltage islands with (0.6V to 1.2V).

In the MSV high-VDD on cells is allotted to the criti- cal path and low-VDD is allotted to the non-critical blocks which is designed by the designer. partition a chip the done according to the supply voltage of island and it is placed in the proper regions. Level shifter block are placed in near the neighbouring blocks to make the power planning. Issue in the MSV floorplanning can be overcome by SKB-tree with his good properties it voltage island drives floorplaning are placed the block which operate in the same voltage with in the fixed-outline. the islands which operate in the one voltage placed into several islands it will leads to more power routing resource, increases the complexity of the power ,voltage drops and create the more complexity placing the level shifters. This type of the problem will increase the more complexity of the power planning due to the overlapping of wires. SKB- Tree representation fixed-outline floorplanning optimize total wirelength and it also constrain the zero death space in the chip.

II. RELATED WORKS

In [2], Two algorithm are used for solving the voltage assignment problem they are min cost flow(MCF)and value- oriented branch-and bound (VOBB) algorithms. MCF is a fast algorithm and VOBB is a slower but it an optimal algorithm. in the simulated annealing based floorplanner will embed the faster MCF algorithm for obtaining the minimum power consumption. VOBB algorithm applied in the post processing steps this

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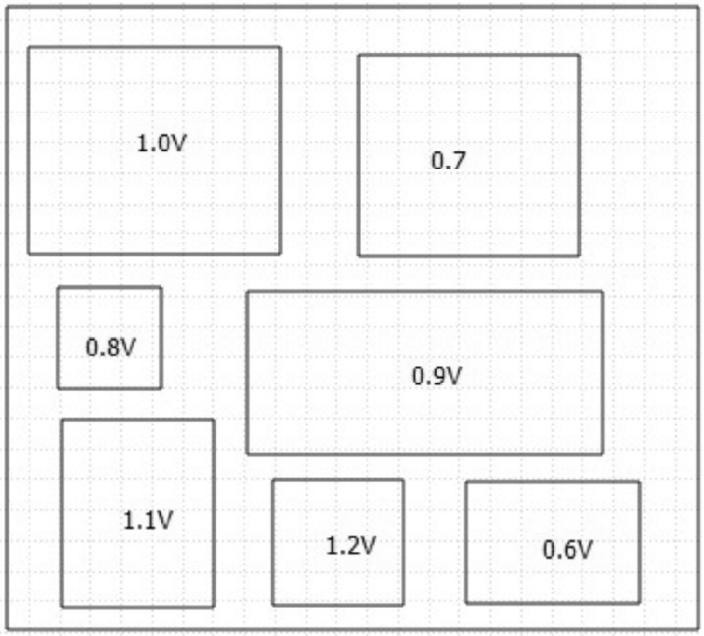

Figure 1: General view of the core consist of different supply voltages

approach significant improvement on the power saving compare to the most updated previous works. the delay of the modules are calculated with the number of clock cycles the MCF named by cost-scaling algorithm after the voltage assignment solution from flow value network.delay choices on each edge are not continuous it will not produce the voltage assignments.but VOBB is gives the optimal voltage assignment by employing the MCF on the candidate floor plan which is did by VOBB by this process it will produce the optimal output which the designer required.this framework classified into floorplanning stage and post processing stage. in the floor planning stage to get the minimum delay and wire ability the modules are moved randomly and level shifter are placed and once again power is calculated the VOBB algorithm is performed once again the working voltage to each module to the timing constraint is satisfied.

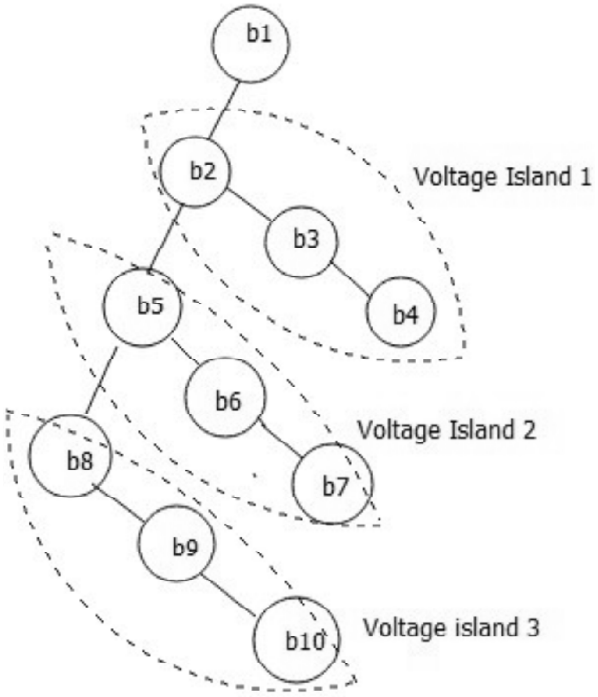

Figure 2: SKB- tree with different voltage levels

III. SKB TREE

Due to new designing requirement increase in the cur- rent IC design the floorplanning become complex. In this two important problem are fixed outline and voltage-island driven floorplanning.By using the SKB-tree [1] (skewed B*- tree)problems can by solved .It is used for voltage-island driven floorplanning for placing the block which have same voltage into fixed-outline island, which can able to reduce power routing resource. SKB-Tree also called as a left-right skewed B*-tree. The figure 2 shown below is the SKB tree with levels of the tree as Voltage islands.

Compare to the B*-Tree[3] it searching time is low because it has only right-childs. It does not need contour during the packing of the blocks .set of block allocation is done according to their area so soft block are placed into a restricted region for each solution .A zero dead space floorplanning with soft block have achieved very easily by using the SKB-Tree representation .

Here different power supply are allocated for the various blocks the power planning become difficult so the designer should be handle the power pad very carefully because it cause the overlapping when it get overlapped it produce the IR drop the cluster constraint the blocks which are all working in the same voltage are placed in island which makes optimization of area and wire length difficult. To solve this block voltage determined using dynamic programming to obtain an optimal power consumption and initialize voltage island based on the result.

IV. VOLTAGE-ISLAND DESIGN

In [4] the MSV design the voltage are classified into two types row based and voltage based islands .In this standard cells are rearranged according to the operating voltage and it is placed in different row Each rows operate with the different voltage level. Voltage island based powered by the special pads with the different voltages. The islands are formed by the group of clusters .it has the collection of standard cells which is operated in the same voltage level. It done for low power designing it brings the complex problem in physical level floor planning and the thermal distribution .

Pitch is not placed in the top level design because search pitch will consume time during in floor planning and its not need also[5]. In global power supply network voltage drop is very sensitive to the position of the voltage islands.

In the power grid network pattern the cells operate in the different voltage will share the same ground. The voltage island should be placed near to the power pins in order to minimize the complexity of power routing and IR drop. [6]

Level shifter are placed behind the islands to overcome the delay and area. its inserted to nets according to the voltage assignment of VDDL and VDDH. Voltage assignments will not done similar with the floor planning. The island merging is help us to get the optimized area. To reduce the system search for islands timing cost table technique is used it done by dynamic programming. By this technique reduce the searching space, frame works and the total power consumption.

V. EXPERIMENTAL RESULTS

Two processor’s such as Sayeh and lambda, verilog net list and its constraints are taken as benchmarks to evaluate the performance.the simulation is carried out in Cadence Digital Encounter. PD1,PD2 and PD3 are the different power domains here the three different voltage is applied they voltage are 0.9,1.8,1.6 the table1 and 2 shows the optimized results of the SKB-Tree. The performance of SKB tree is tested for varying density of number of modules inside the power domains.It is observed from the results that varying the density of elements there is no change in the performance.

The figure 3 is layout of Sayeh processor with Set-A, figure 4 is layout of lambada processor for Set-B, figure 5 is layout of Sayeh processor for Set-B.

Table I
Power and Delay for Sayeh Processor

circuit	*Set A*			*Set B*		
	No. of elements	*Power*	*Delay*	*No. of elements*	*Power*	*Delay*
Sayeh	PD1 = default	0.236	509.3(ps)	PD1 =defult	0.056	509.3(ps)
	PD2=(10)	1.515		PD2=4	0.57	
	PD3=(4)	0.75		PD3=10	1.159	

VI. CONCLUSION

In this paper we have proposed SKB-tree floorplanning compared to the normal floorplanning it gives the optimized power, level shifter planning is easier and gives very low dead- space in the fixed-outline floorplanning.

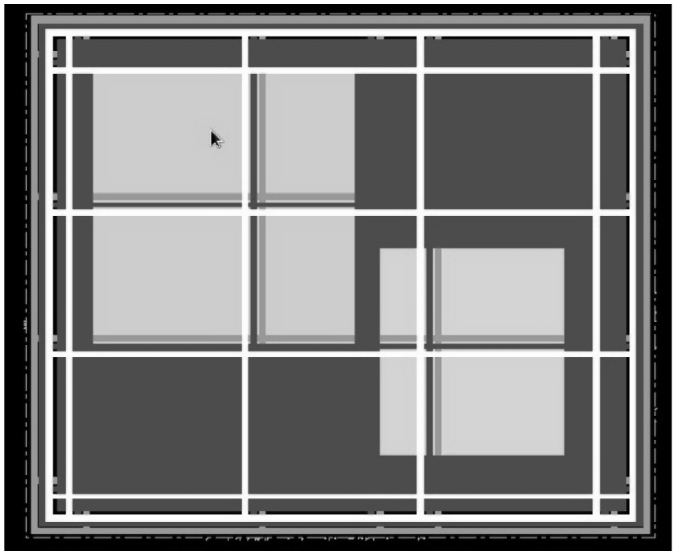

Figure 3: layout of Sayeh processor for set-A

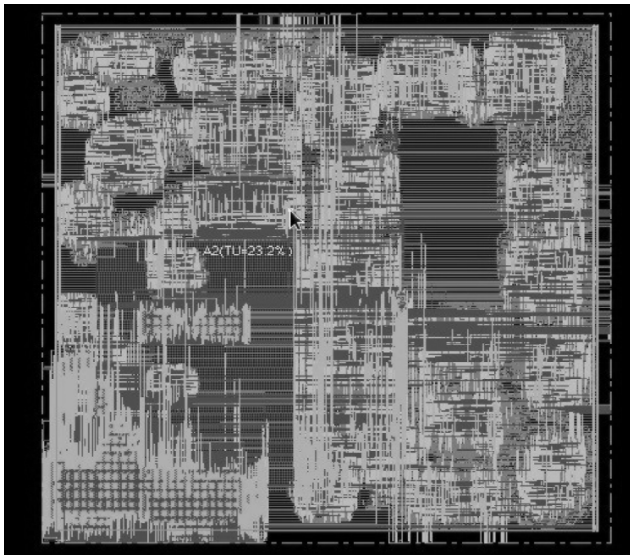

Figure 4: layout of Lambda processor for set-B

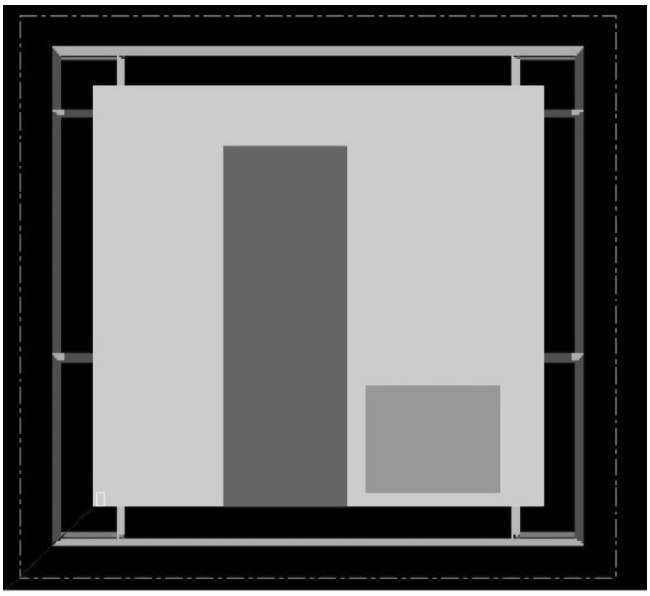

Figure 5: layout of Sayeh processor for set-B

Table II
Power and Delay for Lambda Processor

Circuit	*Set A*			*Set B—*		
	No. of elements	*Power (mW)*	*Delay*	*No. of elements*	*Power (mw)*	*Delay*
lambda	PD1= default	128.9		PD1= default	137.9	
	PD2 = 6	10.84	14ns	PD2 = 4	9.86	14ns
	PD3 = 3	27.86		PD3= 5	18.32	

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