Single VDBA based Multifunction Filter

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Abstract: In this paper single voltage differencing buffered ampliûer (VDBA) based multifunction ûlter topology that provides low pass (LP), band pass (BP), and high pass (HP) filter functions has been presented. The configuration is suitable for implementing high quality factor filters with low component spread. The working of realized filter topology is verified through SPICE simulation for which the VDBA is implemented using 0.18μm CMOS technology. The simulation results are observed to be in close agreement with the results obtained from the theoretical calculations.

Keywords: Multifunction Filter, VDBA, Analog building block

1. INTRODUCTION

Filters are substantial blocks, widely used in many integrated circuits such as radio-frequency applications, data conversion in A/D, D/A systems [1] and many others. The filters can be designed using conventional voltage mode Op-Amps. However, these configurations exhibit limitations in their performance due to the low slew rate and constant gain-bandwidth product [2]. A number of analog building blocks (ABB) such as such as current differencing buffered amplifier (CDBA) [3], differential difference current conveyor (DDCC) [4], current differencing transconductance amplifier (CDTA) [5], second generation current conveyor (CCII) [6] , differential voltage current conveyor (DVCC) [7], Operational Transconductance Amplifiers (OTAs) [8] and many others as listed in [2] have been reported in literature to overcome the limitations Op-Amp based circuits .However, all these blocks process current signals only. The voltage differencing buffered amplifier (VDBA) is an alternate ABB which not only is free from slew limitation but also processes the voltage signals. As the name suggests the VDBA uses voltage differencing input stage and provides a current output, given by the product of the differential input voltage and transconductance gain. The transconductance being the bias current dependent enables electronic tuning of circuit parameters [9]. This results in simpler circuit design with lesser passive component count. It also provides a buffered voltage output which results in easily cascadable structures [10]. Additionally, since the VDBA provides both voltage and current outputs it further enhances the design flexibility [11]. Thus the VDBA has evolved as a promising choice for analog applications.

An exhaustive literature review suggests that the VDBA and its variants have been used for realizing a variety of analog filters [9-20]. Available literature on filters can be classified as single input multiple outputs (SIMO) [10-12] multiple input single output (MISO) [9,15-17] and single input single output (SISO) [13-14,18-20].The available VDBA based filters with their prominent features have been listed in Table 1. It may be observed from Table 1 that all single VDBA based SISO filters provide only one type of filter response. Also these structures do not provide high pole quality factor (Q_o) with moderate component spread which is a desirable condition for integrated applications. To fill this research gap in this paper a new generalized second order multifunction SISO filter topology is proposed which employs single VDBA, two capacitors and three resistors. The proposed topology can be used to realize three filter functions namely, low pass (LP), band pass (BP), and high pass (HP), through appropriate component selections. The added attraction of the proposed topology is that it does not put any component matching constraint on the design. The proposed topology is suitable for high Q_0 filter implementation with moderate component spread.

The remaining organization of the paper is as follows: Section 2 presents the description of the proposed configuration. The sensitivity analysis is presented in section 3. The effect of non-idealities of VDBA has been dealt with in section 4. The SPICE simulation results for verification of the proposed topology are placed in section 5 followed by conclusion in section 6.

Table 1
Comparison of the proposed work with the previously reported work

Ref. No.	ABB	No of ABBs	Type	Standard filter Function	Mode	Passive Components (R+C)	Independent ω_o and Q_o	Technology used for ABB
[14]	VDIBA	1	SISO	AP	VM	0+1	-	OPA860
[15]	VDIBA	1	MISO	LP, BP, HP, AP, BS	VM	1+2	YES	CMOS
[9]	VDBA	2	MISO	LP, BP, HP, AP, BS	VM	0+2	NO	CMOS
	VDBA	2	MISO	LP, BP, HP, AP, BS	VM	1+2	YES	CMOS
[16]	VDIBA	1	MISO	LP, BP, HP, AP, BS	VM	1+2	YES	OPA 860+AD830
[17]	VDIBA	2	MISO	LP, BP, HP, AP, BS	VM	0+2	YES	FGMOS
[12]	ZC-VDBA	2	SIMO	LP, BP, HP	CM	0+2	YES	CMOS
[13]	VDBA	N	SISO	AP	VM	(0+N-1)	YES	BiCMOS
[18]	FB-VDBA	1	SISO	AP	VM	1+1	-	OPA860
[11]	VDBA	3	SIMO	HP, BP, LP	VM	0+2	YES	CMOS
[10]	FB-VDBA	2	SIMO	HP, BP, LP	VM	4+2	YES	OPA860
[19]	VDBA	1	SISO	BP	VM	2+2	-	OPA860
[20]	FB- VDBA	1	SISO	AP	VM	1+1	-	BiCMOS
Proposed work	VDBA	1	SISO	LP, HP, BP	VM	3+2	YES	CMOS

2. THE PROPOSED CIRCUIT

The schematic symbol of the VDBA is shown in Figure 1. It has a pair of high-impedance voltage inputs V_p and V_n, a high-impedance current output z and low-impedance voltage output w. The input stage of VDBA can be easily implemented by differential amplifier, which converts the input voltage to output current that ûows out of the z terminal. The output stage can be formed by unity gain voltage buffer. The ideal VDBA terminal equations are defined as

$$\begin{bmatrix} I_p \\ I_n \\ I_z \\ V_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_p \\ V_n \\ V_z \\ I_w \end{bmatrix} \tag{1}$$
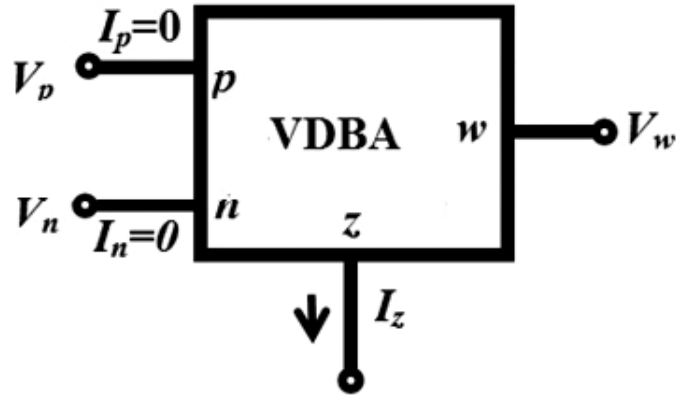
Figure 1: Schematic symbol of the VDBA.

The proposed filter topology is shown in Figure 2. The voltage transfer function of the proposed configuration using routine circuit analysis may be obtained as
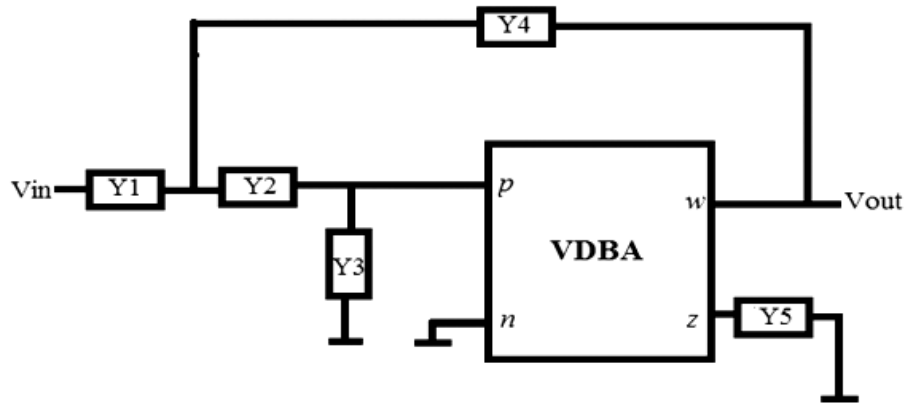

Figure 2: The proposed topology

$$\frac{Vo}{Vin} = \frac{KY_1 Y_2}{Y_1 Y_2 + Y_1 Y_3 + Y_2 Y_3 + Y_2 Y_4 + Y_3 Y_4 - KY_2 Y_4}, \tag{2}$$

Where

$$K = \frac{g_m}{Y_5}, \tag{3}$$

The appropriate admittance choices would result in three required filter responses, as listed in Table 2.

Table 2
Admittance Selection for Proposed Filter Topology

Response type	Y_1	Y_2	Y_3	Y_4	Y_5
LP	G_1	G_2	sC_3	sC_4	G_5
HP	sC_1	sC_2	G_3	G_4	G_5
BP	G_1	sC_2	$G_3 + sC_3$	G_4	G_5

For the admittance choices available in Table.2, the transfer function for LP, HP and BP can be expressed as:

$$\left(\frac{V_O}{V_{in}}\right)_{LP} = \frac{K\dfrac{G_1 G_2}{C_3 C_4}}{s^2 + s\left(\dfrac{C_3(G_1+G_2)+G_2 C_4(1-K)}{C_3 C_4}\right) + \dfrac{G_1 G_2}{C_3 C_4}} \tag{4}$$

$$\left(\frac{V_O}{V_{in}}\right)_{HP} = \frac{Ks^2}{s^2 + s\left(\dfrac{G_3(C_1+C_2)+G_4 C_2(1-K)}{C_1 C_2}\right) + \dfrac{G_3 G_4}{C_1 C_2}} \tag{5}$$

$$\left(\frac{V_O}{V_{in}}\right)_{BP} = \frac{Ks\dfrac{G_1}{C_3}}{s^2 + s\left(\dfrac{C_3(G_1+G_4)+C_2(G_1+G_3)+G_4 C_2(1-K)}{C_2 C_3}\right) + \dfrac{G_3(G_1+G_4)}{C_2 C_3}} \tag{6}$$

The resonant angular frequency (ω_o), quality factor (Q_o) and filter gain (H_o) for the three filters may be obtained from equation (4-6) are listed in Table 3.

Table 3
Parameters of the proposed topology

Filter Type	ω_o	Q_o	H_o
LP	$\sqrt{\dfrac{G_1 G_2}{C_3 C_4}}$	$\dfrac{\sqrt{C_4 C_3(G_1 G_2)}}{C_3(G_1+G_2)+G_2 C_4(1-K)}$	K
HP	$\sqrt{\dfrac{G_3 G_4}{C_1 C_2}}$	$\dfrac{\sqrt{C_1 C_2(G_3 G_4)}}{G_3(C_1+C_2)+G_4 C_2(1-K)}$	K
BP	$\sqrt{\dfrac{G_3(G_1+G_4)}{C_2 C_3}}$	$\dfrac{\sqrt{C_2 C_3 G_3(G_1+G_4)}}{C_3(G_1+G_4)+C_2(G_1+G_3)+G_4 C_2(1-K)}$	$\dfrac{G_1 C_2}{C_3(G_1+G_4)+C_2(G_1+G_3)+G_4 C_2(1-K)}$

Table 4 lists the filter parameters for all the three responses when all the conductance except G_5 are set equal to G and all capacitors are set equal to C. It may be observed from the Table 4 that ω_o can be set using appropriate G and C values and the desired Q_o can be obtained with the help of G_5 thereby making tuning independent.

Table 4
Filter Parameters for Equal Component Design

Filter Type	ω_o	Q_o	H_o
LP	G/C	1/(3-K)	K
HP	G/C	1/(3-K)	K
BP	√2G/C	√2/(5-K)	K/(5-K)

3. SENSITIVITY ANALYSIS

The derived passive sensitivities of ω_o and Q_o for the proposed filter configurations are summarized in Table 5.

Table 5
Passive Sensitivities

Filter Type	*Passive Component*	ω_o	Q_o
LP	G_1	$\dfrac{1}{2}$	$\dfrac{1}{2} - \dfrac{C_3 G_1}{C_3(G_1+G_2)+G_2 C_4(1-K)}$
	G_2	$\dfrac{1}{2}$	$\dfrac{1}{2} - \dfrac{C_3 G_2 + C_4 G_2(1-K)}{C_3(G_1+G_2)+G_2 C_4(1-K)}$
	C_3	$-\dfrac{1}{2}$	$\dfrac{1}{2} - \dfrac{C_3(G_1+G_2)}{C_3(G_1+G_2)+G_2 C_4(1-K)}$
	C_4	$-\dfrac{1}{2}$	$\dfrac{1}{2} - \dfrac{C_4 G_2(1-K)}{C_3(G_1+G_2)+G_2 C_4(1-K)}$
HP	C_1	$-\dfrac{1}{2}$	$\dfrac{1}{2} - \dfrac{C_1 G_3}{G_3(C_1+C_2)+G_4 C_2(1-K)}$
	C_2	$-\dfrac{1}{2}$	$\dfrac{1}{2} - \dfrac{C_2(G_3+G_4(1-K))}{G_3(C_1+C_2)+G_4 C_2(1-K)}$
	G_3	$\dfrac{1}{2}$	$\dfrac{1}{2} - \dfrac{G_3(C_1+C_2)}{G_3(C_1+C_2)+G_4 C_2(1-K)}$
	G_4	$\dfrac{1}{2}$	$\dfrac{1}{2} - \dfrac{G_4 C_2(1-K)}{G_3(C_1+C_2)+G_4 C_2(1-K)}$
BP	G_1	$\dfrac{1}{2} - \dfrac{1}{2}\dfrac{G_3 G_4}{G_3(G_1+G_4)}$	$\dfrac{1}{2}\dfrac{G_1}{(G_1+G_4)} - \dfrac{G_1(C_2+C_3)}{C_3(G_1+G_4)+C_2(G_1+G_3)+G_4 C_2(1-K)}$
	G_3	$\dfrac{1}{2}$	$\dfrac{1}{2} - \dfrac{G_3 C_2}{C_3(G_1+G_4)+C_2(G_1+G_3)+G_4 C_2(1-K)}$
	G_4	$\dfrac{1}{2} - \dfrac{1}{2}\dfrac{G_3 G_1}{G_3(G_1+G_4)}$	$\dfrac{1}{2}\dfrac{G_4}{(G_1+G_4)} - \dfrac{G_4(C_3+C_2(1-K))}{C_3(G_1+G_4)+C_2(G_1+G_3)+G_4 C_2(1-K)}$
	C_2	$-\dfrac{1}{2}$	$\dfrac{1}{2} - \dfrac{C_2(G_1+G_3)+G_4 C_2(1-K)}{C_3(G_1+G_4)+C_2(G_1+G_3)+G_4 C_2(1-K)}$
	C_3	$-\dfrac{1}{2}$	$\dfrac{1}{2} - \dfrac{C_3(G_1+G_4)}{C_3(G_1+G_4)+C_2(G_1+G_3)+G_4 C_2(1-K)}$

From the results in Table 5 it is evident that the filter configurations are insensitive to parameter variations as passive sensitivities are low and not larger than 0.5 in magnitudes.

4. NON- IDEALITY ANALYSIS

This section discusses the effect of non-idealities over the performance of the proposed topology. The non-ideal model of the VDBA [18] is depicted in Figure 3. Z_p and Z_n are the parasitic impedances of input terminals p and n, and Z_z and Z_W are the parasitic impedances of output terminals z and w terminals resp.

In presence of these non-idealities the transfer functions may be obtained as
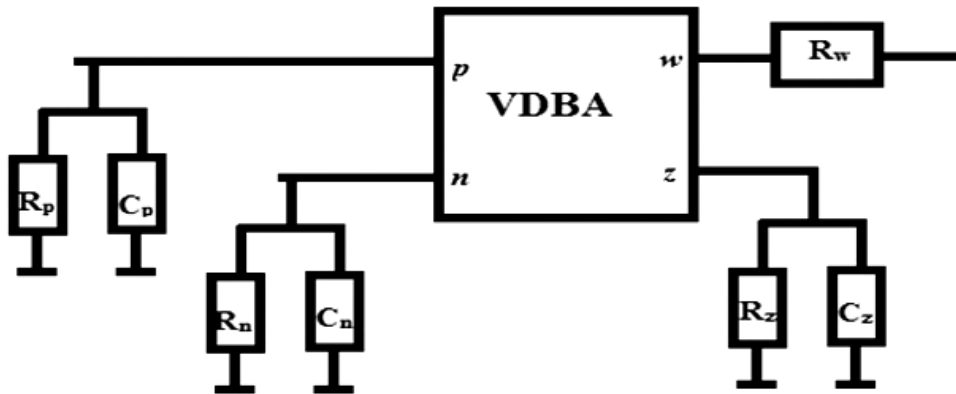

Figure 3: Non Ideal model of VDBA [18]

$$\left(\frac{V_o}{V_{in}}\right)_{LPn} = \frac{G_1 G_2 \frac{g}{(G_5 + G_z + sC_z)}}{s^2 \frac{C_4 * G_w}{sC_4 + G_w}(C_3 + C_p) + (\frac{sC_4 * G_w}{sC_4 + G_w})(G_1 + G_2 + G_p) + s(C_3 + C_p)G_2(1 - \frac{g}{(G_5 + G_z + sC_z)}) + G_1 G_2 + G_p G_2(1 - \frac{g}{(G_5 + G_z + sC_z)})} \quad (7)$$

$$\left(\frac{V_o}{V_{in}}\right)_{HPn} = \frac{C_1 C_2 s^2 \frac{g}{(G_5 + G_z + sC_z)}}{s^2(C_1 C_2 + C_1 C_p + C_2 C_p) + s(C_1 + C_2)(G_3 + G_p) + s\frac{G_4 * G_w}{G_4 + G_w}(C_2 - \frac{C_2 g}{(G_5 + G_z + sC_z)} + C_p) + \frac{G_4 * G_w}{G_4 + G_w}(G_3 + G_p)} \quad (8)$$

$$\left(\frac{V_o}{V_{in}}\right)_{BPn} = \frac{sC_2 G_1 \frac{g}{G_5 + G_z + sC_z}}{s^2 C_2(C_3 + C_p) + sC_2(G_1 + G_3 + G_p) + s(C_3 + C_p)(G_1 + \frac{G_4 * G_w}{G_4 + G_w}) + sC_2\frac{G_4 * G_w}{G_4 + G_w}(1 - \frac{g}{(G_5 + G_z + sC_z)}) + (G_3 + G_p)(G_1 + \frac{G_4 * G_w}{G_4 + G_w})} \quad (9)$$

It is clear from equations (7-9) that non idealities of VDBA introduce parasitic poles and zeros in the transfer function causing some discrepancies from the ideal behaviour. However since $Y_3 >> (G_p + sC_p)$, $G_5 >> (G_z + sC_z)$ and $Y_4 << G_w$ therefore these deviations may be rendered ineffective.

5. SIMULATION RESULTS

To validate the results obtained from the theory, the proposed filter topology has been simulated using PSPICE. For simulations, the VDBA was implemented using CMOS [9], as shown in Figure 4. Table 6 shows the transistors aspect ratios. SPICE simulations are carried out using supply voltages of ±0.9V.

Table 6
W/L ratios

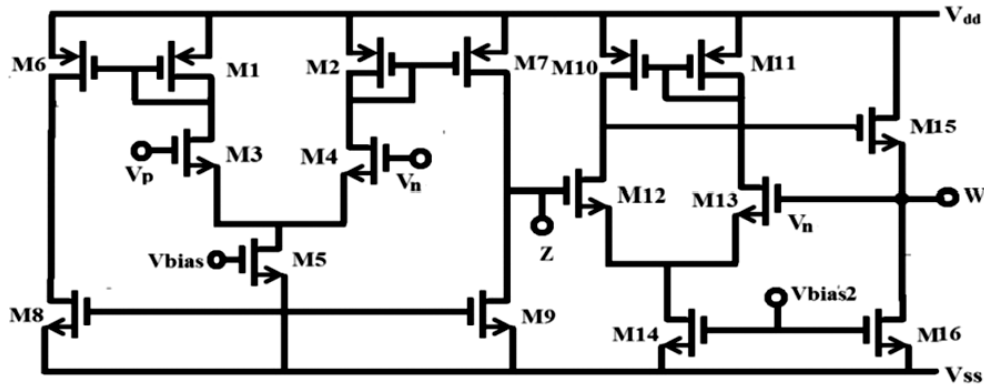| Sr. No	Transistors	W(µm)/L(µm)
1	M1-M4	20/1
2	M5	5/1
3	M6-M7	30/1
4	M8-M9	10/1
5	M10-M11, M15	40/1
6	M12-M13, M14, M16	20/1

Figure 4: CMOS structure of VDBA [9]

The LP, HP and BP filter configurations were designed to give Butterworth response for an f_o of 1.59MHz. Component values chosen for various responses are listed in Table 7.

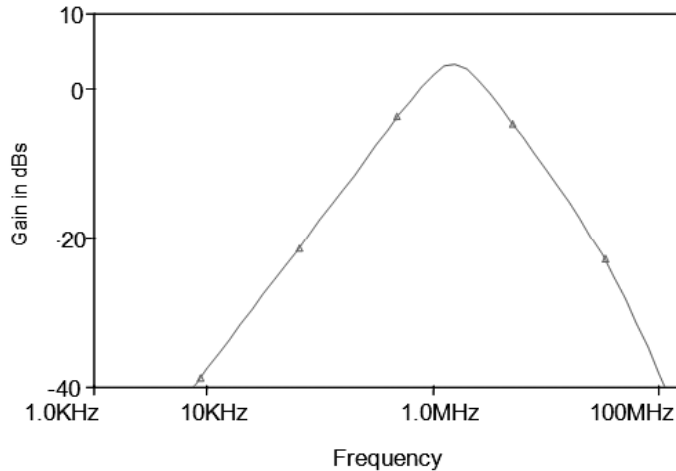**Table 7**
Component Values Chosen for Various Responses

Response type	Resistance Values (kΩ)		CapacitanceValues (nF)
LP	$R_1 = R_2 = 10$	$R_5 = 13.32$	$C_4 = C_5 = 0.01$
HP	$R_3 = R_4 = 10$	$R_5 = 13.32$	$C_1 = C_2 = 0.01$
BP	$R_1 = R_3 = R_4 = 14.14$	$R_5 = 25.52$	$C_2 = C_4 = 0.01$
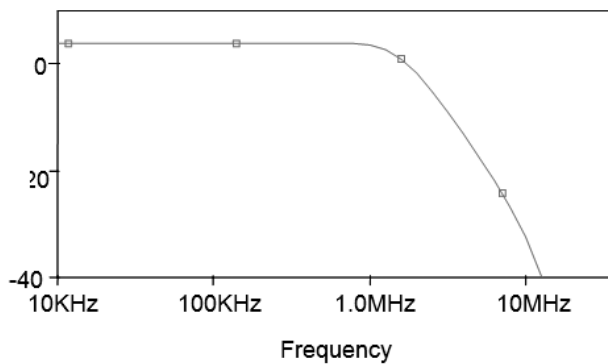
(a)
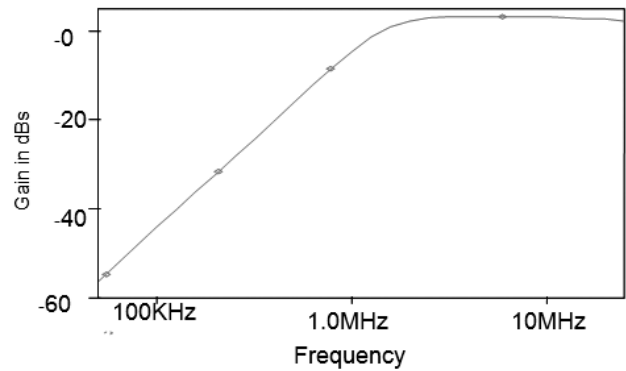
(b)

(c)

Figure 5: Frequency Responses of Proposed (a) LP Filter (b) HP Filter (c) BP Filter

The simulated frequency responses of all the three configurations are shown in Figures.5 (a), (b) and (c) respectively. The simulated f_o is observed to be 1.57 MHz in case of LP and BP whereas in HP it is found to be 1.50MHz. The simulated values are in close agreement to the theoretical frequency of 1.59MHz.

To show the tuning of f_o, BP responses are plotted for three different values of f_o while keeping Q_o fixed at 0.707 as depicted in Figure 6(a).The components chosen for the same are listed in Table 8.

Table 8
Component values used for f_0 tunability

| f_o | Components | | | |
	$R_1=R_2=R_3;$	R_5	$C_3=C_4$	Q_o
.795MHz	14.14KΩ	25.2 KΩ	0.02nF	0.707
1.59MHz	14.14KΩ	25.2 KΩ	0.01nF	0.707
3.18MHz	14.14KΩ	25.2 KΩ	0.005nF	0.707

The independent tunability of Q_o with R_5 is shown in Figure 6(b). The center frequency f_o is taken to be 1.59MHz. The component values chosen and the Q_o so obtained are given in Table 9. It may also be observed from the Table 9 that a small change in R_5 results in large variation in Q_o value.

Table 9
Component values used for independent tunability of Qo

| f_o | Components | | | |
	$R_1=R_2=R_3$	$C_4=C_3$	R_5	Q_0
1.59MHz	14.14KΩ	0.01nF	30.156 KΩ	1
1.59MHz	14.14KΩ	0.01nF	40.18 KΩ	10
1.59MHz	14.14KΩ	0.01nF	41.74 KΩ	50

The performance of proposed filter topology is also evaluated through well known Monte Carlo statistical analysis. For this purpose, LP, HP and BP filters are simulated by setting the values of all passive elements in 5% tolerance. The simulated standard deviation of f_0 is observed to be 37.712 KHz, 76.7 KHz and 66.4 KHz for BP,
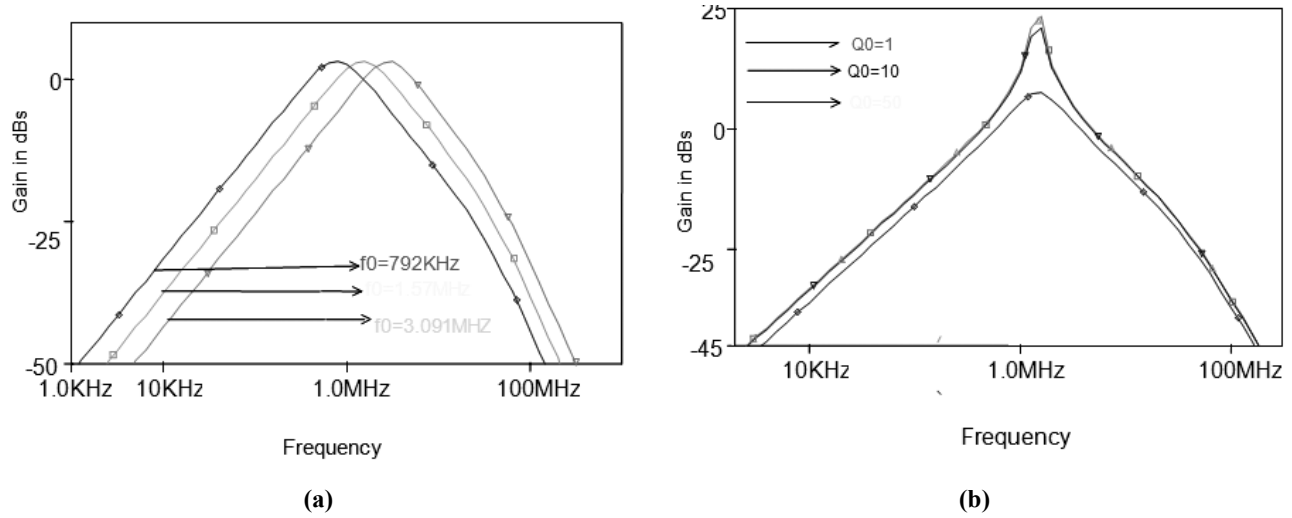
(a)   (b)

Figure 6: BP response depicting independent tunabilityof (a) f_o (b) Q_o
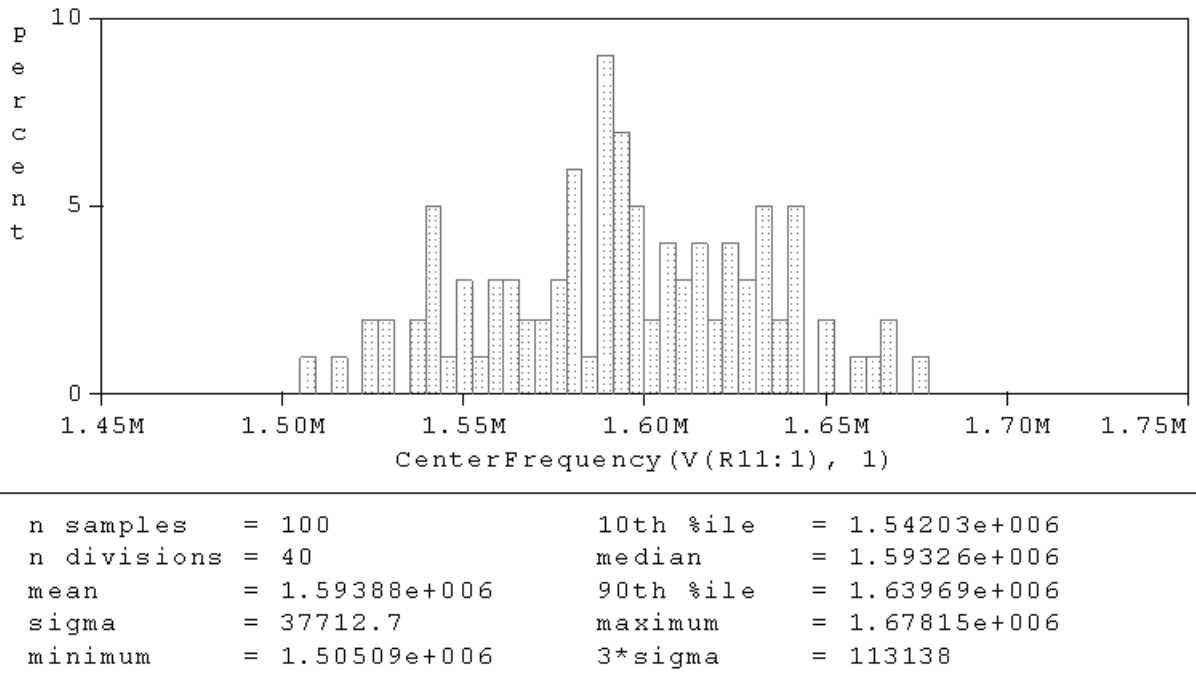

Figure 7: Monte Carlo statistical results BP Filter

LP and HP configuration respectively. This implies that the proposed filter topology has reasonable sensitivity characteristics. For the sake of brevity the derived histogram after 100 simulation runs for BP filter only is shown in Figure 7.

6.   CONCLUSION

A new voltage mode single VDBA based generalized filter topology is presented in this paper. The configuration can be used to synthesize LP, HP and BP filters with appropriate choices of admittance. The proposed configuration is a suitable choice for high quality factor implementation. Passive sensitivities for the configuration are found to be low. Extensive SPICE simulations using 0.18 µm CMOS technology are carried out to observe the

performance of the proposed configuration. The simulation and theoretical results are found in close agreement thus verifying the proposition.

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