IJCTA
Vol.8, No.1, Jan-June 2015, Pp.140-148

Two New First Order All Pass Filters Based on Differential Difference Complementary Current Conveyor

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ABSTRACT

The aim of this paper is to analyze two new all-pass filters which provide better gain as well as phase response at high and low frequencies, using optimum number of passive components with no need for matching of elements. The proposed filters are of first-order and employ Differential Difference Complementary Current Conveyor (DDCCC) as active element. The first proposed topology is using one DDCCC, one grounded resistor and one floating capacitor. Second proposed topology is using one DDCCC, one grounded capacitor and one floating resistor. The theoretical results are verified with SPICE simulation using model parameters of 0.5 μm CMOS process. These configurations are suitable for very large scale integration (VLSI) realization and find applications in high-Q band-pass filters, phase modulators, quadrature oscillators and multiphase oscillators.

Index terms: Current conveyor; CCII; DDA; DDCC±; DDCCC; all-pass filter; SPICE,

1. INTRODUCTION

Current conveyor offers an alternative way of abstracting complex circuit function into easier one. So, from the recent past, researchers are paying attention on current conveyor for developing an application either through-current mode or voltage-mode approach. It is also popular due to its high performance, low power consumption, high bandwidth, high output voltage swing and functional versatility [1]-[11]. But there is a drawback with CCII. It has only one input voltage terminal. This paper used DDCCC as an active element which offers the combined features of CCII and DDA like high-input impedance and arithmetic operation capability. So DDCCC has now become a versatile basic building block for realization of amplifiers, filters, and oscillators [11].

This paper concentrated on all-pass filters. All-pass filters are used to correct any phase shifts occurring due to the operation of analog filters, without altering the amplitude of input signal. They are also used in the design of quadrature and multiphase oscillators [4]-[9], [11]-[14]. Recently, many all-pass filters have been proposed. Some of them have CCI or CCII as an active element [8], [13]-[15]. Some have passive component matching restrictions [4-6], [11], [15]-[18]. Some used more number of active elements or passive elements [7, 13, 15]. Some used floating capacitor which is

not suitable in fabrication point of view [5, 6, 12, 13]. All the above DDCC based all-pass networks used either DDCC+ or DDCC-. In this paper we are using DDCC as a single unit called Differential Difference Complementary Current Conveyor (DDCCC) [10, 11, 17].

2. DDCCC FUNDAMENTALS

The symbol of six-port DDCCC is shown in Fig. 1. The internal structure of this device is shown in Fig. 2. It can be characterized by the following matrix-relation between various voltage and current variables [18]-[20].

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ V_X \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ \beta_1 & -\beta_2 & \beta_3 & 0 & 0 & 0 \\ 0 & 0 & 0 & \alpha_1 & 0 & 0 \\ 0 & 0 & 0 & 0 & \alpha_2 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \\ -I_X \\ V_Z \end{bmatrix} \quad (1)$$

In the DDCCC, Y_1, Y_2, and Y_3 are three voltage input terminals with high input impedance. X is a low impedance current input terminal. Z+ and Z- are two high impedance current output terminals. The hybrid matrix can be represented by the following equations:

$$I_{Y1} = I_{Y2} = I_{Y3} = 0,\ V_X = \beta_1 V_{Y1} - \beta_2 V_{Y2} + \beta_3 V_{Y3},\ I_{Z+} = \alpha_1 I_X \text{ and } I_{Z-} = -\alpha_2 I_X \quad (2)$$

Here α_1 and α_2 represent the current tracking errors from X to Z+ and Z- terminals respectively. β_1, β_2 and β_3 represent the voltage tracking errors from Y_1, Y_2, Y_3 to X terminal. Ideally $\beta_1 = \beta_2 = \beta_3 = \alpha_1 = \alpha_2 = 1$. Actually these tracking errors arise due to parasitic capacitance and resistance of the DDCCC.

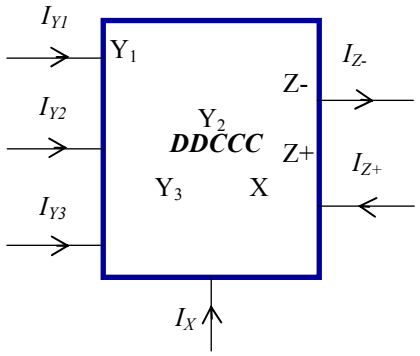

Figure 1: Symbol for DDCC

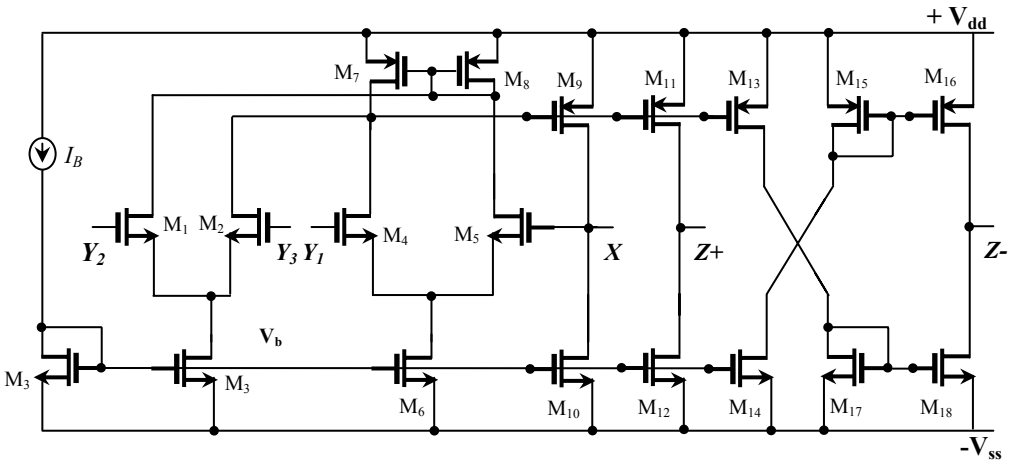

Figure 2: Device level presentation of DDCCC

3. PROPOSED DESIGN

To improve the circuit performance, the proposed topology has floating element. The first topology shown in Fig. 3 has one grounded resistor connected to Y_2 terminal and one floating capacitor connected between input and output terminals. The floating capacitor by-passes the active element completely. If we analyze the circuit at high frequencies, we see that capacitor will become short circuit at $V_i = V_0$. Ideally, its voltage transfer function is given by

$$\frac{V_o(s)}{V_i(s)} = \frac{sCR-1}{sCR+1} \tag{3}$$

It provides 180^0 to 0^0 phase shift. And the phase response is given by

$$\phi(\omega) = 180^0 - 2\tan^{-1}(\omega CR) \tag{4}$$

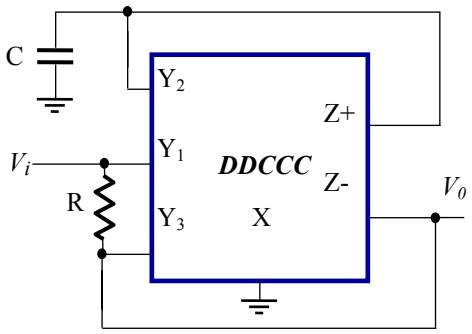

Figure 3: Proposed all-pass filter with grounded resistor

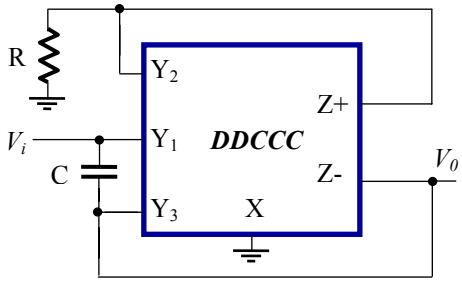

Figure 4: Proposed all-pass filter with grounded capacitor

The second topology shown in Fig. 4 has one grounded capacitor and a floating resistor is connected between input and output terminals. Ideally its voltage transfer function is given by

$$\frac{V_o(s)}{V_i(s)} = \frac{1 - sCR}{1 + sCR} \tag{5}$$

It provides 0^0 to 180^0 phase shift. Its phase response is given by

$$\phi(\omega) = -2\tan^{-1}(\omega CR) \tag{6}$$

4. NON-IDEAL ANALYSIS

Due to grounded X terminal, the intrinsic resistance at terminal X does not affect the circuit performance or the filter pole [8]. Here we took in to account the tracking errors and calculated the gain and phase response.

From Fig. 3, we can write voltage transfer function as

$$\frac{V_o(s)}{V_i(s)} = \frac{\alpha_2\beta_2 sCR - \alpha_1\beta_3}{\alpha_2\beta_2 sCR + \alpha_1\beta_1} \tag{7}$$

and phase response as

$$\phi(\omega) = 180^0 - \tan^{-1}\frac{\alpha_2\beta_2\omega CR}{\alpha_1\beta_3} - \tan^{-1}\frac{\alpha_2\beta_2\omega CR}{\alpha_1\beta_1} \tag{8}$$

From Fig. 4, we can write voltage transfer function as

$$\frac{V_o(s)}{V_i(s)} = \frac{\alpha_2\beta_2 - \alpha_1\beta_3 sCR}{\alpha_2\beta_2 + \alpha_1\beta_1 sCR} \tag{9}$$

and the phase response as

$$\phi(\omega) = -\tan^{-1}\frac{\alpha_1\beta_3\omega CR}{\alpha_2\beta_2} - \tan^{-1}\frac{\alpha_1\beta_1\omega CR}{\alpha_2\beta_2} \tag{10}$$

Effects Of Non-Ideality On Pole Frequency:

Ideally, from Eqs. (2) and (4), we can observe that the pole/zero frequency will be $\omega_{p/z} = 1/RC$ and its sensitivity due to passive element is $S_{R,C}^{\omega_{P/Z}} = 1$. From Eqs. (4) and (5) we can observe that the pole frequency is different from the zero frequency and it is given by the following characteristic equations.

For Fig. 3, $\omega_P = \alpha_1\beta_1/\alpha_2\beta_2 RC$, $\omega_Z = \alpha_1\beta_3/\alpha_2\beta_2 RC$ and

For Fig. 4, $\omega_P = \alpha_2\beta_2/\alpha_1\beta_1 RC$, $\omega_Z = \alpha_2\beta_2/\alpha_1\beta_3 RC$

After analysis we found that the sensitivity of pole or zero frequency due to DDCCC is not more than unity. The sensitivities for Fig. 3 are given by

$$\left|S_{\alpha_1\alpha_2\beta_1\beta_2}^{\omega_P}\right| = 1 \tag{11}$$

$$\left|S_{\alpha_1\alpha_2\beta_2\beta_3}^{\omega_z}\right| = 1 \tag{12}$$

and for Fig. 4, they are given by

$$\left|S_{\alpha_1\alpha_2\beta_1\beta_2}^{\omega_P}\right| = 1 \tag{13}$$

$$\left|S_{\alpha_1\alpha_2\beta_2\beta_3}^{\omega_z}\right| = 1 \tag{14}$$

5. SIMULATION RESULTS

The proposed all-pass filters were simulated using PSPICE with 0.5 µm MITEC parameters. The parameters are given in table 1 and the aspect ratios of transistors are given in table 2.

Table 1. 0.5 µm MIETEC CMOS process model parameters; LEVEL-3.

MODEL NT NMOS LEVEL=3
+UO=460.5 TOX=1.0E-8 TPG=1 VTO=.62 JS=1.8E-6+XJ=.15E-6 RS=417 RSH=2.73 LD=0. ETA=0+VMAX=130E3 NSUB=1.71E17 PB=.761 PHI=0.905+THETA=0.129 GAMMA=0.69 KAPPA=0.1 AF=1+WD=.11E-6 CJ=76.4E-5 MJ=0.357CJSW=5.68E-10+MJSW=0.302 CGSO=1.38E-10 CGDO=1.38E-10+CGBO=3.45E-10 KF=3.07E-29 DELTA=0.42+NFS=1.2E11
MODEL PT PMOS LEVEL=3
+UO=100 TOX=1.0E-8 TPG=1 VTO=-.58 JS=3.8E-6+XJ=.1E-6 RS=886 RSH=1.81 LD=0.03EETA=0+VMAX=115E3 NSUB=2.08E17 PB=.911PHI=0.905+THETA=0.120 GAMMA=0.76 KAPPA=2 AF=1+WD=.14E-6 CJ=85E-5 MJ=0.429 CJSW=4.67E-10 +MJSW=0.631 CGSO=1.38E-10 CGDO=1.38E-10+CGBO=3.45E-10 KF=1.08E-29 DELTA=0.81 +NFS=0.52E11

The supply voltages of proposed all-pass filter circuits are ±2.5 V and the biasing voltage V_B is -1.7 V. The simulation results of all-pass network shown in Fig. 3 are given in Fig. 5, Fig. 6 and Fig. 7 and those of all-pass network shown in Fig. 4 are given and Fig. 8 and Fig. 9. The passive component values selected are R=10 kΩ, C = 100 pF and the pole frequency f_0 = 159 KHz.

Table 2. Transistors Aspect Ratios.

TRANSISTOR	W (µm)	L (µm)
M_1, M_2, M_4, M_5	0.8	0.5
M_3, M_6	14.4	0.5
M_7, M_8	4.0	0.5
M_9, M_{11}, M_{13}, M_{15}, M_{16}	10.0	0.5
M_{10}, M_{12}, M_{14}, M_{17}, M_{18}	45.0	0.5

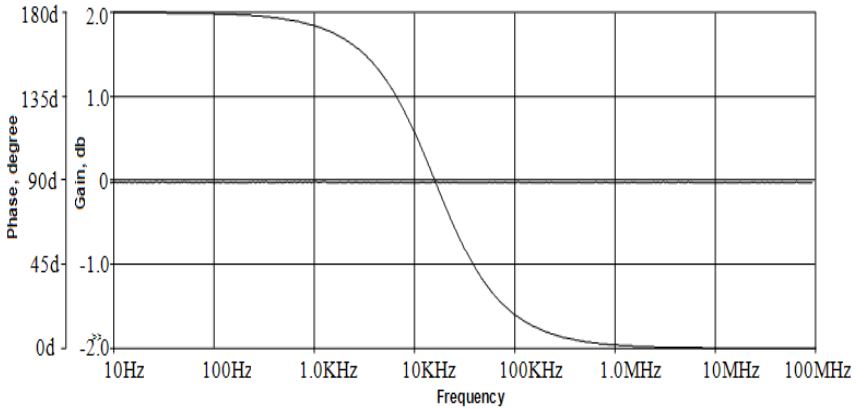

Figure 5: Phase and magnitude plots of the proposed circuit of Fig. 3 for R = 10 kΩ, and C= 100 pF

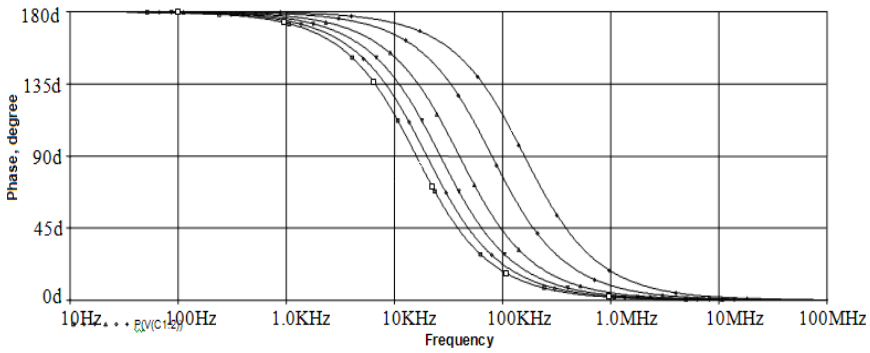

Figure 6: Phase plots of the proposed circuit of Fig. 3 for C= 100 pF and for different values of R (10 kΩ, 20 kΩ, 40 kΩ, 60 kΩ, 80 kΩ, 100 kΩ)

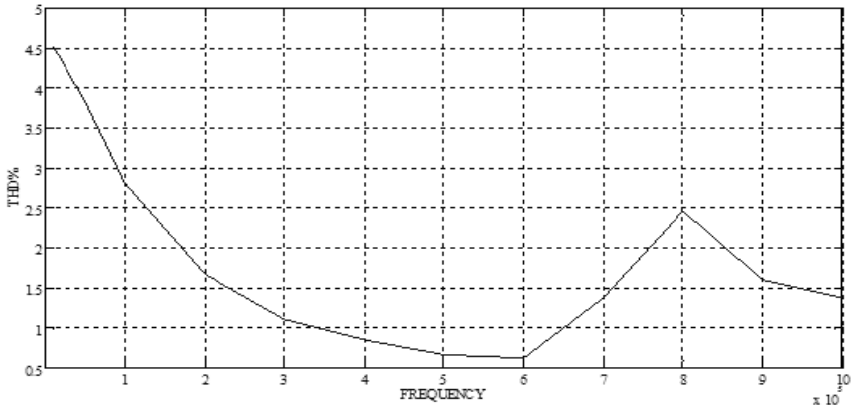

Figure 7: Dependence of output voltage harmonic distortion on input voltage frequency for 0.3 V (peak to peak) of the proposed all-pass filter of Fig. 3

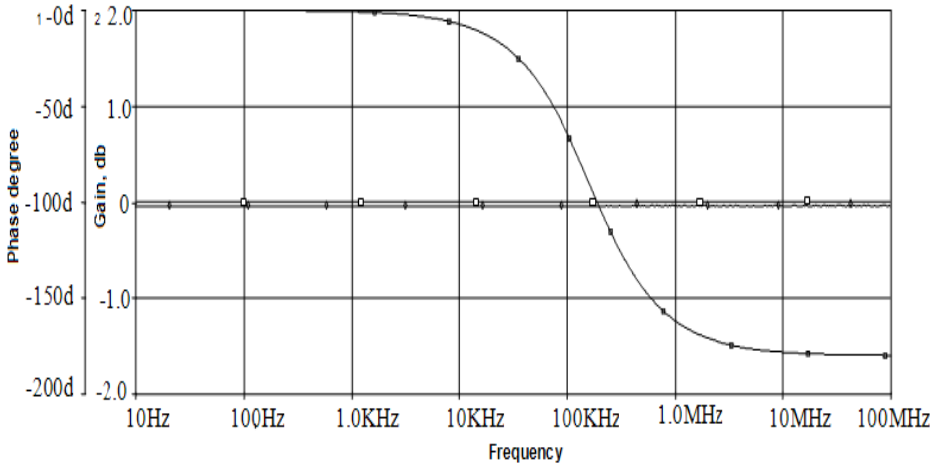

Figure 8: Phase and magnitude plots of the proposed circuit of Fig. 4 for R = 10 kΩ, and C= 100 pF

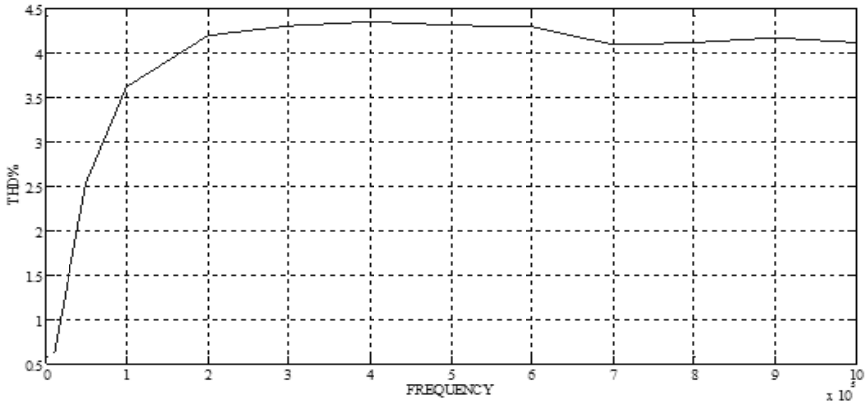

Figure 9: Dependence of output voltage harmonic distortion on input voltage frequency for 0.3 V (peak to peak) of the proposed all-pass filter of Fig. 4.

6. CONCLUSIONS

Two new DDCCC based all-pass filters are proposed. Both use optimum and canonical number of passive components. So there is no need for passive component matching. No capacitors are connected at X terminal. We found that Total Harmonic Distortion (THD) of both circuits is less than 5%. However its value is decreasing for first proposed circuit with increasing frequency and it is less than 2.5%. The first circuit has grounded resistor which provides the tunable property. It has a feed-forward capacitor that is connected between input and output. So it is suitable for high frequency operation [16]. The circuits are verified using SPICE simulation and the simulated results agreed with theoretical ones.

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