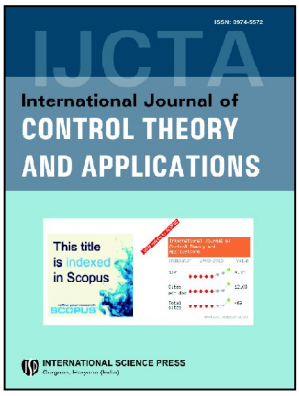

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A Review Article on Performance Comparison of CNTFET Based Full Adders

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Abstract: The paper pact with the full adder circuits in CNTFET technology. As it is the future technology which overcomes the limitations in the CMOS technology such as drain induced barrier lowering, short channel effects. The CNTFET technology has low power, high performance characteristics and also current carrying ability. It reduces the leakage power and the temperature effect on threshold voltage is small when compared with the CMOS technology. CNTFET device is similar to the CMOS device i.e., its channel is formed by CNTs. It works on the ballistic transport principle. It is an efficient device because of the chirality. Here the work is done on the full adders in CNTFET and its performance parameters such as propagation delay, power dissipation are considered for 0.9 v power supply and are compared. The full adder reduces the complexity. The performance parameters and the transient results of the CNTFET full adders are efficient and are simulated with 32nm technology in CADENCE software.***Keywords*:** CNTFET, Full Adders, Power Dissipation, Propagation Delay.

1. INTRODUCTION

The demand for scaling down increases as the technology grows. The CMOS technology has various false effects of scaling down such as short channel effects, hot carrier effect and drain induced barrier lowering to overcome these limitations a new device CNTFET has been introduced. It has the current [1] driving capability, reduces leakage power, high trans-conductance. Carbon nanotube field effect transistor (CNTFET) shown in Fig. 1 is the very effective technology and it is the future promising technology as it works on the principle of ballistic transport and the device structure is similar to CMOS device.

CNTFET uses a single or a group of CNTs as the channel material [2]. These were produced from a layer of graphite rolled into tubes called graphene. CNTs are of two groups namely SWCNT and MWCNT [3]. SWNTs comprises single graphene sheet is enfolded making a tube, whereas, MWNT consists of concentric tubes of graphene resembling a paper role. Among SWNT and MWNT, the former are considered to be more important owing to their electric properties.

In the CNT, channel region is undoped, whereas source and drain regions are doped heavily. By applying voltage to gate terminal the ID can be exact. The threshold voltage (V_{TH}) can be considered using (1).

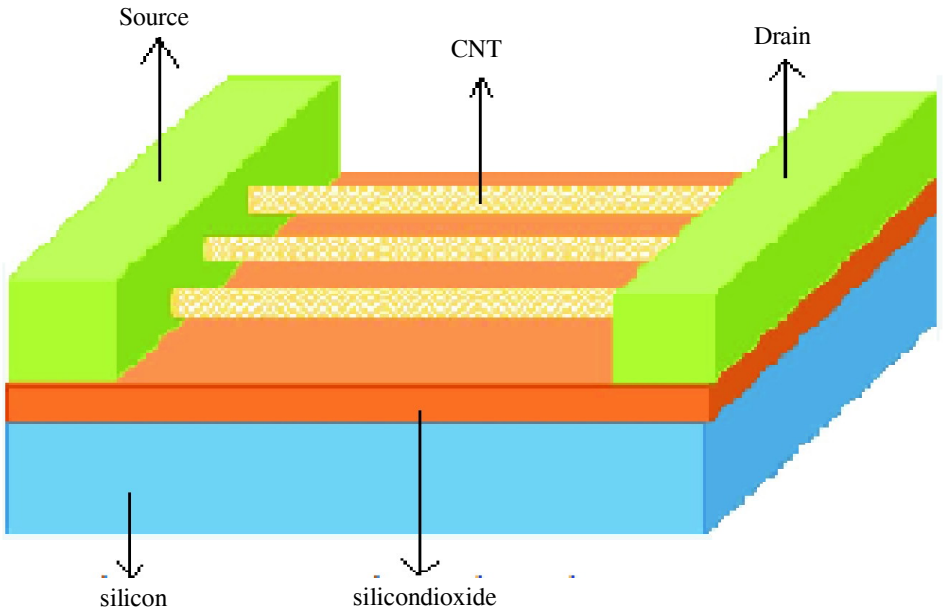

Figure 1: CNTFET Arrangement

$$V_{TH} = \frac{0.43}{D_{CNT}} \text{ (V)} \tag{1}$$

The electrical conductivity of carbon Nano tubes exhibits either metallic or semiconducting behavior based on chirality vector, relating to the arrangement of the graphene sheet, denoted by integers (n_1, n_2) which represent the number of unit vectors. For instance, CNT is metallic if $|n_1 - n_2| = 3K$ or $n_1 = n_2$. The nanotubes satisfying this phenomenon are called as armchair, whereas, SWCNTs are semiconducting if n_2=0, and the nanotubes are called zigzag or chiral. The diameter of CNT can be calculated using:

$$D_{CNT} = 0.078\sqrt{\left(n_1^{\ 2} + n_2^{\ 2} + n_1 n_2\right)} \tag{2}$$

The semiconducting channel between drain and source of CNTFET can be turned on/off electrostatically through the third contact gate. CNTFETs are suitable for low-voltage, low-power and high speed applications through ballistic conduction by decreasing the power dissipation and also increasing the speed. In this paper different full adder logic styles are discussed. Full adder provides Sum and Cout for three input signals A, B and Cin [4].

2. FULL ADDER DESIGNS

The C-CMOS logic design style in Fig. 2 comprises of 28T. The reduced short-circuit current gives full voltage swing outputs and its critical path consists of five transistors, resulting in long propagation delay [5]-[9]. At low voltage reliable operation is provided and it is robust against voltage scaling.

The TFA in Fig. 3 comprises of 16T and 4T in its critical path. It produces the same delay for the Sum and Cout [6]. Because of lower transistor count and low input capacitances it has low power consumption compared to C-CMOS and performance degrades due to coupling inputs to outputs.

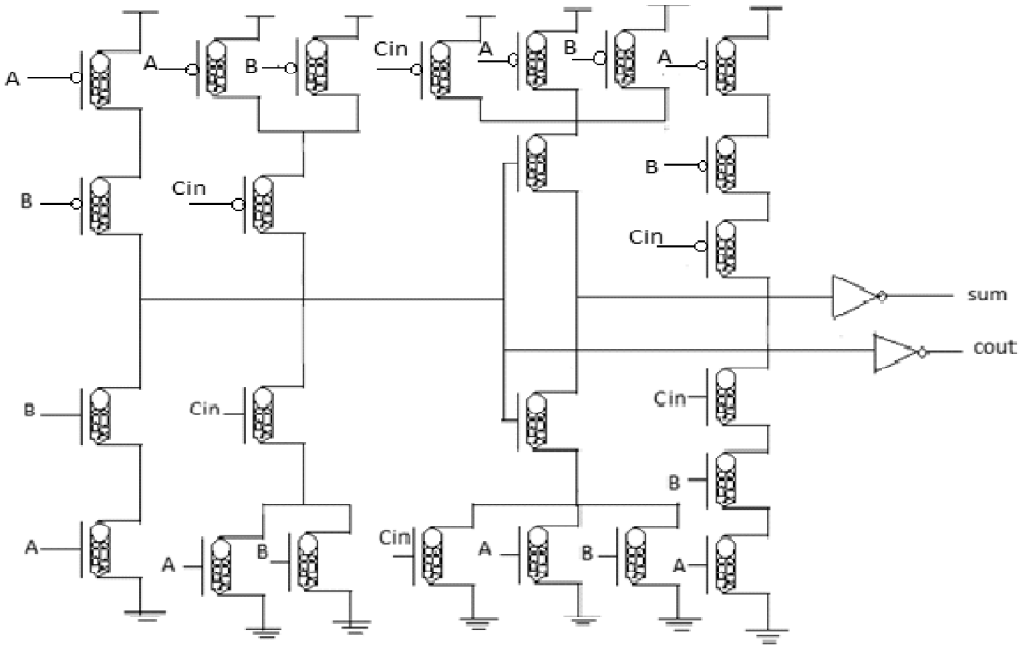

Figure 2: C-CMOS FA

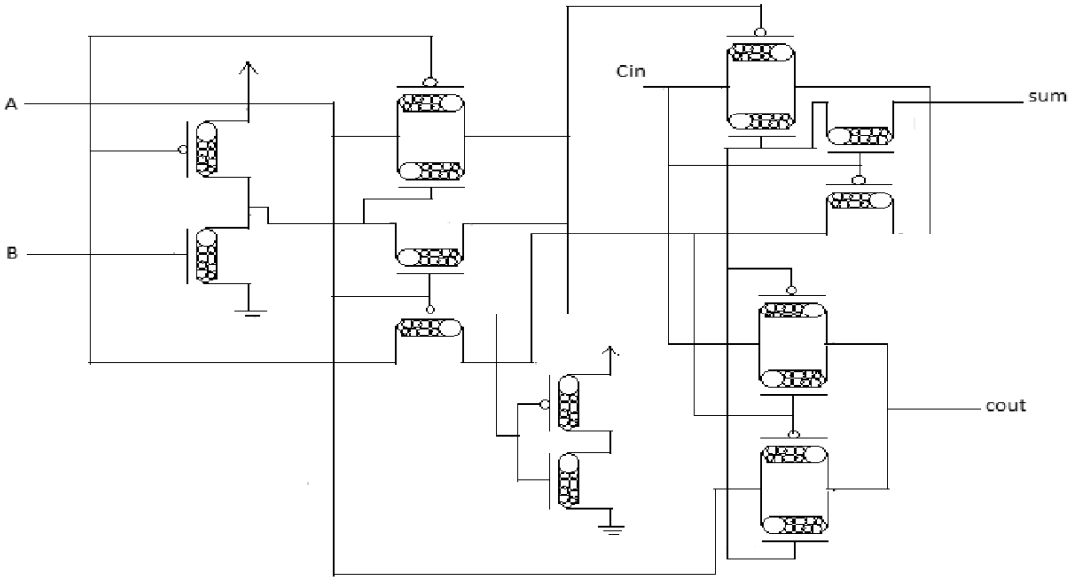

Figure 3: TFA

A transmission gate adder (TGA) shown in Fig. 4 uses CMOS transmission gates and has 20T with 4T in its critical path [6]. Its performance degrades due to lack of driving capability which can be overcome by using buffers at the output nodes. It has less delay and power consumption when compared to TFA.

The SERF in Fig. 5 uses 10T and due to no direct path which reduces the power consumption [6]. Despite threshold loss problem, the major advantage of this system is its energy efficient design which is achieved by eliminating the direct path.

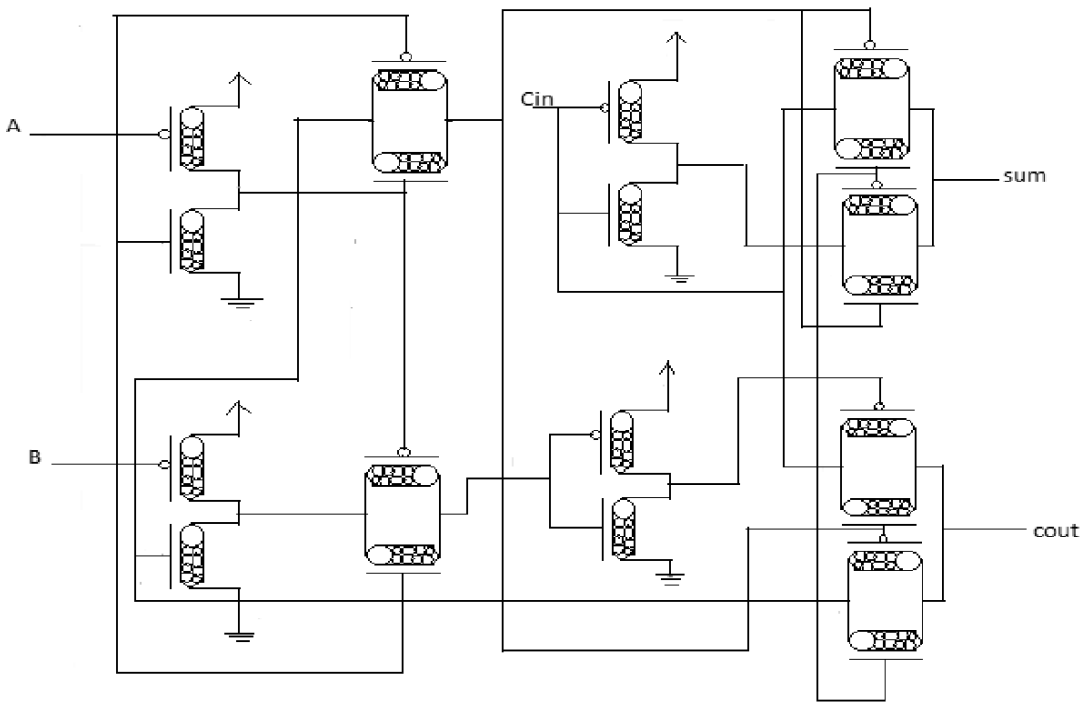

Figure 4: TGA

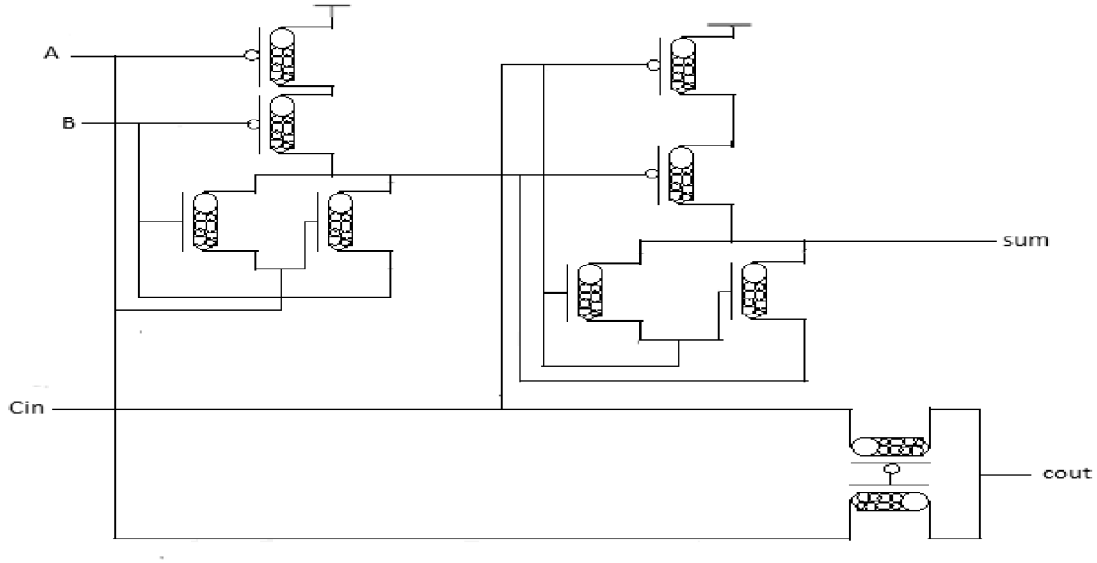

Figure 5: SERF

Similarly, in Fig. 6, 13A for proving sum 10T and two cascade two input XNORs are used. For realizing two-input XNOR circuit it uses both CMOS and pass-transistor logic (PTL) styles, in which the later do not provide enough driving power [6]. Relatively higher power consumption of 13A could be due to the short-circuit power dissipation [10]-[12].

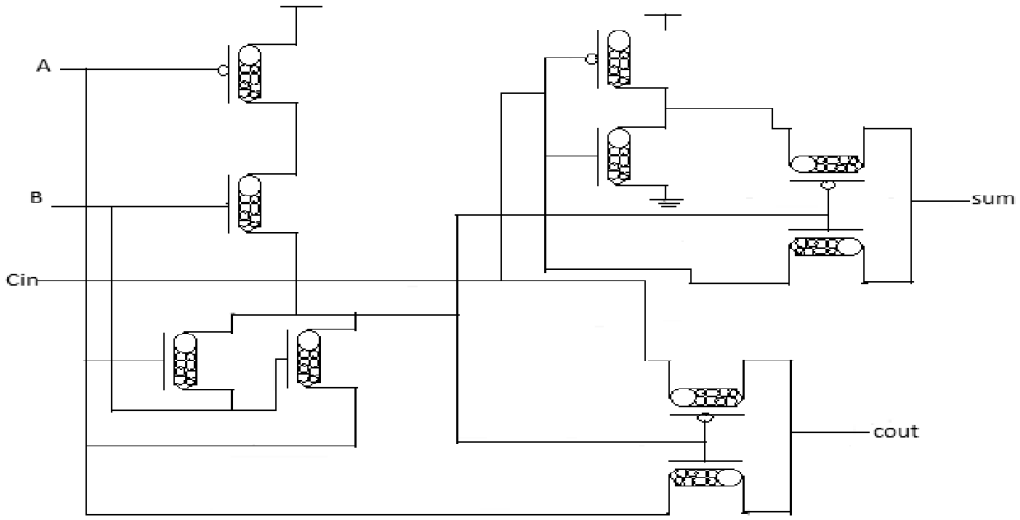

Figure 6: 13A

The HPSC FA i.e. hybrid pass transistor logic with static CMOS output drive full adder in Fig. 7 consists of 26T and uses 4T for generating two-input XOR/XNOR. FL transistor and PT are used for strengthening XOR/ XNOR circuit output for overcoming the threshold-loss problem [13].

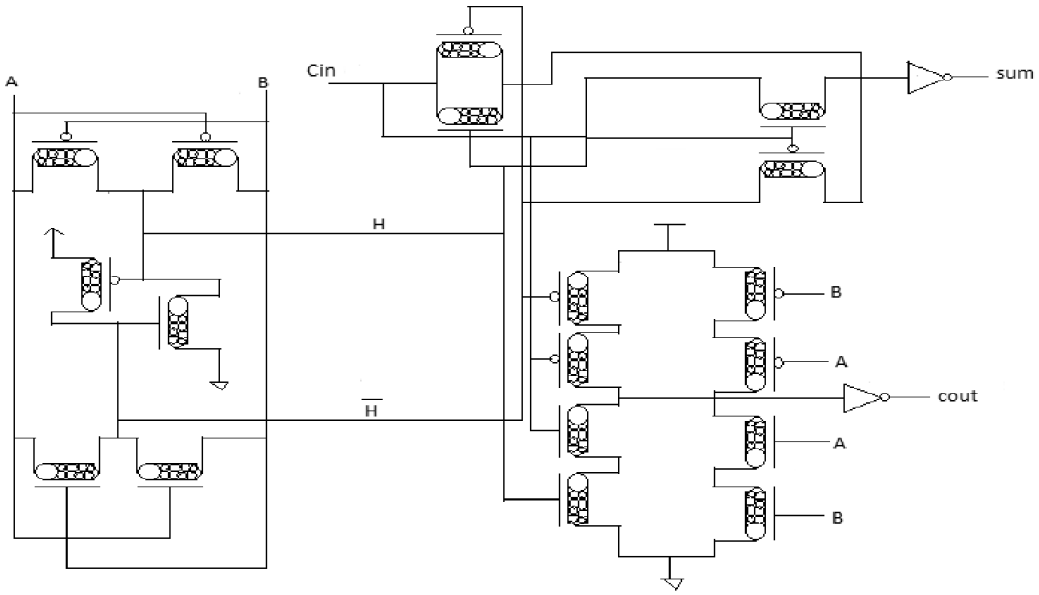

Figure 7: HPSC FA

The High performance HPSC FA in Fig. 8 comprises of 24T with 4T in its critical path. When compared to HPSC it has high power consumption. Because of the additional inverter this results in large short-circuit current and more delay than the HPSC [14]. The cross coupled P-CNTFETs are used for restoring the XOR/XNOR circuit output for increasing the speed.

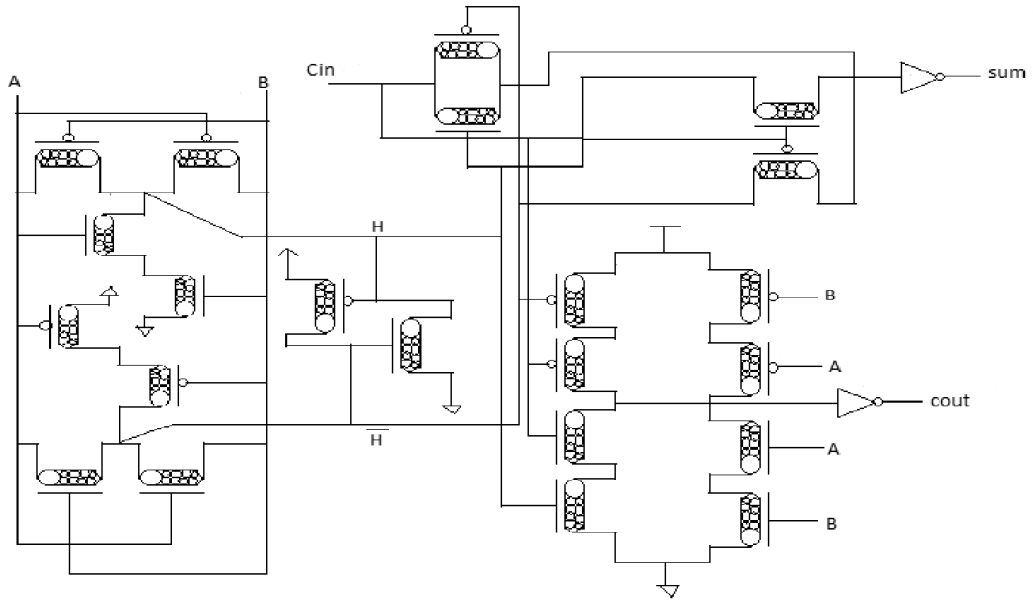

Figure 8: High Performance HPSC FA

The PT-FA in Fig. 9 comprises of 26T with 4T in its critical path. The good driving capability is providing by the use of NOT gates at output [15]. There is leakage of current and high power consumption due to non-full output swing.

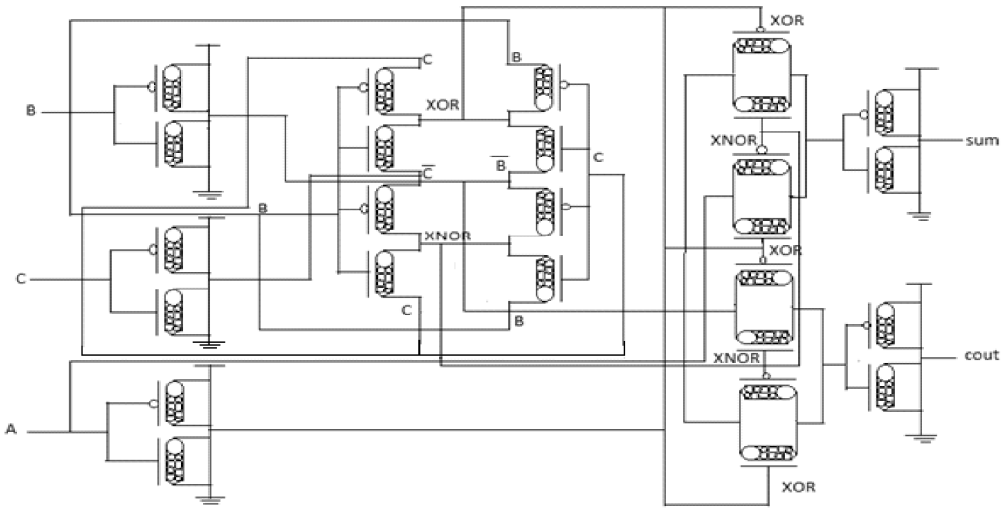

Figure 9: PT-FA

The FL-FA in Fig. 10 used for restoring non-full-swing outputs of the XOR/XNOR circuit. It contains 28T with 4T in the critical path [15]. The desired driving power is provided by using inverters at the output nodes. The feedback loop reduces power consumption and delay by generating full swing output voltage and by eliminating static power dissipation.

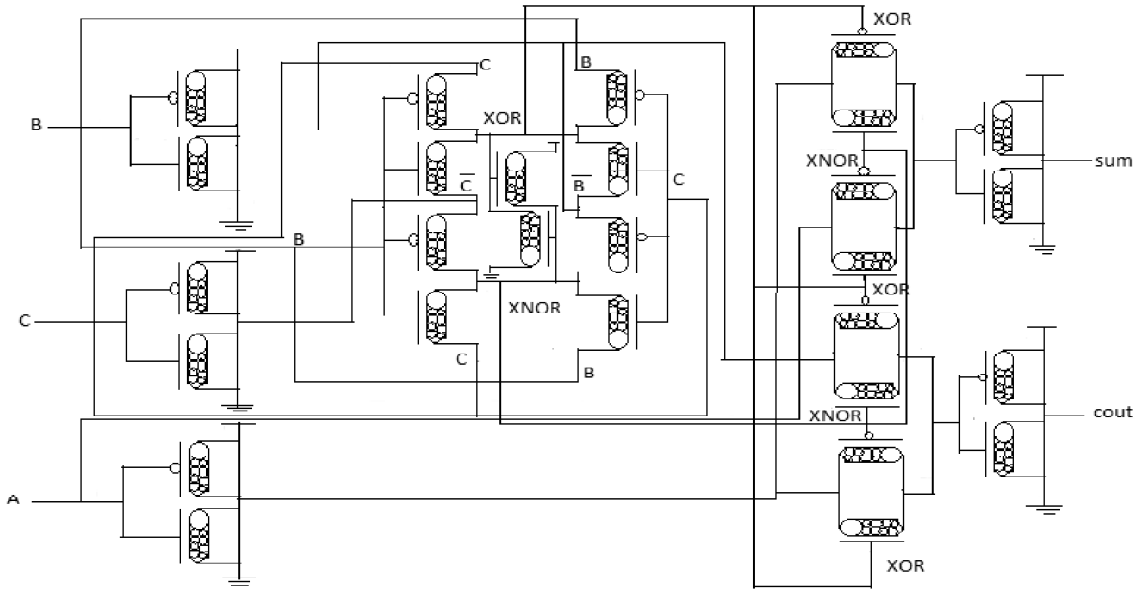

Figure 10: FL-FA

The DD-FA in Fig. 11 has double driving path for XOR/XNOR circuits. For producing full output swing for the XOR/XNOR circuit transmission function and PTL logic are used [20]. It contains 30T and 4T in its critical path. It has low power consumption compared to PT-FA and FL-FA.

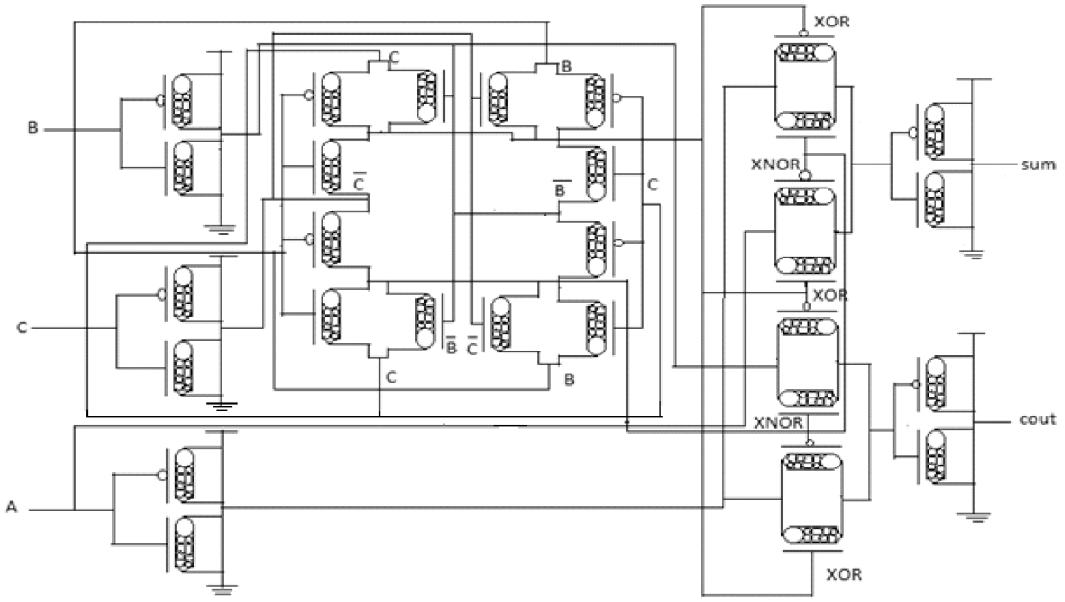

Figure 11: DD-FA

The SD-FA in Fig. 12 with 28T has single driving path for the XOR/XNOR circuit. TG and PTL logics are used for generating desired outputs [15]. Because of few transistors it utilizes low power compared to DD-FA.

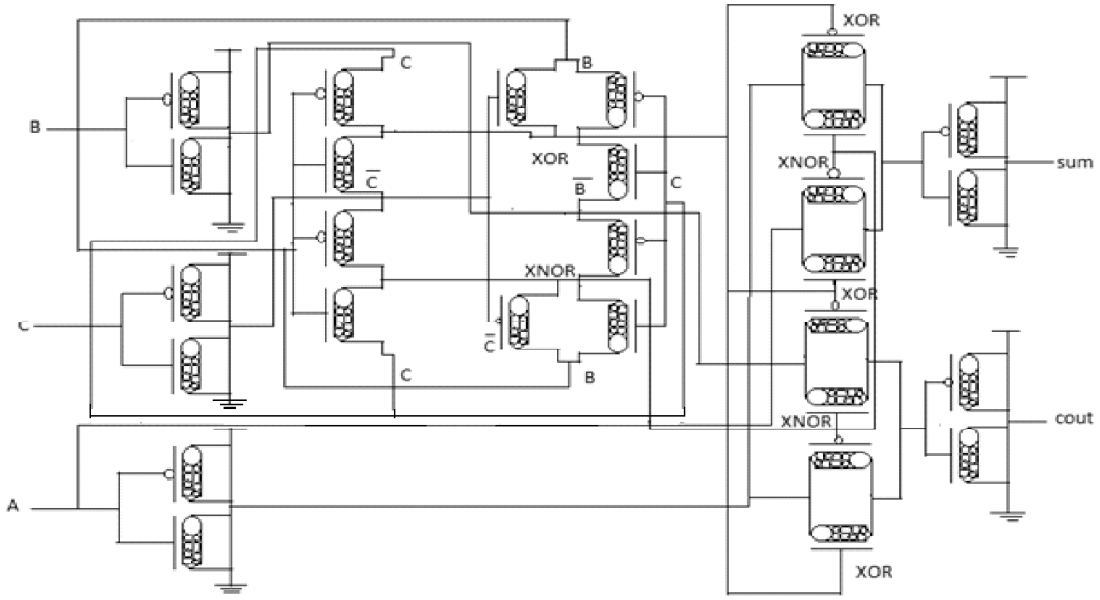

Figure 12: SD-FA

The RSD-FA in Fig. 13 is used for removing two pass transistors which are single driving. The RSD-FA has 26T with driving capability [15]. Owing to its less number of transistors, it has least power dissipation when compared with FL-FA, DD-FA.

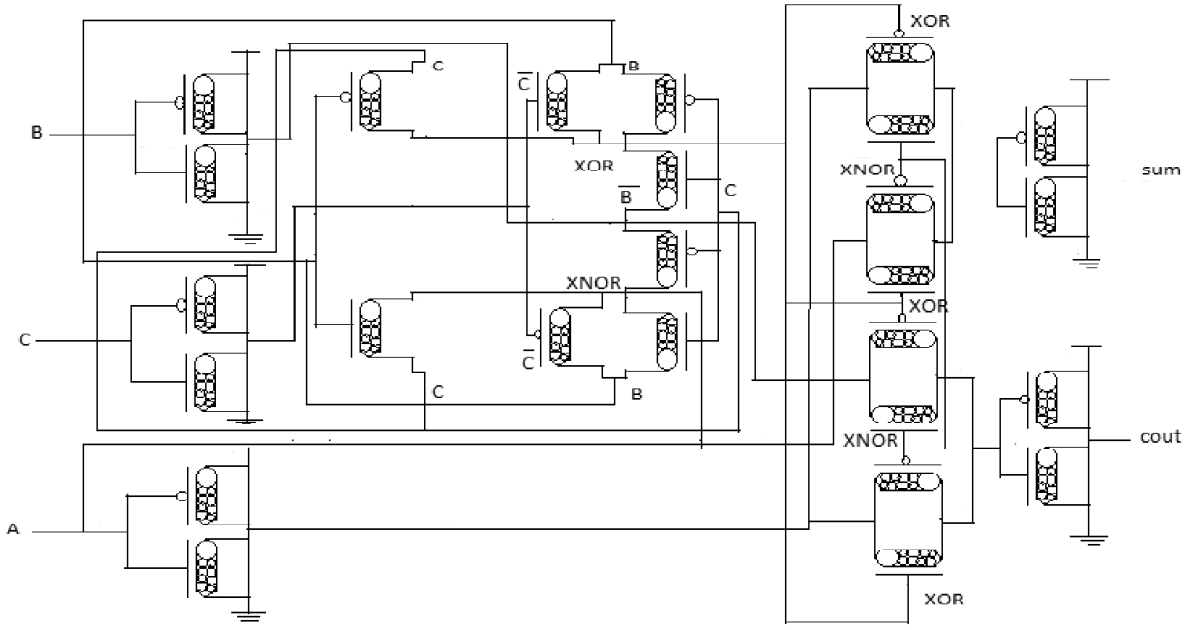

Figure 13: RSD-FA

The ND-FA with non-driving power in Fig. 14 is used for producing full output swing by using TGs. The lack of driving power is owing to input output coupling [15]. It has 24T and is quicker due to 3T in its critical path. Due to small fan-outs it does well.

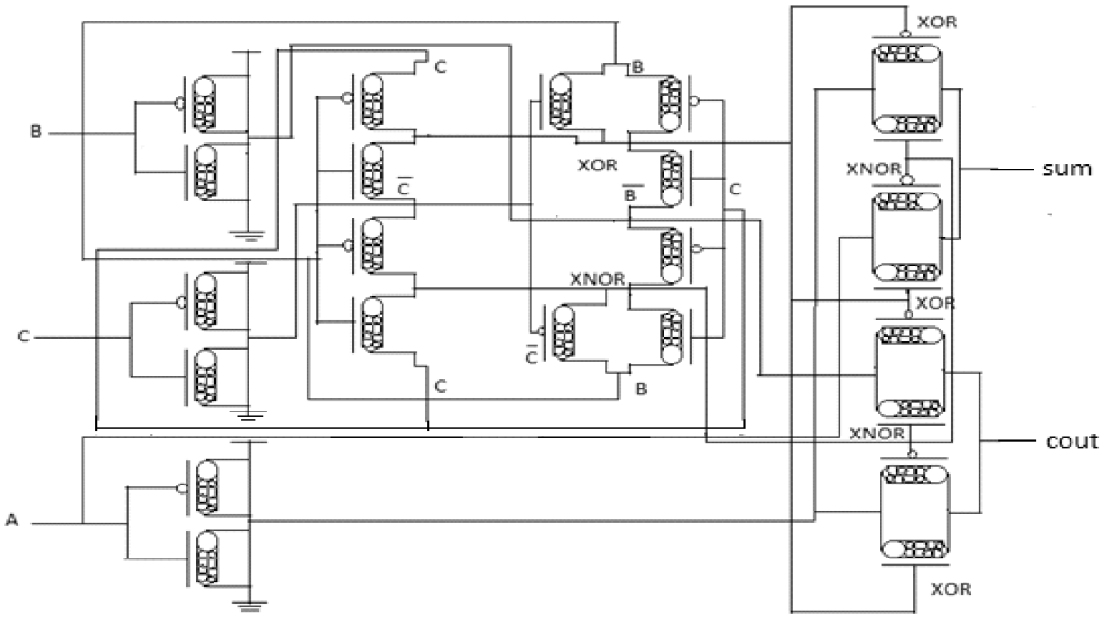

Figure 14: ND-FA

3. SIMULATION AND PERFORMANCE ANALYSIS

The full adders performing with 0.9 v power supply is checked by simulation using CNTFETs. Here the chirality vector used is (19, 0) by this the diameter and threshold voltage reaches 1.467 nm and 0.27 V. The performance analysis is performed using CADENCE with 32 nm channel length [18]. The simulations for full adders are shown below.

C-CMOS full adder simulation is in Fig. 15

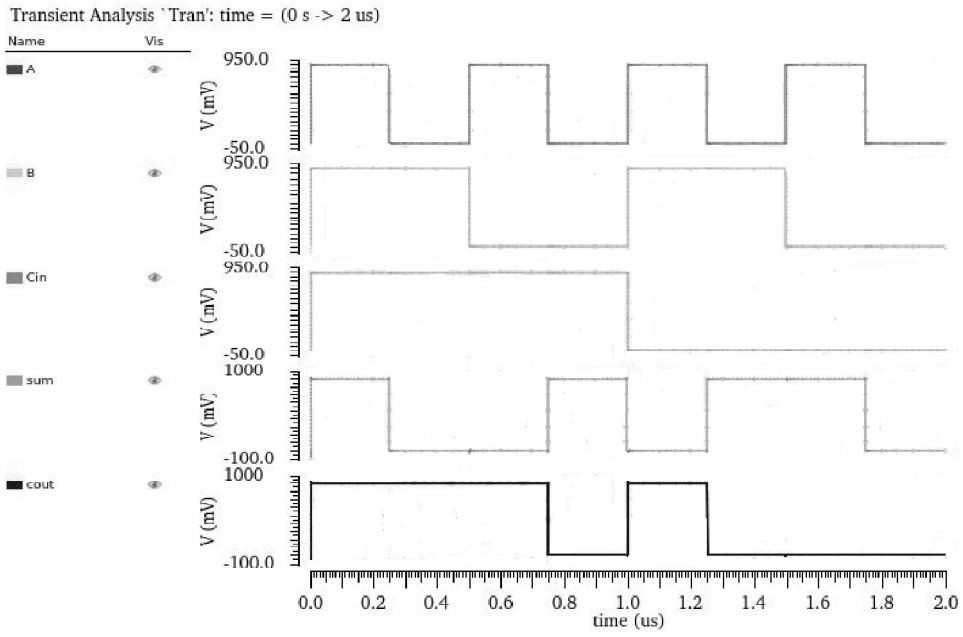

Figure 15: Simulation of C-CMOS

TFA simulation is in Fig. 16

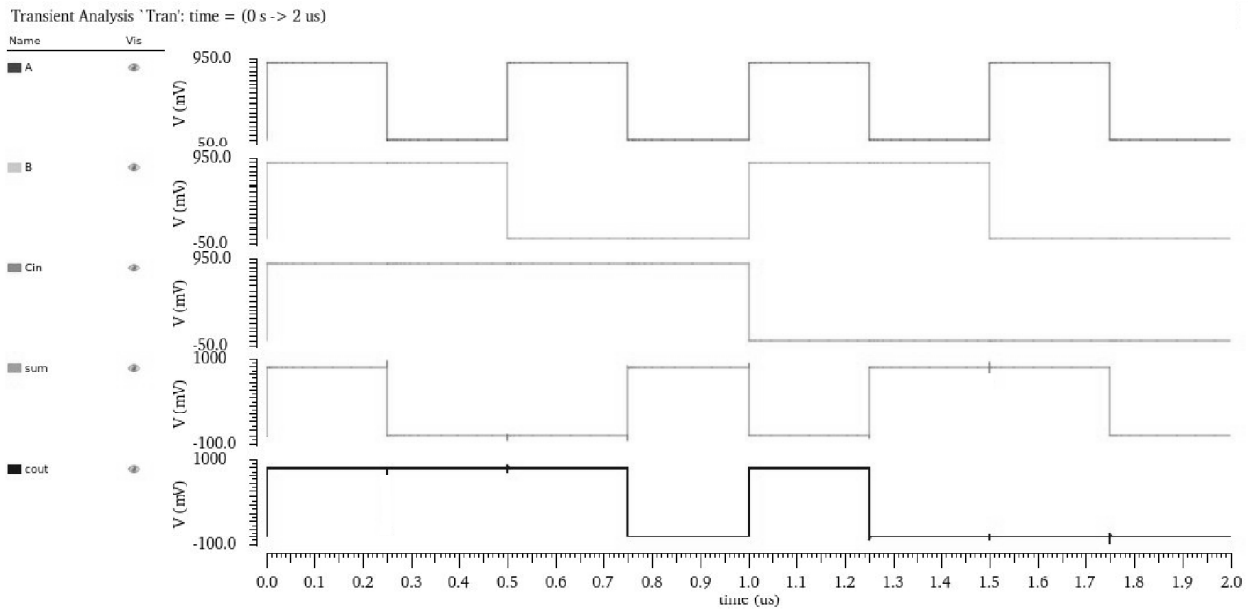

Figure 16: Simulation of TFA

TGA simulation is in Fig. 17

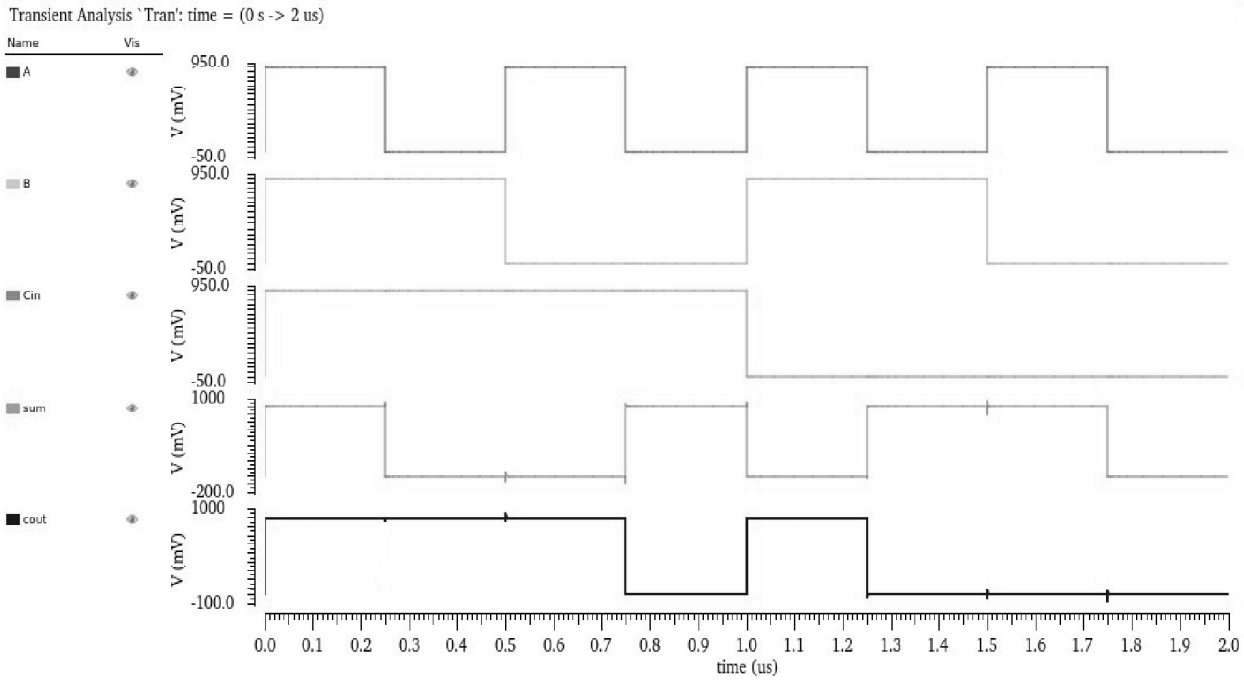

Figure 17: Simulation of TGA

SERF full adder simulation is in Fig. 18

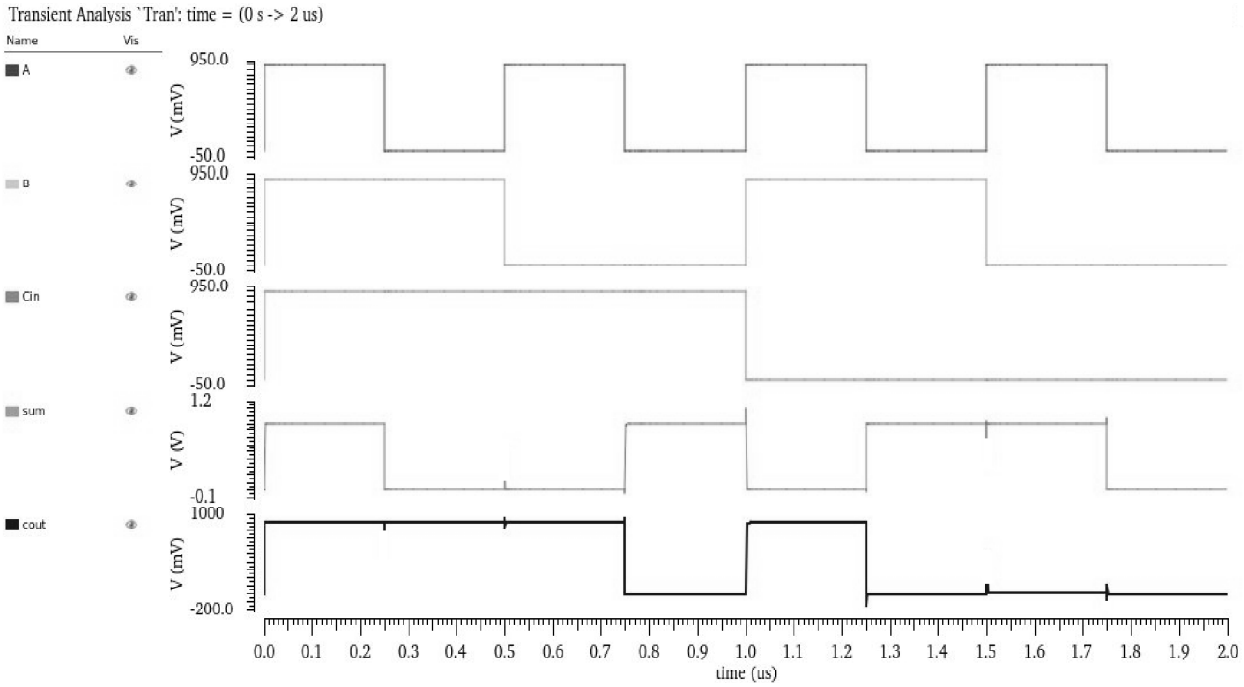

Figure 18: Simulation of SERF

13A full adder simulation is in Fig. 19

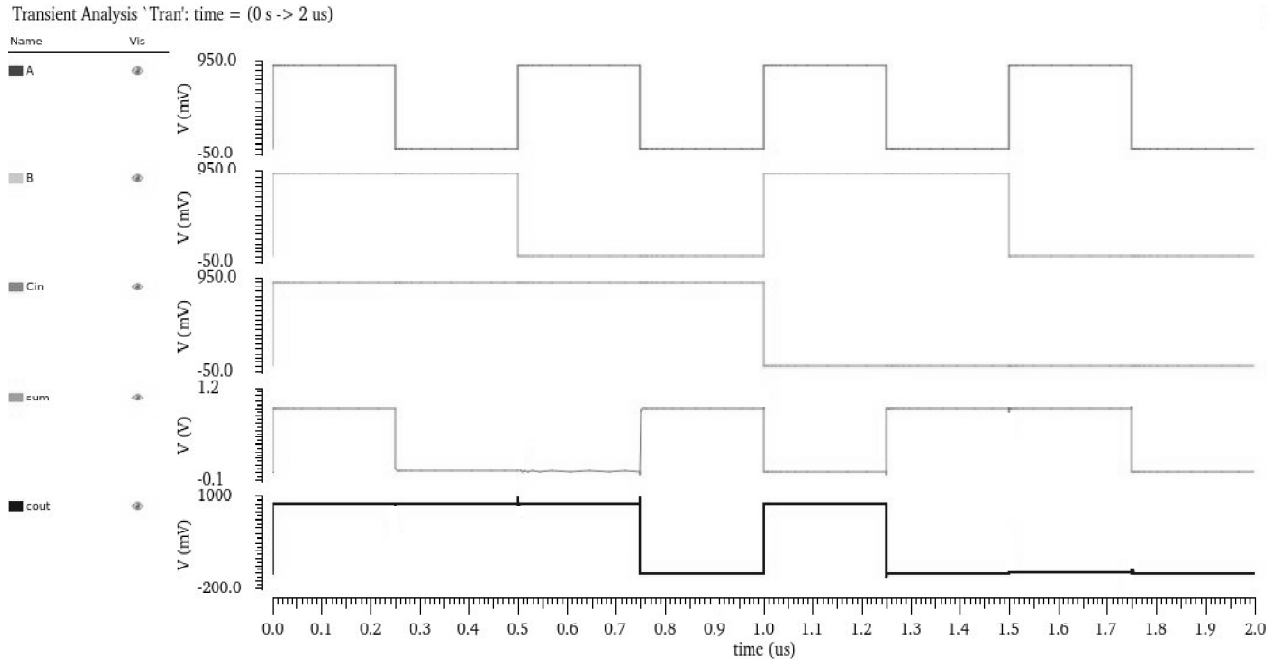

Figure 19: Simulation of 13A

HPSC full adder simulation is in Fig. 20

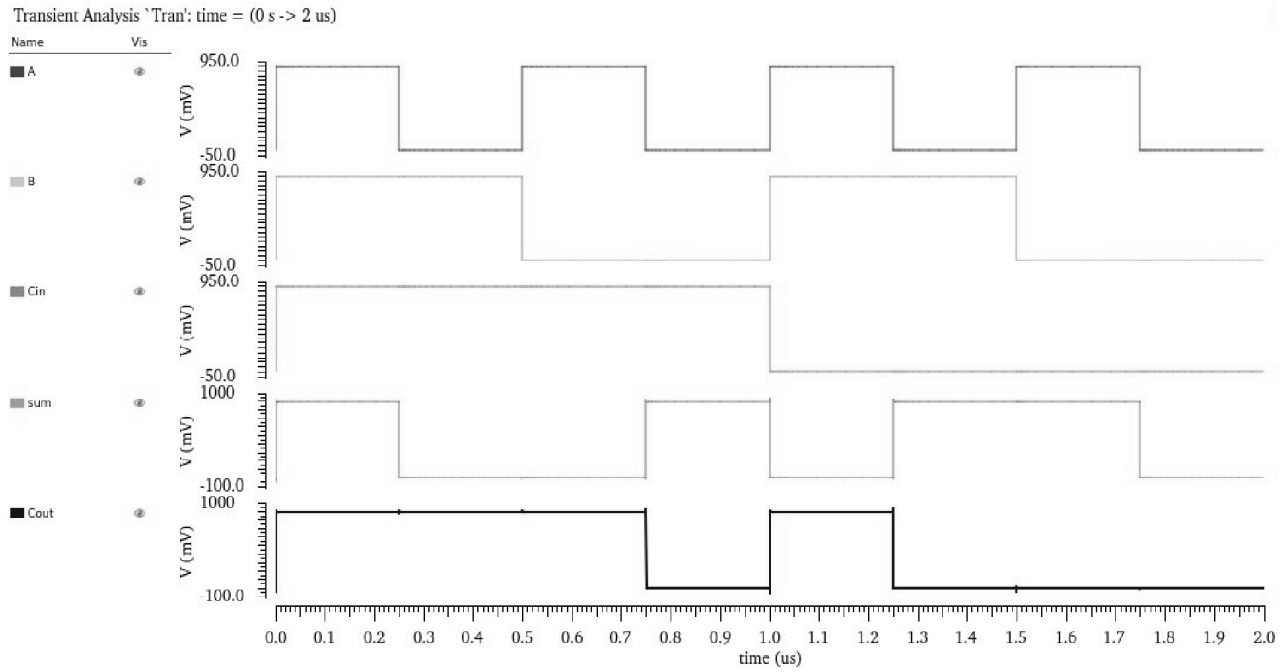

Figure 20: Simulation of HPSC

High performance HPSC-FA simulation is in Fig. 21

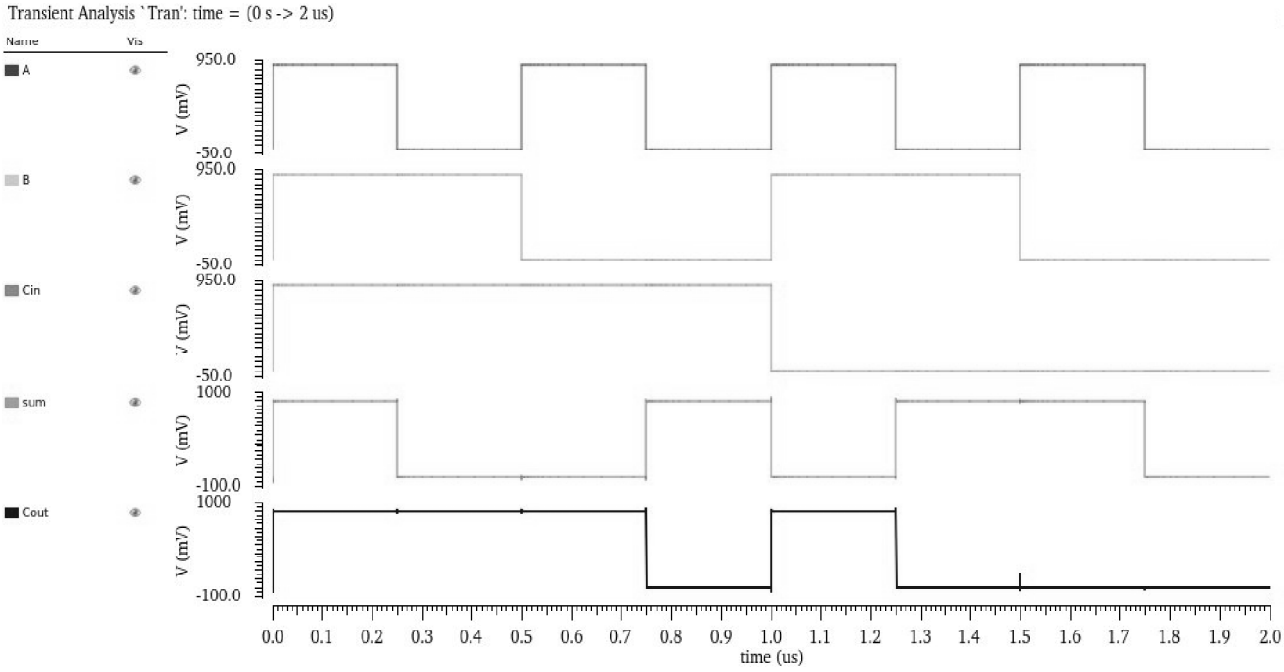

Figure 21: Simulation of High Performance HPSC

PT-FA simulation is in Fig. 22

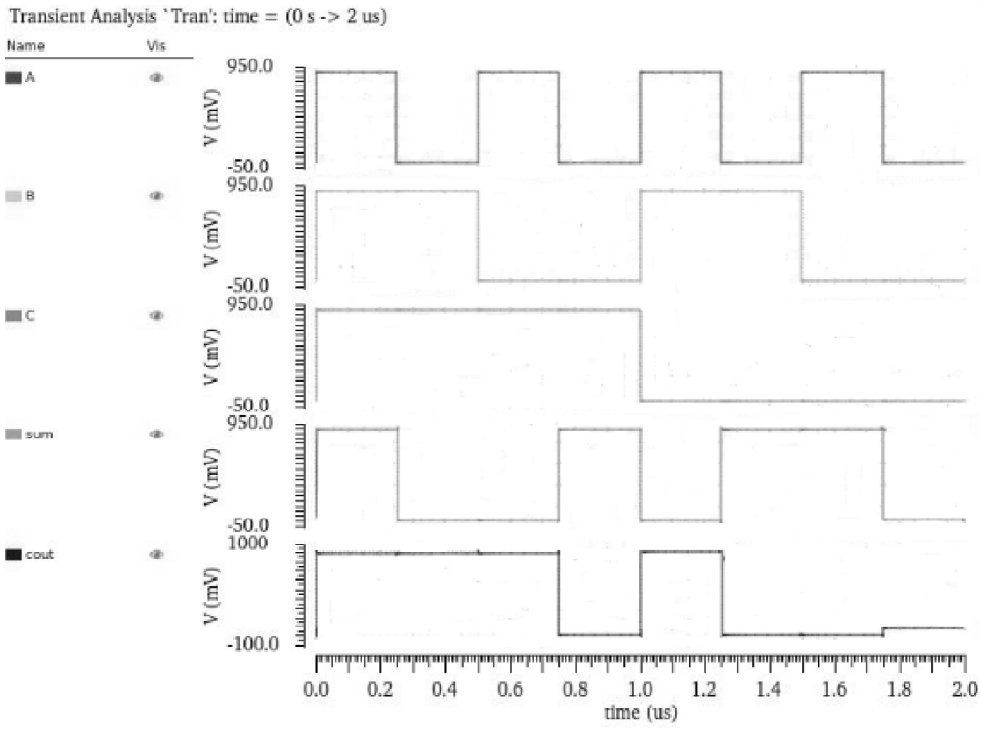

Figure 22: Simulation of PT-FA

FL-FA simulation is in Fig. 23

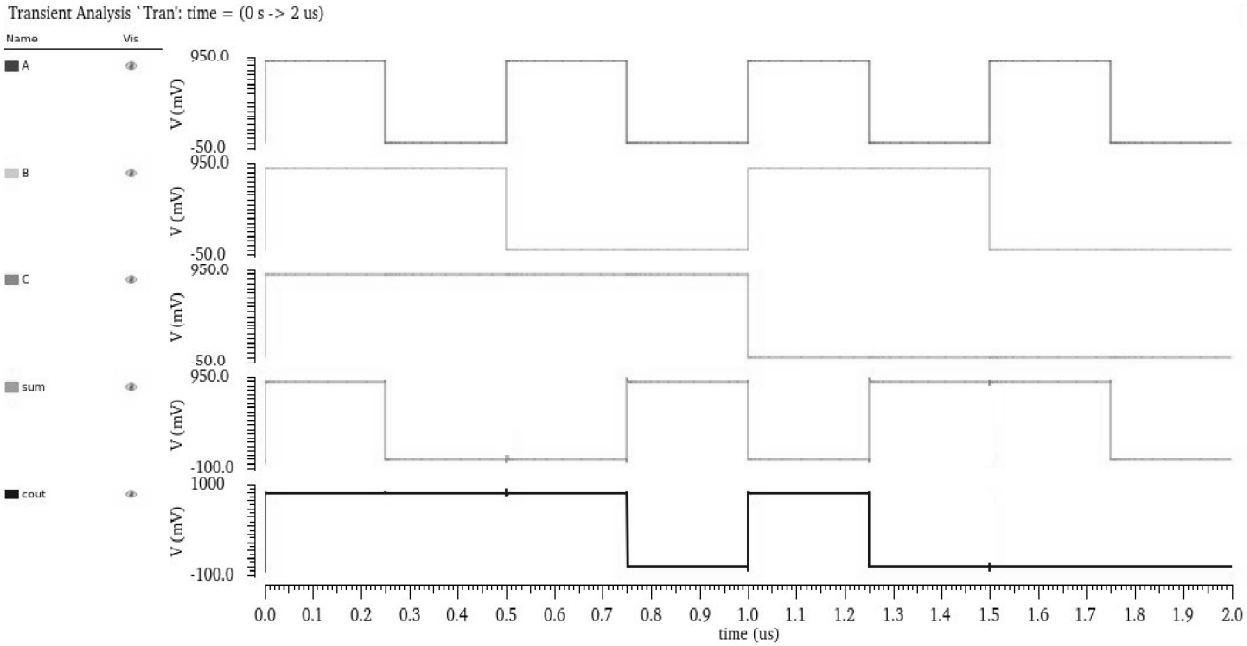

Figure 23: Simulation of FL-FA

DD-FA simulation is in Fig. 24

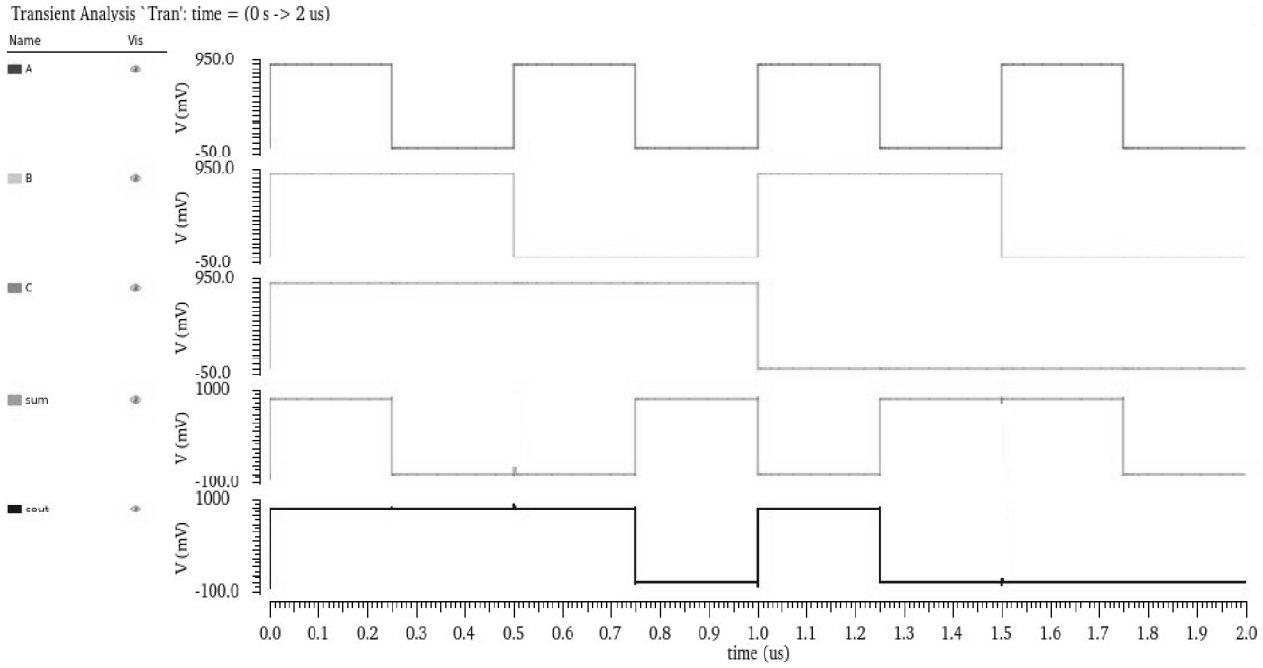

Figure 24: Simulation of DD-FA

SD-FA simulation is in Fig. 25

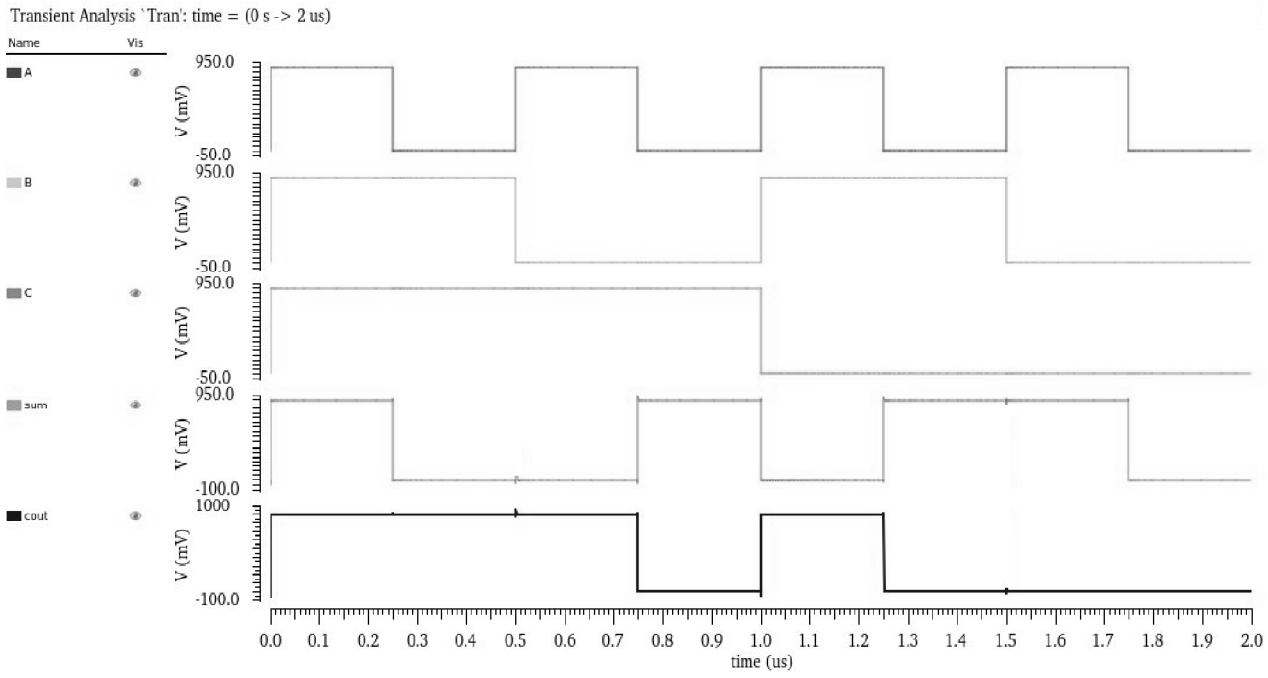

Figure 25: Simulation of SD-FA

RSD-FA simulation is in Fig. 26

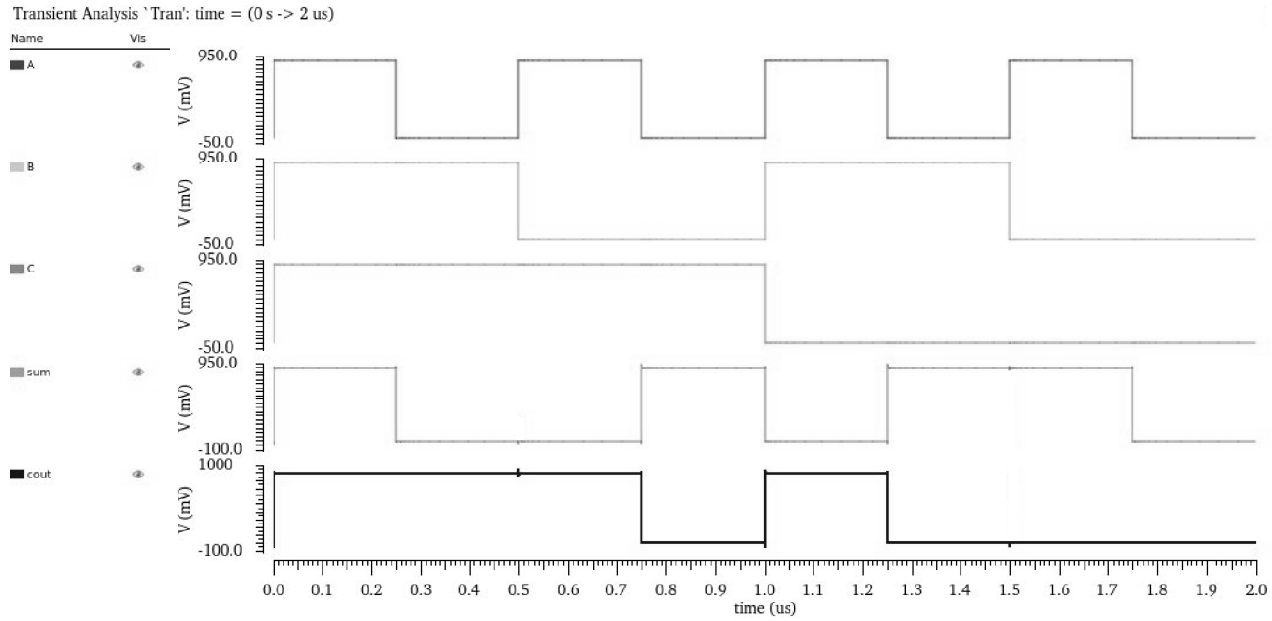

Figure 26: Simulation of RSD-FA

ND-FA simulation is in Fig. 27

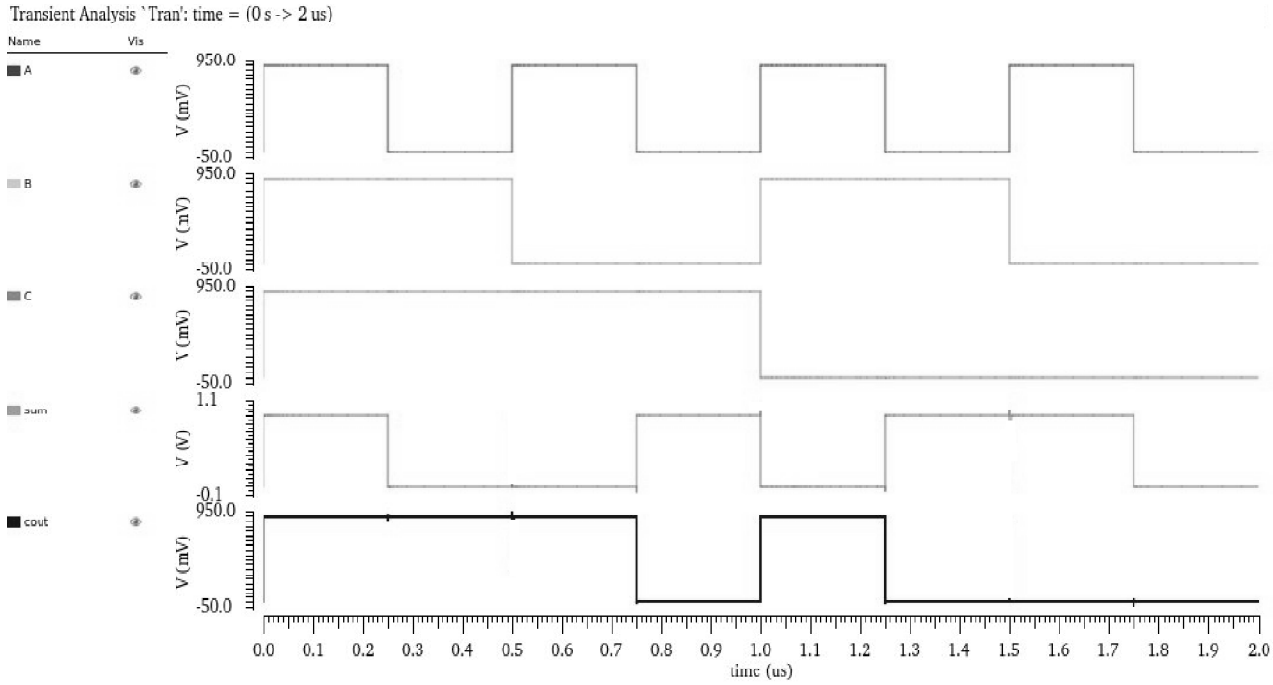

Figure 27: Simulation of ND-FA

The RSD-FA and FL-FA are highly robust. DD-FA and SD-FA has the good results [16]-[17]. The delay and power are calculated shown in Table 1. The ND-FA has less delay at 0.9 V and the RSD-FA has least power consumption [18]-[20].

Table 1
Comparison of Delay, Power and PDP

S. No	Design Names	V_{dd} = 0.9 V		
		Delay (E-11 S)	Power (E-6 W)	PDP (E-17 J)
1.	PT-FA	1.7862	0.17381	3.1046
2.	FL-FA	1.2410	0.18416	2.2854
3.	DD-FA	1.1798	0.11837	1.3925
4.	SD-FA	0.9798	0.14164	1.3878
5.	RSD-FA	0.9963	0.07123	0.7096
6.	ND-FA	0.6470	0.13614	0.8808
7.	C-CMOS FA	2.3695	0.11460	2.7155
8.	HPSC FA	3.5237	0.08314	2.9296
9.	High performanceHPSC FA	3.5024	0.11363	3.9798
10.	TFA	1.4701	0.10827	1.5917
11.	TGA	1.1236	0.13418	1.5077
12.	SERF	935.27	4.3261	4046.07
13.	13A	915.78	5.9084	5410.80

4. CONCLUSION

As MOSFET has problems in nanoscale region a technology named CNTFET was emerged. The CNTFET devices enables high speed and low power because of ballistic transport and low OFF current. The simulations and the performance analysis are evaluated using CADENCE tool in 32 nm CNTFET technology. For finding full adders robustness the transient analysis were performed.

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