I J C T A, 9(4), 2016, pp. 1989-1995

Design and Implementation of a Low Power Carry Propagate Adder Using GDI Cell

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ABSTRACT

Full adder is an essential component in the design of digital circuits. This paper introduces a novel low power Carry Propagate Adder using GDI technique. This technique allows reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design. The proposed Carry Propagate Adder using GDI cells is compared with CMOS adder in terms of area, delay and power dissipation. The circuits are simulated using HSPICE for power and delay calculations and the area measurements are done using MICROWIND in 90nm technology.

Keywords: Full adder**,** Gate Diffusion Input Technique (GDI), Complementary Metal Oxide Semiconductor (CMOS), Shannon's Expansion Theorem, Carry Propagate Adder.

1. INTRODUCTION

Addition is the most important basic function of any digital processing system. Adders are not only used for arithmetic operation but also necessary to compute virtual physical address in memory fetch operation in all modern computers. Address plays a critical role in microprocessor. For designing a fast processing digital system fast adders are essential. Many fast adders are available but the design of high speed with low power and requiring less area are still challenging. In modern super computers, multiple ALU'S with wide adders and multiple execution core units on the same chip creates thermal hotspots and large temperature gradients. This affects the circuit reliability and increasing the cooling cost of the system. Ideally, adders should have highest performance with least amount of power dissipation and small layout area to minimize unnecessary delays. While designing power dissipation is taken as the main design objective equal to the performance of the system due to fast growth of power density in integrated circuits as well as popularity of portable devices. Specially for the VLSI designers, designing power efficient adders for digital system has become main goal [5].

Generally Ripple Carry Adders are used among all types of adders because of its compact design but it is the slowest adder. On the other hand, Carry Propagate adders are the fastest adders but they occupy large area and large power dissipation [6]. CMOS is the most common circuit design style/technique for designing any digital circuit but it dissipates most of the power during transistor switching activity. Here we propose a power efficient Carry propagate adder based on gate diffusion input circuit design style [3].

In this paper, section II explains the gate diffusion input technique and section III gives the details of CMOS logic. Section IV describes the design of carry propagate adder from ripple carry adder. The simulation results are shown in section V and section VI gives the conclusion.

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2. GATE DIFFUSION INPUT (GDI) TECHNIQUE

Generally for designing any digital circuit CMOS logic is used. It consumes more power, more propagation delay, it occupies more space and more complexity while designing the digital circuits. To overcome the

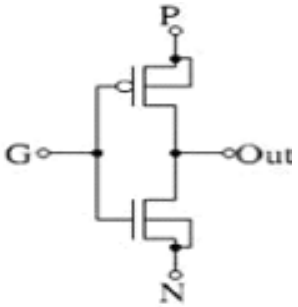


Figure 1: GDI Basic cell

Table 1
Truth table of GDI Gate

N	P	G	Out	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	A+B	F2
'1'	B	A	A+B	OR
B	'0'	A	AB	AND
C	B	A	AB+AC	MUX
'0'	'1'	A	A	NOT

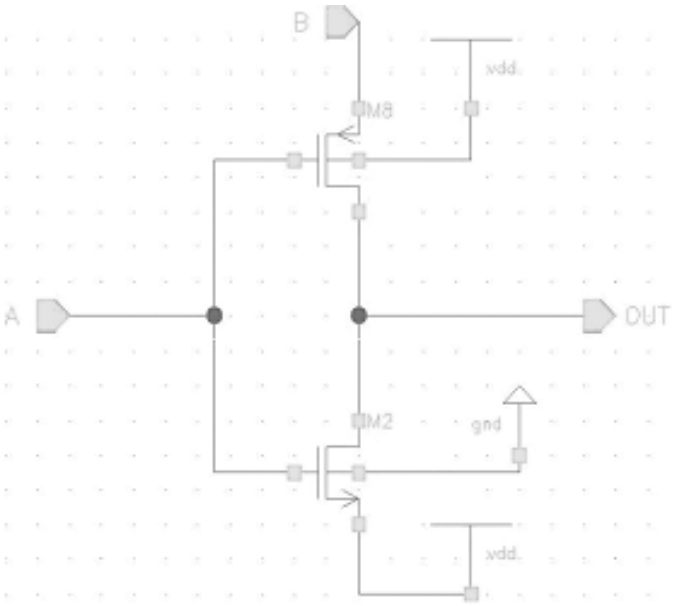


Figure 2: GDI OR Gate

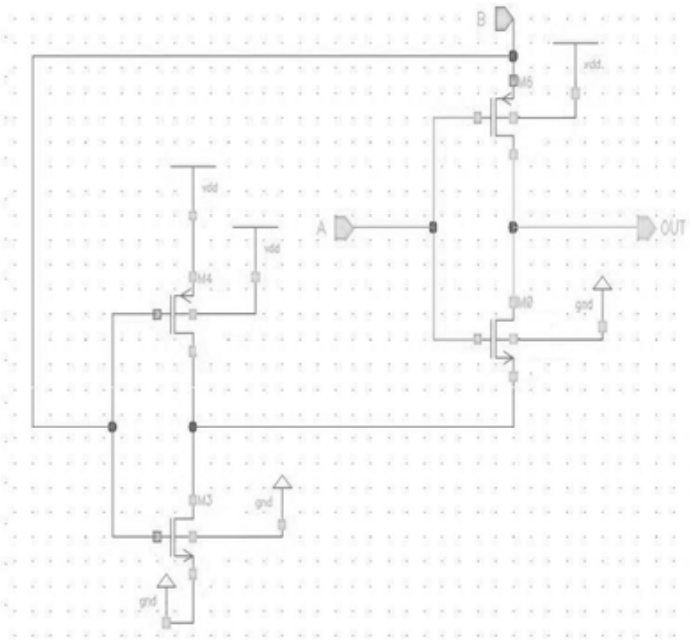


Figure 3: GDI XOR Gate

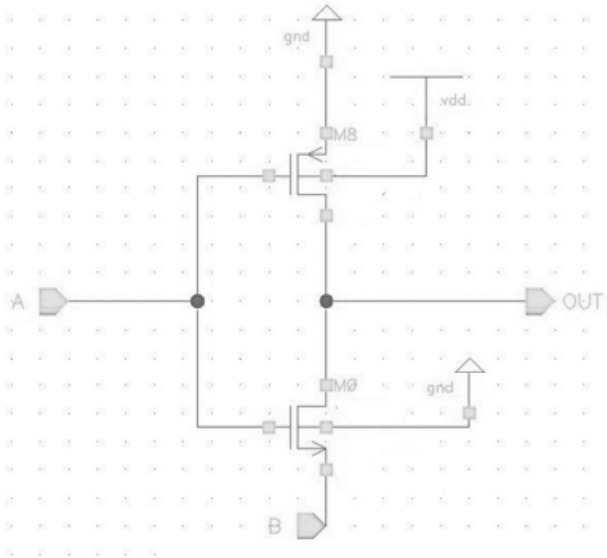


Figure 4: GDI AND Gate

difficulties of CMOS logic, a new logic called Gate Diffusion Input (GDI) is proposed in this work [2]. The basic GDI cell is shown in Fig. 1 and table 1 shows the truth table of basic gates using GDI cells. Fig. 2, Fig. 3 and Fig. 4.show the implementation of OR, XOR and AND gate using GDI technique.

3. CMOS LOGIC

CMOS is a technology for constructing integrated circuits. It is used in microprocessor, microcontroller, static RAM and other digital logic circuits [9]. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converter, and highly integrated transceivers for many types of communication. CMOS is also sometimes referred to as complementary-symmetry metal–oxide–semiconductor [4]. The Full adder circuit is designed using basic digital gates like AND, OR and XOR and are shown in Fig. 5, Fig. 6 and Fig. 7 respectively and a 28T full adder is shown in Fig. 8.

4. CARRY PROPOGATE ADDER

A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the

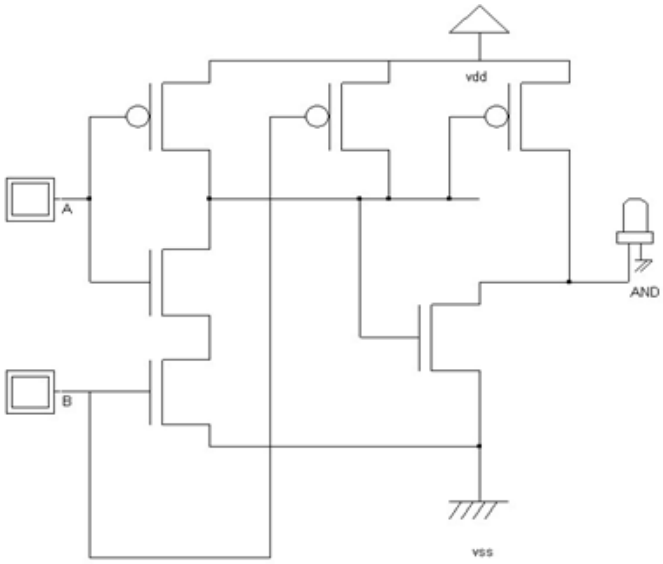


Figure 5: CMOS AND Gate

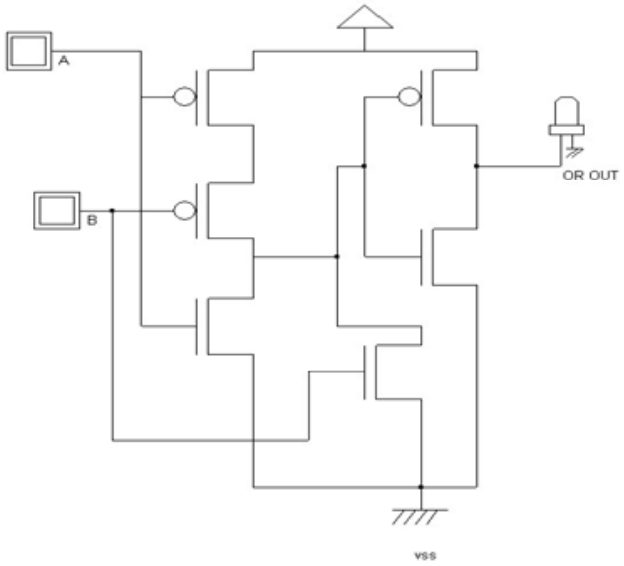


Figure 6: CMOS OR Gate

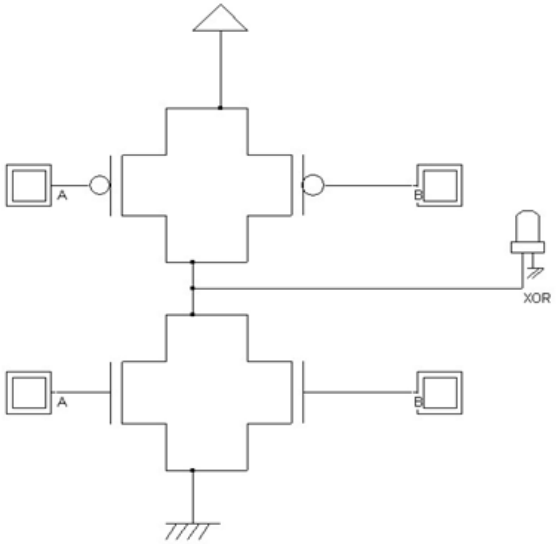


Figure 7: CMOS XOR Gate

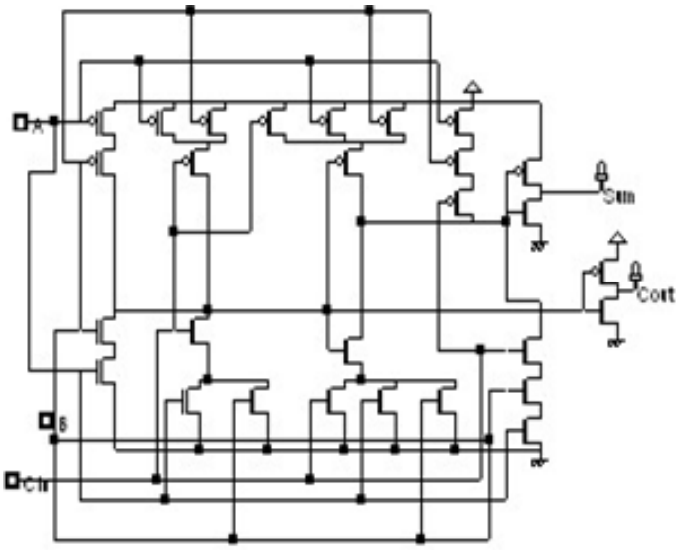


Figure 8: Full Adder-28 Transistor

next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. A propagation delay inside the logic circuitry is the reason behind this.

Propagation delay is time elapsed between the application of an input and occurrence of the corresponding output. Consider a NOT gate, When the input is "0" the output will be "1" and vice versa. The time taken for the NOT gate's output to become "0" after the application of logic "1" to the NOT gate's input is the propagation delay here. Similarly the carry propagation delay is the time elapsed between the application of the carry in signal and the occurrence of the carry out ( ) signal [8].

The Boolean equations of a full adder are given by:

= ABC + AB'C' + A'B'C + BA'C'

= (AB'+BA')C + AB + A'B') C'

= A⊕B⊕C

= AB + AC + BC

= AB + C (A⊕B)

Fig. 8 shows a 1-bit RCA and a 1-bit CPA with carry propagate and generate signal [1]. The full-adders connected to make a multi-bit carry-propagate adder is shown in Fig. 10. The right-most adder adds least-

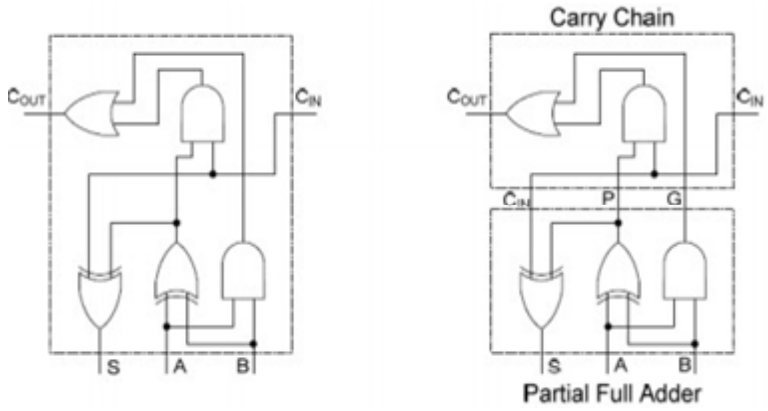


Figure 9: a) one bit RCA b) one bit CPA cell

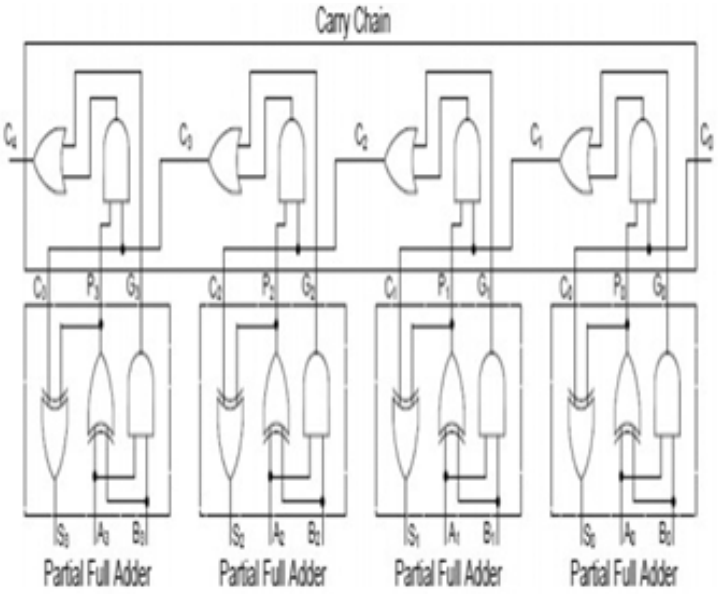


Figure 10: Carry Propagate Adder

significant bits [10]. Carry-out is passed to next adder, which adds it to the next-most significant bit, and this can be extended to any number of bits. The full adder is developed using the basic types of digital gates like AND, OR and XOR.

The internal signals P_i and ?? are given by:

= ?+ ?

??=?? ??

The output sum and carry can be defined as:

??= P_i +?? ?+

??+1 =?+ P_i??

?? is known as the carry Generate signal since a carry (??+ 1) is generated whenever ???=1, regardless of the input carry (??) [7].

Pi is known as the carry propagate signal since whenever Pi =1, the input carry is propagated to the output carry, i.e.,??+1 =??

The values of Pi and Gi only depend on the input operand bits (??&??) as clear from the Fig. 10.

Table 2
Power and Delay of GDI and CMOS gates

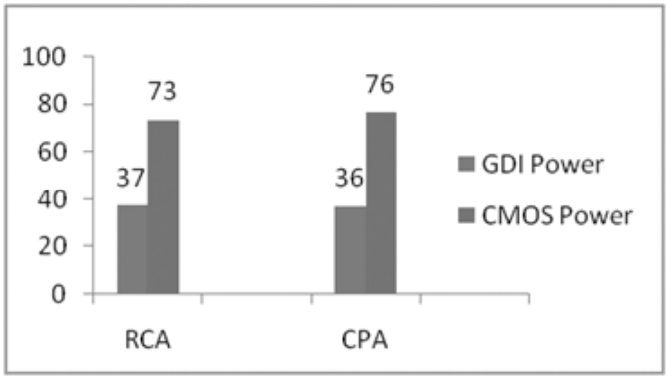
Gatetype	GDI				CMOS			
	Power (µW)	Delay (nsec)	PDP	No. of Transistor	Power (µW)	Delay (nsec)	PDP	No. of Transistor
AND	0.1162	3.81	0.44	2	1.153	3.82	4.404	6
OR	0.104	0.098	0.010	2	1.902	0.110	0.209	6
XOR	0.723	0.0126	0.009	4	1.243	0.0113	0.014	12

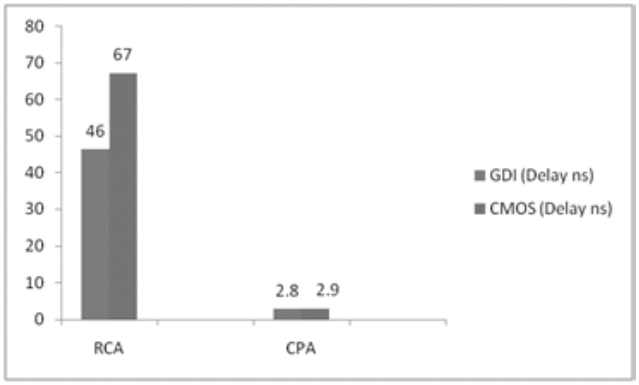
Table 3
Comparison of adder design using GDI an CMOS

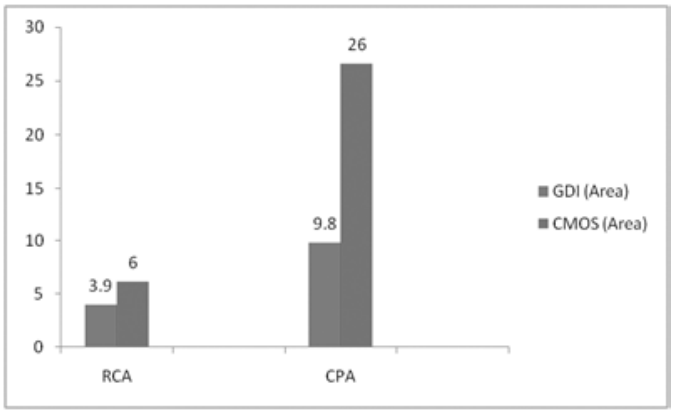
Adder	GDI				CMOSer			
	Power (µW)	Delay (nsec)	Area (µm)2	PDP	Power (µW)	Delay (nsec)	Area 2 (µm)	PDP
RCA	37.12	46.32	3.97	1719.40	73.23	67.13	6.12	4915.92
CPA	36.97	2.81	9.8	103.88	76.31	2.93	26.61	223.58

5. SIMULATION RESULTS

Logic gates are the fundamental building block for any digital circuit and they continue to be a topic of interest especially as technologies are scaled to the nanometer regime. In this work, the power and delay analyses of CMOS logic GDI logic circuits are carried out in 90nm process technology**.** The net lists of the circuits are extracted and simulated with BSIM4 models of MOSFET. The simulations are done in HSPICE







at a temperature of 27º C. The power, delay and power delay product (PDP) results of CMOS and GDI logic gates are shown in Table II and the comparison of RCA adder and CPA are given in Table III.

6. CONCLUSION

In this paper a l ow power Carry Propagate Adder based on GDI technique is presented. Ripple carry adder and carry propagate adder designed using GDI cells are simulated using HSPICE and their perfor mances are compared with CMOS based adders. From the g r a p h results it is concluded t hat the carry propagate adder based on gate diffusion input technique has a better performance than CMOS based adder in terms of power consumption, propagation delay, area required and power delay product.

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