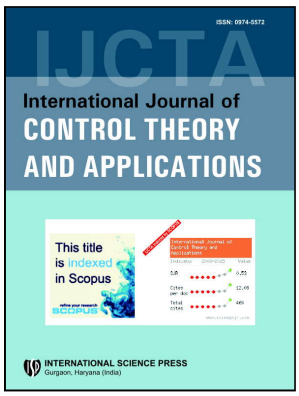

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Signaling Approach Based VoQ Router Architecture

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Abstract: System on chip (SoC) is integrated circuit containing thousand of components in a single chip and Network-On-Chip (NoC) is the novel communication mechanism going to be use for SoC whereas Router is the prime factor of NOC architecture. The paper presents the implementation of Virtual Output Queue (VOQ) wormhole switch router architecture with new Signaling approach features. The implementation is obtained through VHDL coding of router blocks in behavioral fashion which are later connected in structural style to get the complete Virtual Output Queue (VOQ) router architecture. A new signaling mechanisms based communication protocol we introduce here in order to enhance the mapping between IP cores for QoS supports. A communication technique which is implemented in our design is to achieve less average latency of packets and maximum throughput. It provides low latency to the packets traversing inside the network.

Keywords: Router, Signaling Approach ,VoQ

1. INTRODUCTION

Microprocessor industry is changing from single-core to multi-core and consist of hundred to thousand or more identical cores arranged as chip multiprocessors, which needs efficient communications among all processors. Because of that SoC requires high-performance, scalable, flexible and user - friendly interconnection [1]. It is a big challenge to researchers how to provide efficient communication in SoC.

Network on chip (NoC) is a communication mechanism on an integrated circuit generally between IP and present hardware resources in SoC. It brings great improvements the over conventional communication method that was done by bus and crossbar interconnections methods for on-chip communication. It also improves the scalability of SoCs compared to other designs. Because of that it becoming an excellent alternative method for traditional on-chip communication architecture.

NoC consists of different components. Major components of NoC are routers, physical channels and network interfaces. The primary component in the communication infrastructure of NoC is the router with a set of bidirectional input output ports that linked to neighboring routers and it is also connected with the Intellectual Property (IP) core. Routers are interconnected with neighboring router by a pair of parallel opposite channels .The channels connected through the interconnecting link to form a given topology such as a ring , mesh, star or

torus network . Channels forwards data packets throughout the network from the source IP to the destination IP. A complete NoC architecture can be portrayed with different topology and by strategies. For example buffering, switching, flow control, routing and arbitration. These all parameters are very important factors in NoC design while Quality-of-service (QoS) is very critical issue and considerable factor for many run time applications where the hard real-time demand is presented[2]. In such kind of applications, the on-chip network needs to provide a competent service bounded by predefine transmission delays and communication throughput.

There are two working methods are available for NoC, the Packet switch and Circuit switch. Most of the existing NoC works on circuit-switching method for getting the adaptability and predictability in multi-cores system design [4,5,6,7]. But the majority of authors conclude that packet-switched on-chip interconnection networks will be essential to address the complexity of future SoC designs with various QoS requirements [3] [8,9,10].

The major part of NoC is router and most of the good service proving responsibility is depended on it . So, the router needs to adequately utilize the available bandwidth of the links to deliver communication data between IP cores and satisfies the different requirements for each service level. Different router architectures is existing and research is still going on. Authors in [14] have been presented packet-switch system based NoC router with QoS support. They use a priority based scheduler mechanism to solve conflicts between multiple connections with heterogeneous traffic flows and to minimize network latency whereas in [8] assigning different priorities to various data packets to achieve specified QoS targets , and exploring the advantages of wormhole routing and virtual channels .

In this paper we are elaborating the design and implement the new router architecture with a new signaling feature based communication protocol. This will allow the scalable data transfer and manage dynamically several communications in parallel. The complete paper is organized as follows. After the introduction we explorer the propose NoC router architecture with QoS support in section II. Section III is the signaling protocol mechanism, the RTL implementation of router architecture has described in section IV, Network topology and Routing algorithm that we prefer for the router test is in V, VI respectively . Results and the conclusion at the end.

2. VIRTUAL OUTPUT QUEUE (VOQ) ROUTER ARCHITECTURE WITH SIGNALING APPROACH

VHDL code is used to implementation and designing for blocks of router that include Virtual Output Queue (VOQ), scheduler and Demux . The Virtual Output Queue (VOQ) block consists of the control unit and memory block to store the data bytes. All of these blocks are then connected using the structural style of modeling to get the complete router blocks. The structural view of the router block is below :

The traditional method of forwarding traffic through a router is based on buffering ingress traffic in input queues on ingress interfaces, forwarding the traffic across the fabric to output queues on input interfaces, and then buffering datagrams again on the output queues before transmitting the traffic to the next hop. The traditional way of queuing packets on an ingress port is storing traffic destined for different egress ports in the same input queue (buffer). During periods of congestion, the router might drop packets at the egress port, so the router might dissipate resources transporting traffic beyond the switch fabric to an egress port, only to drop that traffic instead of forwarding it. And because input queues store traffic destined for different egress ports, congestion on the one egress port could affect traffic on a different egress port, a situation is called head-of-line blocking (HOLB).One excellent solution for this problem is Virtual output queue base router architecture. We use this in our router mechanism.

The basic approach of Virtual output queue (VOQ) architecture is as following :

- Instead of separate physical buffers for input and output queues, VOQ router uses the physical buffers on the ingress port of each Packet Forwarding Engine to store traffic for every egress port. Every

output queue in router on an egress port has buffer storage space mechanism on every ingress pipeline on all of the Packet Forwarding Engines on the router. The mapping of input port storage space to output queues is 1-to-1 mapping, so each output queue receives buffer space on each input port.

- Instead of one input queue containing traffic destined for multiple different output queues (a one-to-many mapping), each output queue in each router has a dedicated VOQ comprised of input buffers on every Packet Forwarding Engine that are dedicated to that output queue (a 1-to-1 mapping). This architecture prohibits communication between any two ports from affecting another port.
- Instead of storing traffic on a physical output queue until it can be forwarded, a VOQ does not transmit packets from the input channel across the fabric to the egress channel until the egress port has the resources to forward the traffic. A VOQ is nothing but a collection of input queues (buffers) that receive and store traffic destined for one output queue on one egress port. Each output queue on each output port has its own dedicated VOQ, which consists of all of the input queues that are sending traffic to that output queue.

A VOQ is a collection of input queues that receive as well as store traffic destined for one output queue on one egress port. Each output queue on each output port has its own dedicated VOQ, which consists of all of the input queues that are sending traffic to that output queue. Figure 1 shows VoQ Router Architecture [12].

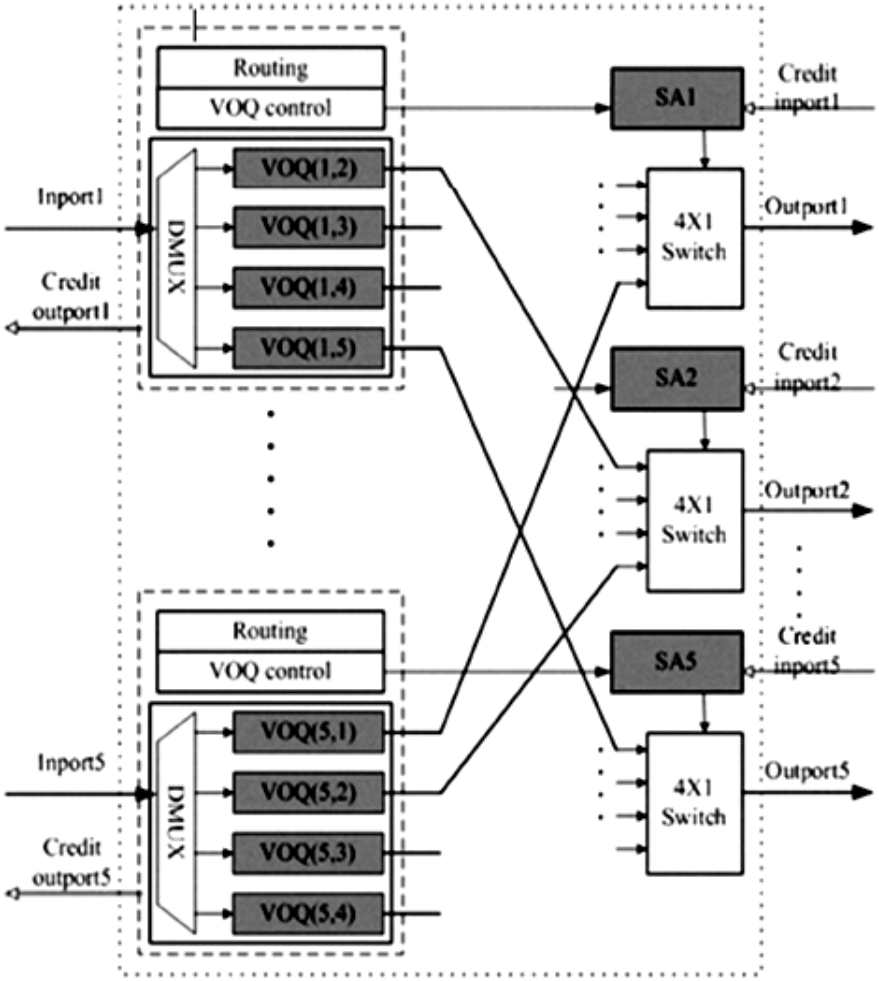

Figure 1: Router Architecture

3. SIGNALING BLOCK

Congestion in the context of NoC defines different states of network such as a node or link carries large data, traffic gets mixed with lots of other traffic , incoming packets arrive simultaneously for the same outgoing link. It may degrade the network service quality because of packets are delayed, no free space available in input buffer so packets are dropped, frame or data packet loss and the blocking of new connections, resulting in queuing delay means and jitter problem. In a congested network, response time slows with reduced network throughput. Lots of reasons are there for congestion occurrence. Suppose the bandwidth is not sufficient and network data traffic exceeds capacity then congestion will be created inside the network .Solution to avoid this is to divide the bandwidth between the network flows in a fairly manner. Authors [15] worked on this issue and propose a new distributed source-throttling congestion control mechanism. They focused on the congestion issue and tried to relieve the effect of congestion in buffer less NoC under high load traffic. This works presented as Cbufferless and they invented the new strategy for a novel congestion detection and control mechanism. They compute the average deflection rate of routing flit and distributed throttling message injection in advance. Because of this the congestion information can be directly obtained inside the node.

In our work a Signaling block introduce inside router to fight this problem. The signaling block perform some major task that is required to the signaling process in the network. It generates and broadcasts signaling information from asynchronous flits in order to update the neighboring routers data with new traffic load states. The important work of this block is to analyze newly received signaling flits in order to update the internal routing table. The information stored in this routing table for making the routing decision.

The block will be collected congestion information from neighboring port by checking status of virtual output queues. If the buffer has free space for storing packets it means no congestion is there otherwise congestion is presented. All neighboring blocks send its current status information to the signaling block through packet flit bit position. So this signaling block has the information of all neighboring block. This is required to manage a head-flit during the path establishment process.

In the signaling block , the signaling process is done by the generation of signaling flit .Singling flits information is nothing but the information of congestion present in neighboring router by checking the free buffer space availability of routers. Singling flits provides the congestion information of neighboring routers . Signaling block holds the neighboring routers information in an internal table which gets updated every time in

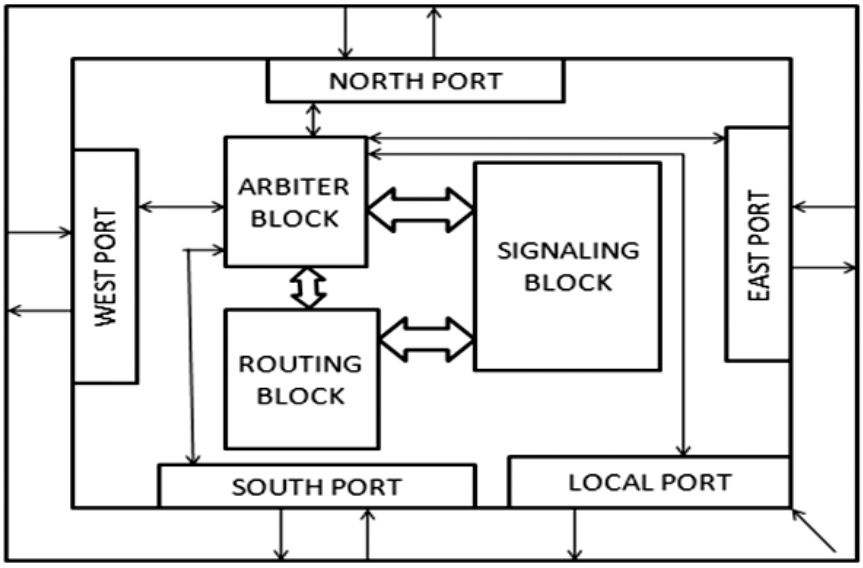

Figure 2: The proposed Router Architecture with Signaling block

case of incoming signaling flit. This information is required to the header flit management for the path establishment processes [11]. Signaling block directly connected to arbiter block and routing block. This information then forward to routing block. Routing block then decided the new route to forward the packets. It always prefers the free route where the no conjunction is present. Figure 2 shows the router architecture with signaling block.

4. IMPLEMENTATION OF RTL

Implementation starts with designing of VHDL codes for blocks of router that include Virtual Output Queue, Demux and Scheduler. The Router consists of different blocks such as Virtual Output Queue ,Routing block, Arbitration block , Memory block to store the data bytes and a new feature of Signaling block . All of these blocks are then connected using the structural style of modeling to get the complete router blocks. The RTL view of the router block is below:

5. NETWORK TOPOLOGY

Network topology provides the interconnection mechanism for various elements such as links, nodes, router etc. of a network. A network topology is the organization of a network, including its nodes and connecting lines. Router gets connected through any of the topology. Topology is an act as a major role in NoC while we consider the performance of NoC. So we studied all topologies in details , made the comparison of all on the basis of our requirement and finalized 2D Mesh topology. The mesh topology is very easy to implement and it is one of the

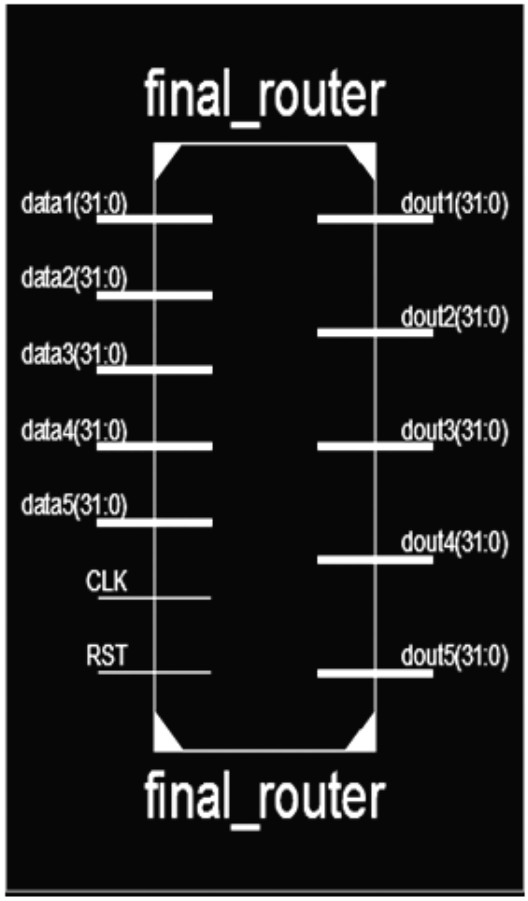

Figure 3: RTL of Router

most frequently preferable network topologies. Because of this simplicity router can be easily built through it . 2D have a simple M columns and N rows type of structure. The routers position is in the intersections of two wires and computational resources such as IP cores are connected near the routers. It is easy to determine the addresses of routers and connected resources as x-y coordinates in the mesh. All its nodes are in equally distance and it is consists of n numbers of different resources and switches. These are in equal form. Routers are connected to every resources and to the other routers through the interactive communication channel. Router has 5 input ports and 5 output ports. Routing is also easily manage through Mesh topology. Hence the implementation of NoC with Mesh topology is simple beneficial regarding space consumption because of low area uses. Mesh topology is impressive in the scalability. So if the designer wants to design NoC for specific application Mesh topology is suitable and scalable. So we prefer 2D Mesh topology for router connectivity.

6. THE ROUTING ALGORITHMS

Travelling path for the packets between source and target switches is defined by Routing algorithms. For exceeding performance of NoC, the network should restrict Live lock, Deadlock and Starvation problems. When the multiple nodes require to access the same set of resources cyclic dependency creates among the resources ,so no packets forwarding progress can be made, no matter what sequence of events happens and deadlock condition has occurred. Live lock situation creates packets circulating in the network without ever making any packet forwarding process to their destination place. Starvation creates if the packet in a buffer requests an output channel and it is blocked because the output channel is always engage for other packets.

Routing algorithms are categorized into three different criteria: 1. How a path is portray, 2. The length of the path , and 3. Where the routing decisions determined. Routing schemes has described in different several ways in different research work. One method is called Source routing. In this method the source node selects the whole path before forwarding the packet. The whole path is decided at the source switch which will be increasing the packet size because the header of the packet has to compulsory carry all the routing information while routing inside the network. Packet must carry the whole routing information this is the main limitation of this approach. In addition, the packets cannot be changed the path after the packet has left the source. Another simple alternate method is present that is distributed routing method. Here the router will take the routing decision as per scenario of the network .By receiving a packet router decides the route based on the destination address, whether it is delivered to the local resource or forwarded to another neighboring router. In another condition, a routing algorithm is invoked to decide which neighboring router the packet should be transferred. Source routing again have some limitation and was not suitable for very large and dynamic networks because of overhead on packet size. But for the small network it is likely to have good extensible performance with regular topologies. Example is the Mesh topology based NoC network. This may simplify the design of the router because of the routing information is directly available within the packet. We prefer here a simple XY routing algorithm which provides adaptive routing based on congestion condition.

7. RESULTS AND CONCLUSION

Table 1
Router result for 2D Mesh Topology

Topology	*Number of Slices*	*Number of Slice Flip Flops*	*Number of 4 input LUTs*	*Maximum Combinational delay*
2D Mesh	348	477	402	6.202ns

We have implemented a novel router architecture with applying new signaling features for efficient QoS supports .We have studied the basic router architecture and existing different router architecture. Analysis all

this existing architecture and find out limitation. We try to overcome this limitation through this work .This is our contribution to this area to develop new router architecture that will consider QoS support features. We test and verify the implemented new router architecture with x- y algorithm and found the results shown in the table 1 . This signaling feature preferred by some author in their work but they introduced this thing in the hardware manner. Limitation of this hardware is increasing cost as well as the size of the router. We try to introduce this feature in software manner and it successfully implemented.

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