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Voltage Stress Analysis of Cascaded Quasi Impedance Source Network Based DC/DC Converter Using SB Control

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ABSTRACT

To convert DC-DC with improved efficiency and reduced ripple free output, this paper uses quasi ZSI (Impedance Source Inverter) for reducing energy losses in the output by the introduction of the two stage quasi impedance source network (qZSI). The proposed two stage quasi Z source network possesses one diode, two capacitors, two inductors in addition to the conventional quasi ZSI. This paper proposes a new approach to the buck-boost DC-DC converter with high frequency, high boost factor and high voltage gain. Theoretical analysis of two operating modes ie shoot-through and non-shoot through mode of simple boost method is presented. The simulated results are presented and analyzed for various duty cycle and modulation index using simple boost pulse width modulation (PWM) technique by using MATLAB. Moreover, the proposed solution features over 31.67% duty cycle reduction 32.4% of increased boost factor(2 times higher boost factor) and provide 30% increased voltage gain(nearly fourfold boost) than two stage quasi Z source buck boost dc-dc converter by changing the overlapping of active states control technique.

Keywords: Impedance Source Inverter (ZSI), Pulse Width Modulation (PWM), full-bridge converter, VDR (Voltage Doubler Rectifier).

1. INTRODUCTION

In various industrial application such as distributed power systems, hybrid electric vehicles, special power supplies and servomotor drives, the traditional VSI and CSI were widely used to replace the traditional inverter. To overcome the problems in the conventional inverters, the Z source inverter was emerged in which bridge type inverter have been successfully combined with dc – dc converter.in addition it provides high efficiency, reliability and low cost for its buck –boost power conversion ability[1]-[3].

The advantage of shoot through state was utilized by gating focused, for the same component rating, shoot through duty cycle is greatly reduced for the same voltage boost ability. In other hand, for the same component rating, shoot through voltage conversion is greatly increased nearly fourfold boost of the DC input voltage due to the presence of VDR in the back end output side. As a modification of popular voltage fed Z source inverter(ZSI), voltage fed quasi Z source (qzsI) with continuous input current are discussed [4-6]. Dmitri vinnikov [7], provide two fold voltage boost of the DC input voltage with the overlapping of the active states control techniques.[10]were implemented with the an input voltage V_{in}= 40V the active duty cycle of active states ant the maximum shoot through duty cycle was set at $D_A = 0.5$ and $D_S = 0.5$ per switching period in order to achieve the increased power density of the single stage converter also VDR implemented at its output side for its voltage doubling effect of the peak voltage of the secondary winding of isolation transformer.

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To obtain a higher voltage gain with the same shoot through duty ratio D_S = 0.2 and the modulation index in the voltage fed Z source inverter compares with the traditional Z source inverter with input voltage of V_{in}= 230V to the output voltage of V_{out}= 295 (peak V) [11]. The resonant period to match with the switching period of converter due to the large variance of the leakage inductance TR_2 and resonant capacitor C_3 in order to achieve the highest efficiency. Due to the reduced conduction losses of active states and output diodes with the lower current stresses, the converter provide higher output voltage and to get higher efficiency[12].

Trinh et al. [13], dealt with addition of more capacitors and inductors with the conventional ZSI (Impedance Source Inverter) system. By doing this, voltage stress and voltage level can be improved. Even though there is addition of capacitor and inductor to the conventional system, the cost and shoot through ratio is maintained same as that of conventional one. Further, voltage boost ratio can be improved. In order to improve the voltage boost level, concept of switched inductor is used. The reduced shoot through ratio produces increase in voltage boost level. For realising the voltage boost level, Pulse Width Modulation (PWM) control method is used and also the design of passive components is explained. The SL and SC Z Source inverters are proved much higher gain and to keep their component stress on both lower and upper switch of phase leg to boost the dc bus voltage.

The shoot through states are eliminated when the DC input voltage is high and the qzs network based DC to DC converter starts to operate ie in the buck mode and in the conventional voltage source inverter when the front end DC voltage begins to reduce some below predefined value, qzs converter starts to working in the shoot through operating mode in order to achieve boost operating function. Hence qzs network based dc to dc converter working in the both operating condition ie buck-boost mode. This paper lower[14].For renewable and alternate energy source qzsI is an attractive converter for its unique advantage of lowercomponent rating s and constant dcCurrent from the source[15].

Theimproved inverter [16] has a higher modulation index M with reduced V stress on the dc link and current stress flow to the diode and transformer winding also lower input current ripple for the same transformer turn ratio and input and output voltage for the fixed modulation index M with reduced size Depends of problem and application under consideration on which select the controlling techniques because

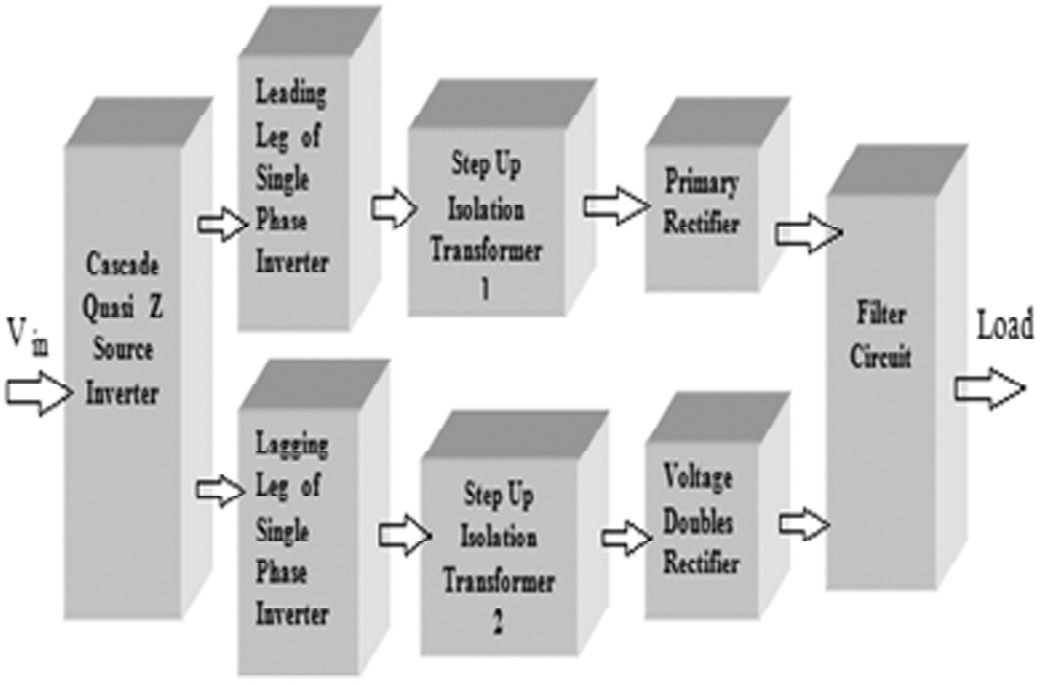


Figure 1: Structure of DC-DC Converter with Cascaded qzsI

each technique has its own advantages and disadvantages and weight of the modulation index. For renewable and alternate energy source qzsI is an attractive converter for its unique advantage of lower component rating s and constant dcCurrent from the source[16].

The coupled inductors in primary switches are used to achieve load current. The input voltage in circulated energy was reduced and also conduction in the system was also reduced. In current load path, inductor does not emerge as a series inductance. In output rectifier, high voltage and duty cycle loss will not affect the proposed system. So, it provides higher efficiency than the conventional converter with small loads.

2. BASIC STRUCTURE OF CASCADE DC/DC CONVERTER

In Fig. 3 the basic block diagram of hybrid dc-dc converter with qZSI is shown. Here, DC supply is given to impedance source network in order to provide wide range of voltage than the traditional voltage or current source inverter. The output from impedance network is given to leading or lagging leg of single phase inverter depending on type of output from network. The fundamental voltage and current can be controlled through use of single phase inverter. In many applications, a constant or adjustable voltage is required.

So, in order to meet those requirements, a single phase inverter is used. The controllable AC output from inverter is stepped up by isolation transformers. Isolation transformers provide isolation of power device from power source and also it protects devices from electric shock or electric stress.

The primary rectifier is used to convert AC to DC and given to filter circuit in order to eliminate ripples in output. The voltage doubler rectifier is used to produce twice as that of input voltage at output terminals. The filter circuit consists of combination LC circuit or output capacitors. It is used to select desired range of frequencies. The voltage doubler is used to improve the level of voltage to a required level and get filtered to reduce the ripples. Ripple free pulse is given to load circuit. So, it results improved quality of output. Thus, efficiency of system gets improved than the conventional method.

In above figure, input current flows I_{in} through the coil L_1 and shunt current I_{sh} flows through the switches. Based on the boosting factor, the level of input voltage can be increased or decreased by the use of impedance network. This network requires capacitance and inductance in small size and also it acts as a second order filter.

Assuming that quasi impedance network inductors L_{i1} and L_{i2}--and capacitors C_{i1} and C_{i2} have same inductance (L) and capacitor (C) respectively, the quasi impedance source network becomes symmetrical. Using symmetry condition and equivalent circuit, we have

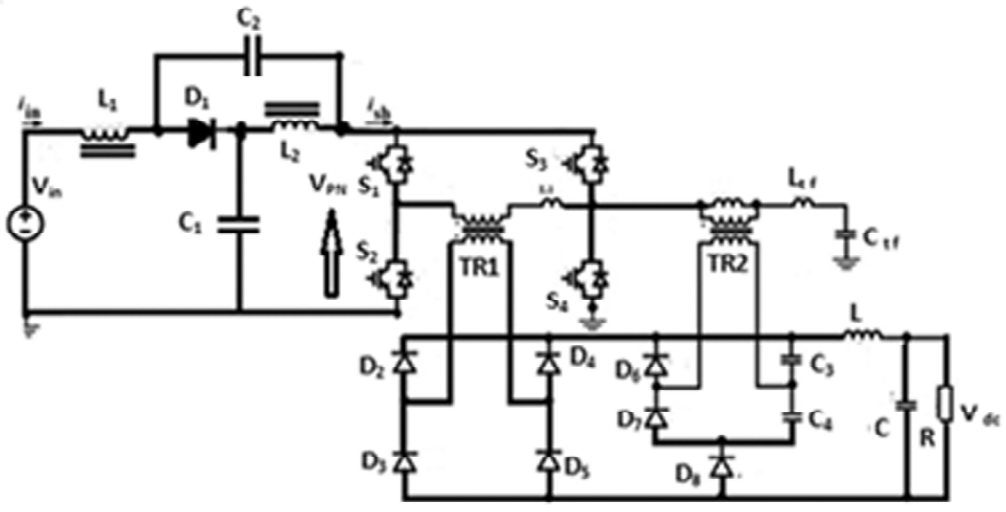


Figure 2: Proposed System for Single Stage

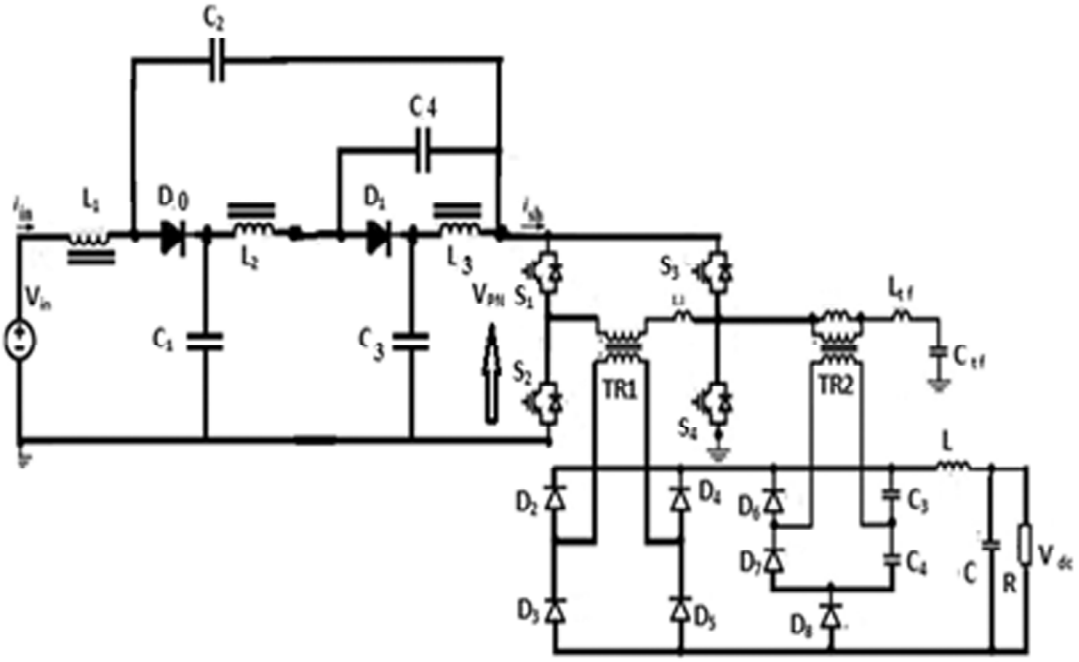


Figure 3: Proposed System For Cascaded Stage

$$V_{Ci1} = V_{Ci2} = V_C \; ; \; V_{Li1} = V_{Li2} = V_L \tag{1}$$

By observation of quasi impedance source dc-dc converter, the shoot through zero state for an interval of shoot through state interval T_{ST} during a switching cycle T_S-can be reduces to the equivalent circuit, Fig. 2 has

$$V_L = V_C \; ; \; V_d = 2V_C \; ; \; V_i = 0 \tag{2}$$

Consider that the quasi Z source Inverter Bridge in any one of non shoot through states for an interval of T_{NST}.

Hence from the equivalent circuit, Fig. 1 has

$$V_L + V_C = V_{in} \; ; \; V_L = V_{in} - V_C \; ; V_d = V_{in}$$
$$V_i = V_C - V_L = 2V_C - V_{in} \tag{3}$$

Where V_{in} is input dc voltage.

The average inductor over one switching period (TS)Should be zero, from equation (2) and (3), we get

$$V_L = \frac{T_{ST} V_C + T_{NST} \left(V_{in} - V_C \right)}{T_S} = 0 \tag{4}$$

or

$$\frac{V_C}{V_{in}} = \frac{T_{NST}}{T_{NST} - T_{ST}} \tag{5}$$

Across the inverter bridge, average dc link voltage can be found as follows,

$$V_i = \frac{T_{NST}}{T_{NST} - T_{ST}} V_{in} = V_C \tag{6}$$

Similarly, from (3), the maximum dc link voltage across Inverter Bridge can be rewritten as,

$$V_i = V_C - V_L = 2V_C - V_{in} = \frac{T_S}{T_{NST} - T_{ST}} V_{in} = BV_{in} \tag{7}$$

Where T_{ST} = Duration of shoot through state

T_{NST} = Duration of non shoot through state

T_S = operating period i.e. switching cycle

$$T_S = T\text{-}_{ST\text{-}} + T_{NST} \tag{8}$$

$$B = \frac{T_S}{T_{NST-T_{ST}}} = \frac{1}{1 - \frac{T_{ST}(1+n)}{T_S}} = \frac{1}{1 - D_{ST(1+n)}} \geq 1 \tag{9}$$

Where n is number of stages

If n = 1 for traditional QZSI that is for single stage QZSI

$$B = \frac{1}{1 - 2D_{ST}} \geq 1 \tag{10}$$

DST is duty cycle of the shoot through state

$$D_{ST} = \frac{T_{ST}}{T_S} \tag{11}$$

The modulation index of QZS main circuit will be decreased to a very low level and it can be expressed as,

$$M \leq (1 - D_{ST})$$

Where M is modulation index

$$\text{M} = \frac{\text{Amplitude of Modulation Waveform}}{\text{Amplitude of Carrier Waveform}}$$

From (7),

$$V_i = B.V_{in} \tag{12}$$

The equivalent dc link voltage of inverter is the maximum dc link voltage. Hence, the phase voltage of QZS inverter can be expressed as,

$$V_{dc} = V_i \tag{13}$$

$$V_{dc} = B.V_{in} \tag{14}$$

Resulting from shoot through state *B* is the boost factor. The equivalent dc link voltage of inverter is the maximum dc link voltage. Hence, phase voltage of QZS inverter can be expressed as,

$$V_{dc} = M.\frac{V_i}{2} \tag{15}$$

Using equation (7) & (12), equivalent dc link of inverter can be further expressed as,

$$V_{ac} = M.B.\frac{V_{in}}{2} \tag{16}$$

Above equation further expressed as in terms of buck- boost factor

$$V_{ac} = B_B.\frac{V_{in}}{2} \tag{17}$$

Where B_{BB} is buck boost factor

$$B_{BB} = M.B = \left(0 \approx \infty\right) \tag{18}$$

The QZSI based dc-dc converter starts to function as traditional VS based dc- dc converter without shoot through condition, when input voltage is high enough, thus performing only buck function of the input voltage. From (1), (5) & (10), the capacitor voltage can expressed as,

$$V_{C1} = V_{C2} = V_C = \frac{\left(1 - D_{ST}\right)}{\left(1 - 2D_{ST}\right)}.V_{in} \tag{19}$$

Note that the Boost factor B in (10) can be controlled by shoot through duty cycle D_{ST} which can be decided by interval of shoot through time T_{ST}. Also, buck boost factor B_{BB} is determined by the modulation index M and boost factor B. In simple boost method Pulse Width Modulation (PWM) techniques the modulation index M can be determined by the ratio of the amplitude of the modulation waveform to amplitude of the carrier waveform.

The voltage conversion ratio of QZS inverter can be expressed as,

$$G = V_{ac} = M.B\frac{V_{in}}{2};\ G = \frac{V_{ac}}{\frac{V_{in}}{2}} = M.B \tag{20}$$

Hence From (1) & (14), the quasi impendence network can perform the step-up dc–dc conversion from V_{in} to V_{dc}, thus the numerical condition D_{ST} is limited to,

$$0 \le D_{ST} \le 0.5 \tag{21}$$

$B = \frac{1}{1 - D_{ST}\left(1 + n\right)} \ge 1$; Where n = 2 for 2 stage

$$B = \frac{1}{1 - 3D_{ST}} \ge 1$$

$$D_{ST} \le 1/3 \tag{22}$$

3. SB PWM CONTROL

The block diagram of gating signal generator is shown in Fig. 4. The various input pulses such as sinusoidal and ramp is compared with relational operator. The Pulse Width Modulation (PWM) signals are generated and part of output is inverted through logic gates to perform the control process of active and zero states. Thus, inverted output signal is given to thyristor switches T_1 and T_3 to turn ON. The relational operators used to analysis and compare the amplitude of various signals given as an input. The Pulse Width Modulation (PWM) with logic gates and comparator provides the control circuit for active and zero states.

The OR gates are used to perform addition of active and shoot-through states. Therefore, switches S_2 and S_4 get operated according to the gating signals. The shoot through states is controlled by comparator signals. The control from PWM signal is given as the input to logic gates which operates the switches. The

upper and lower level signals output are compared with the help of comparator. The output from comparator is given to logic OR3 and given as one of the input to OR1 and OR2. The resultant is used to operate switches S2 and S4.The generation of shoot through pulses are given by Fig. 5.

The upper and lower shoots through pulses generated are shown in figure. The peak of pulses is produced with reference DC line voltages. The lower and upper shoot through pulses are generated by comparing with the reference signal or saw tooth waveform. The lower shoot through pulses are produced as a inter-mediate pulses of upper shoot through pulses.These waves are modified and combined in order

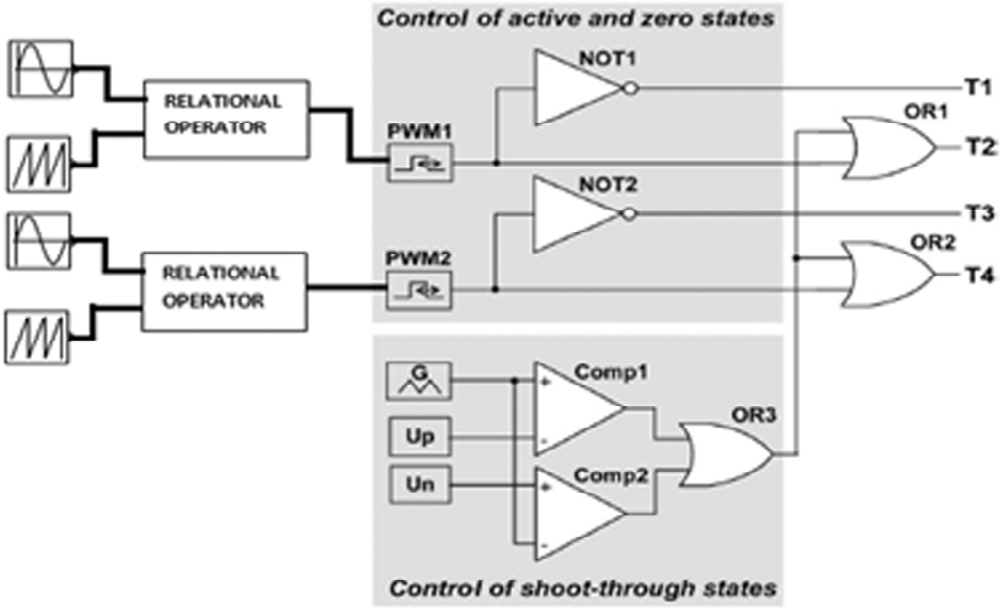


Figure 4: Generalized Block Diagram of Gating Signal Generator

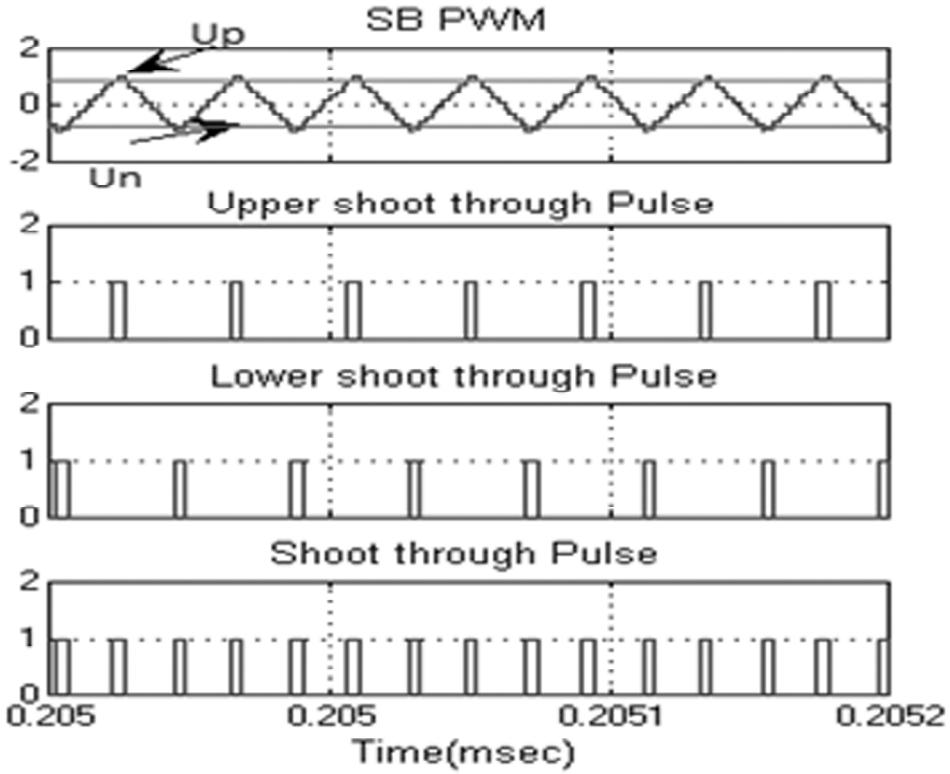


Figure 5: Generation of Upper And Lower Shoot Through Pulses

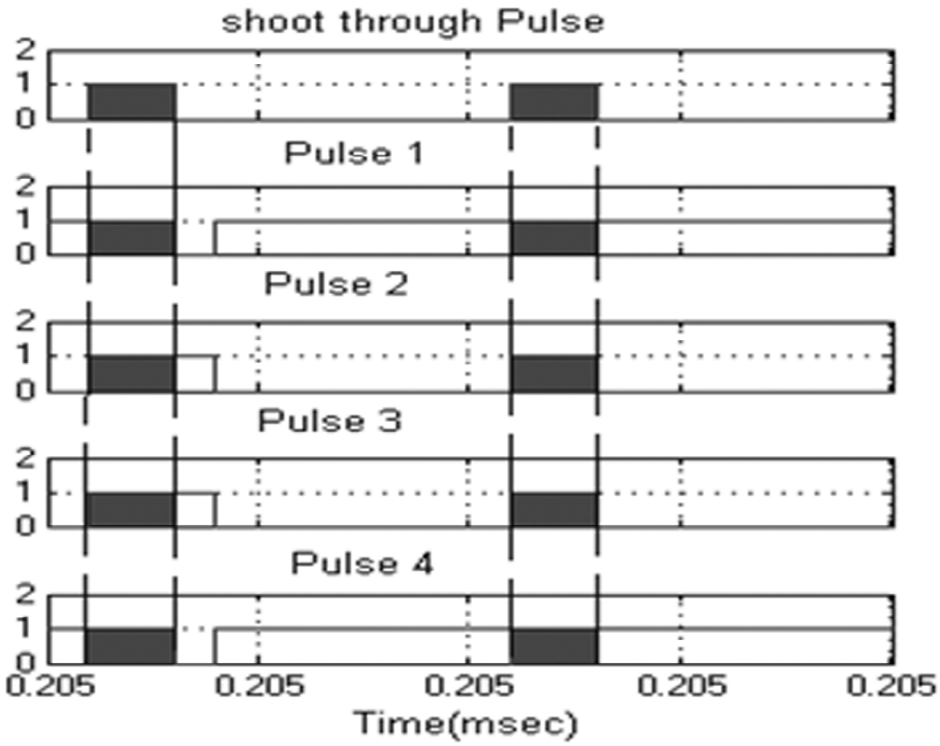


Figure 6: Pulses of Various Switches

to reduce cost and reliability. Thus, the efficiency of power conversion can be greatly increased. In Fig. 6 various (S_1, S2, S3 & S_4) pulses are generated based on input given by the gate signal. At any instant two pulses starts at same time period and remaining two pulse remains in zero position for small interval of time.

4. SIMULATION RESULTS AND DISCUSSION

The parameters used in simulation are shown in Table.1 by using parameters during simulation, the results are taken for various operating condition for boost factor and voltage gain. The simulation results for single stage qzsi converter and cascaded stage qzsI converter are shown in the Table 2 and Table 3 respectively. By using various duty cycle ratio and modulation index condition, the results are taken for simple boost control condition.

As in [8], V_{in} = 40V, D_S = 0.25; M = 0.75 showed that the qzsI provide the voltage gain of B_{max} = 2 for both the shoot through generation during freewheeling state and zero states. When using a generation of shoot through state by overlapping method for cascaded qzsI as shown in [9], to produce a output voltage 80V, the demanded voltage boost is B_{max} = 2 for the shoot through duty ratio D_S = 0.167, modulation index M = 0.833. Mat lab simulation compares it with the cascaded qzsI in [7].when using the SB control method the following simulation parameters are selected for the converters $L_1 = L_2 = L_3$ = 3mH, $C_1 = C_2 = C_3 = C_4$ = 20uF, R = 47Ω.

To demonstrate the waveforms the input voltage is set to 40V, switching frequency was f_S = 47.6 KHz.

To produce same 100V dc output voltage with the SB control of proposed control of cascaded converters with input Voltage V_{in} = 40, shoot through duty ratio D_{ST} = 0.205, modulation index M = 0.795 with voltage gain G = 2.5 and the boost factor B = 2.597 in the simulation. As in single stage qzs converter same output voltage was obtained for the duty cycle D_{ST} = 0.3, M = 0.7 with reduced voltage stress spike across the impedance network capacitance.

Table 1
Simulation Parameter.

V_{in}	40V
L_1, L_2& L_3	3 m H
C_1& C_2	20 µF
C_3 &C_4	20 µF
C_0	20 µF
L_0	0.2 m H
R_0	47&!
f_s	47.66KHz
D_{ST}	0.205
V_{dc}	100V
I_{dc}	2.1A

Table 2
Simulation Results For Boost Factor And Voltage Gain In Various Operating Condition For Single Stage

V_{in}	D_{ST}	M	B	G	V_{dc}	
					Simu	*Calc.*
	0.1	0.9	1.25	1.125	45	50
	0.2	0.8	1.667	1.33	65.2	66.62
40V	0.205	0.795	1.69	1.34	66	67.6
	0.25	0.75	2	1.5	77	80
	0.3	0.7	2.5	1.75	100	100
	0.4	0.6	5	3.0	200	200
	0.45	0.55	10	5.5	400	400

Table 3
Simulation Results For Boost Factor And Voltage Gain In Various Operating Condition For Two Stage

C	D_{ST}	M	B	G	V_{dc}		Io
					Sim	*Calc.*	
	0.1	0.9	1.428	1.318	52.72	57.12	1.3
	0.2	0.8	2.5	2.3	92	100	1.9
40	0.205	0.795	2.597	2.5	100	103.6	2.1
	0.25	0.75	4	3.75	150	160	3.2
	0.3	0.7	10	9	360	400	3.5

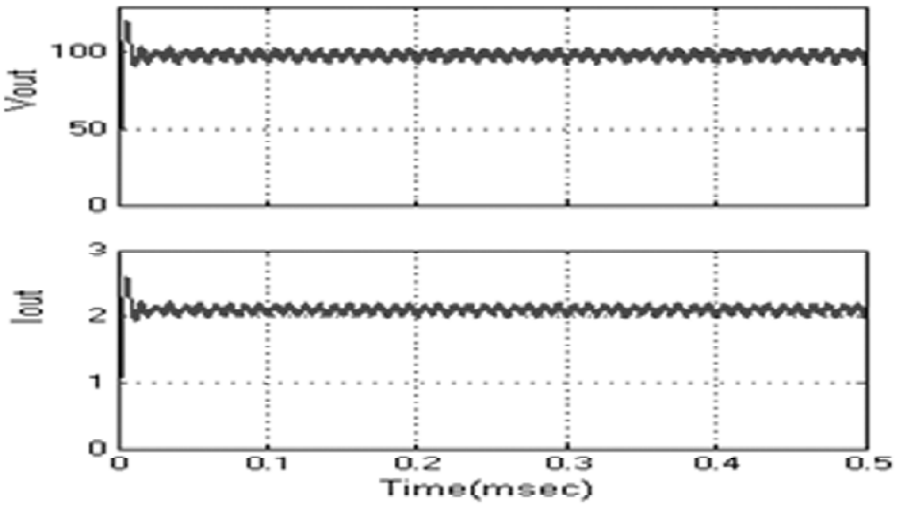


Figure 7: Simulated waveforms of DC Output Voltage Output Current for input voltage V_{in}=40V; D_{ST} =.205; M =0.795

5. VOLTAGE STRESS

One can increase the shoot through duty ratio or the modulation index, to increase voltage gain of the qzsI. Table 4 & 5 shows the simulation result for the case study. It can be shown in Fig. 9, the qzsi ensuring the increased voltage boost of B = 2.597 and voltage gain G = 2.5 with the Shoot through duty ratio D_{ST} = 0.205. Thus the capacitor voltage V(C1), V(C2), V(C3), V(C4) were 69.5V,44.5V, 89V, 24V respectively. Which is almost match with the calculated values. Table 4.show the voltage stress across the various capacitors for the various shoot through duty ratio D_{ST} for n = 2

$$V_{c1} = V_{in}\frac{(1-2D_{ST})}{(1-(1+n)D_{ST})} = 61.5V; \tag{23}$$

$$V_{c2} = V_{in}\frac{2D_{ST}}{(1-(1+n)D_{ST})} = 42.59V; \tag{24}$$

$$V_{c3} = V_{in}\frac{(1-D_{ST})}{(1-(1+n)D_{ST})} = 82.59V; \tag{25}$$

$$V_{c1} = V_{in}\frac{D_S}{(1-(1+n)D_{ST})} = 21.29V; \tag{26}$$

Thus (27) has to be get a hold to the boost method engaged [1]

$$\text{Simple boost: } M \le (1\text{-}D_{ST}) \tag{27}$$

Symbol D_{ST} is used to involve a steady state. As a outcome, altering D_{ST} or M will force a constraint on the other factor, which make matters worse and challenging to design the controller. Because of escalating voltage stress across devices, which results in elevated component rating for a large D_{ST} but a small M.

Notice that, the crest phase voltage of the inverter in steady state, can be written as

$$V_{p-crest} = \frac{1}{2}.\frac{V_{in}}{(1-2D_{ST})}.M \tag{28}$$

the correlation between the input voltage and the capacitor voltage can be expressed as (26) by (28) and

Dividing (23) to (26) by (28) results in

$$\frac{V_{C1}}{V_{p-crest}} \ge 2\frac{(1-2D_{ST})}{M} \tag{29}$$

$$\frac{V_{C2}}{V_{p-crest}} \ge \frac{4D_{ST}}{M} \tag{30}$$

$$\frac{V_{C3}}{V_{p-crest}} \ge 2\frac{(1-D_{ST})}{M} \tag{31}$$

$$\frac{V_{C4}}{V_{p-crest}} \ge 2\frac{D_{ST}}{M} \tag{32}$$

Referring to (27) & (29) to (32) the capacitor voltage inequality for SB control technique can be derived as

$$V_{C1} \ge 2\frac{(1-2D_{ST})}{M}.V_{p-crest};\ 0.1 \le D_{ST} \le \frac{1}{n} \tag{33}$$

$$V_{C2} \geq \frac{4D_{ST}}{M}.\ V_{p-crest};\ 0.2 \leq D_{ST} \leq \frac{1}{n} \tag{34}$$

$$V_{C3} \geq 2\frac{(1-D_{ST})}{M}.\ V_{p-crest};\ 0.1 \leq D_{ST} \leq \frac{1}{n} \tag{35}$$

$$V_{C4} \geq 2\frac{D_{ST}}{M}.\ V_{p-crest};\ D_{ST} = \frac{1}{n} \tag{36}$$

Where n is considered as a no of stages, in this paper n = 2 for cascaded qZS network as described equation (33) to (36) involve that, the voltage across various capacitance V_{C1} to V_{C4} above the $V_{P\text{-}crest}$ at

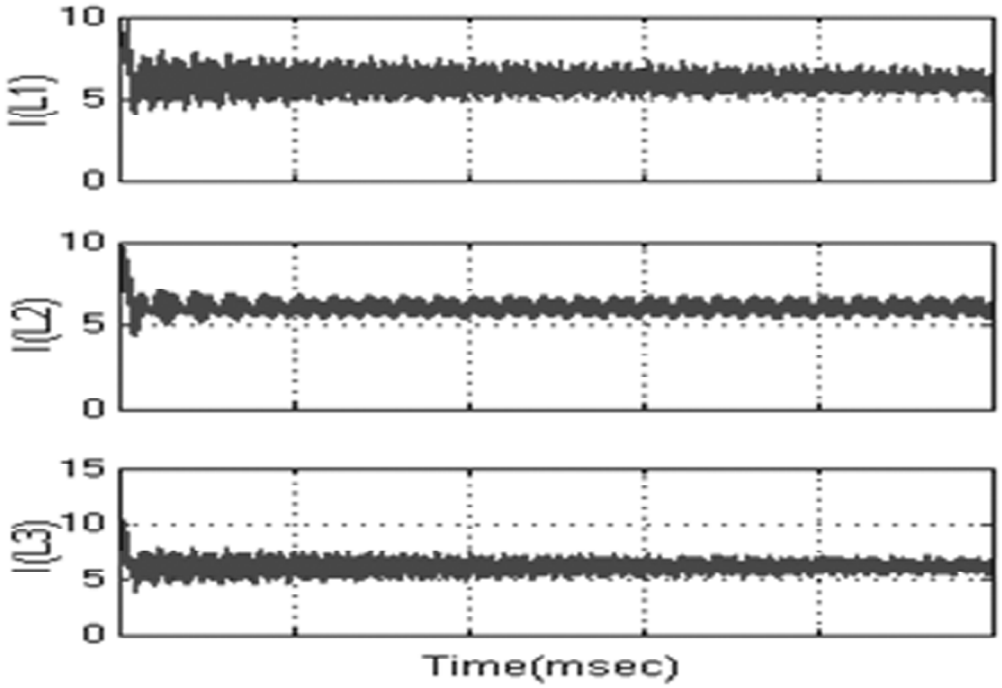
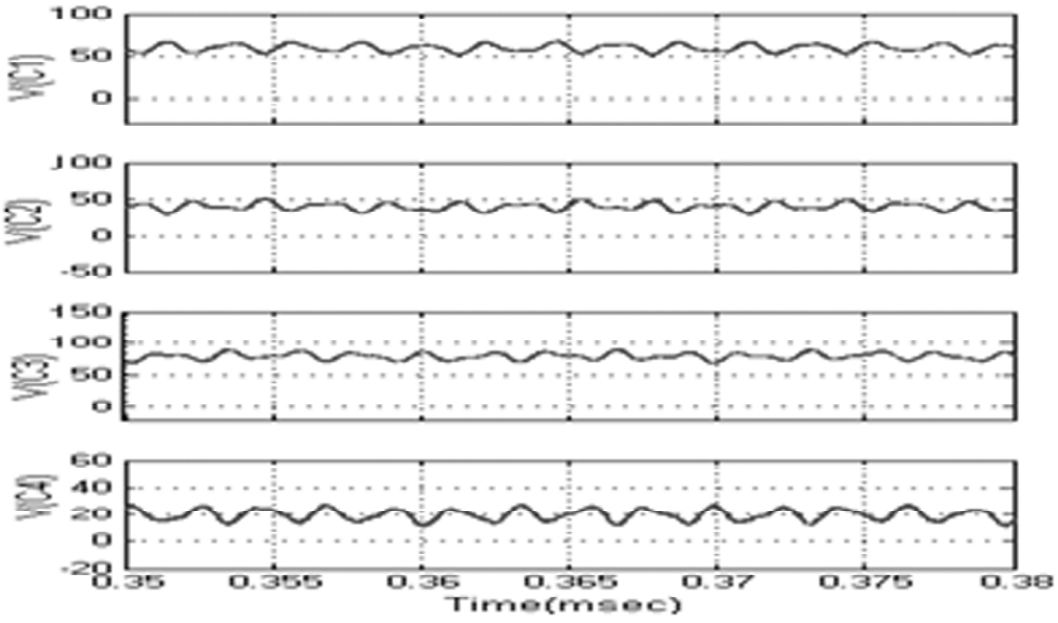
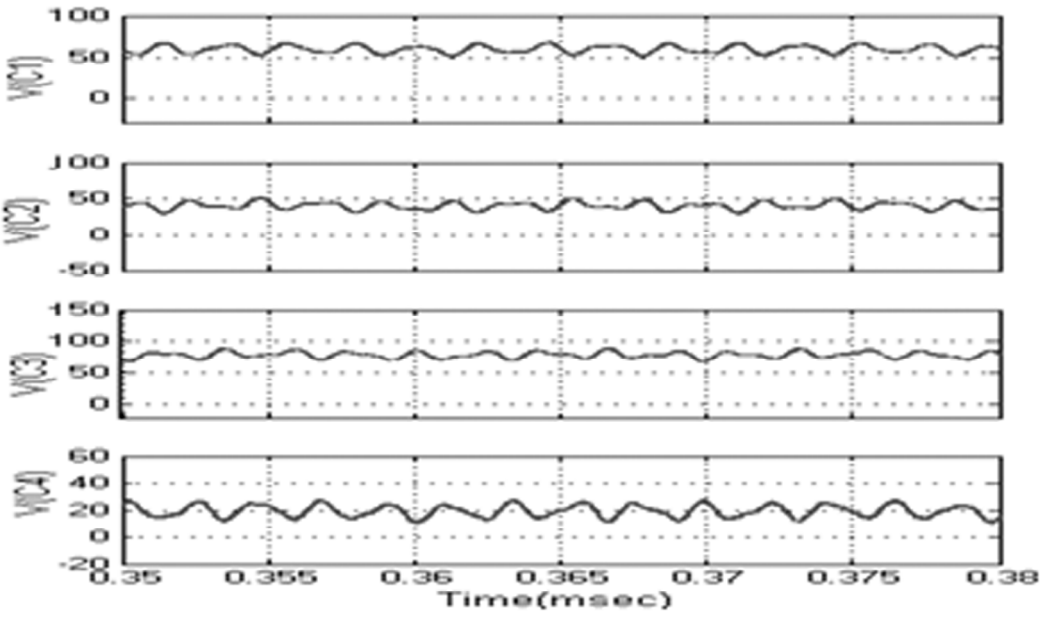


Figure 8: Simulated waveforms of operating voltage of capacitor L1, L2,&L3 during the minimum input voltage V_{in}=40V;D_s=.205.



(a)



(b)

Figure 9 (a): of Simulated waveforms of operating voltage of capacitor C1, C2, C3 & C4 during the minimum input voltage V_{in}=40V; D_{ST} =.205 (b) Zoom in view

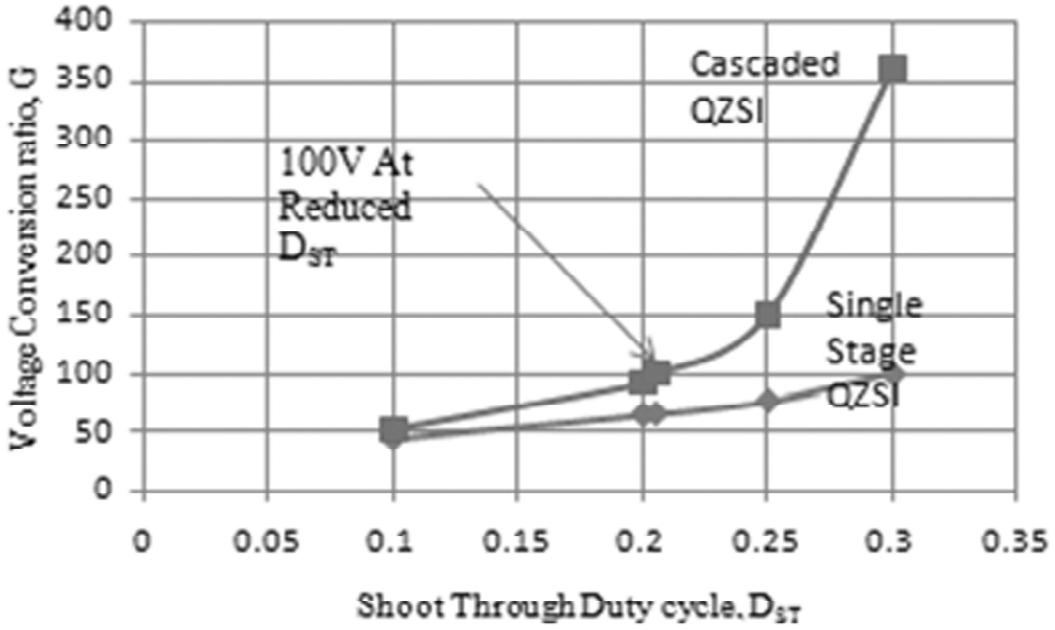


Figure 10: Relationship between D_{ST} and G for n = 1 & n = 2

the most within the given shoot through duty ratio. It lead to lowest voltage stress across devices with the range of D_{ST} as mentioned in the equation from equation (33) to (36), that can be shown in Fig.9a & 9b

In Fig.7, we can see that the simulated and boosted output voltage for the input voltage of 40V. From top to bottom in Fig.8 clearly indicate the three inductor current of L_1, L_2 and L_3. Table.4 & 5 shows the simulation result of the capacitor voltage for various shoot through duty cycle that shows the capacitor voltage of (VC1) 69.5V, (VC2) 44.5V, (VC3) 89V, (VC4) 24V for D_{ST} =0.205 demonstrate the low capacitor requirement in the proposed converter which is lesser or acceptable level compared to that (VC1) 69.5, (VC2) 3V while D_{ST} =0.3 as in the single stage qzsI dc/dc converter.

Table 4
Calculated & Simulated various Capacitor Voltages For Various Shoot Through Duty Cycle For Two Stage

V_C	mode	D_{ST}=0.1	D_{ST}=0.2	D_{ST}=0.205	D_{ST}=0.25	D_{ST}=0.3
V_{C1}	cal	45.69	60	61.5	80	160
	sim	53.8	57.7	69.5	72	165
V_{C2}	cal	45.7	40	42.59	80	160
	sim	19.3	33.6	44.5	77	175.3
V_{C3}	cal	51.43	80	82.59	120	280
	sim	59.4	72.36	89	117	216.1
V_{C4}	cal	5.71	20	21.29	40	120
	sim	14.5	18.94	24	38	128.1

Table 5
Comparisons of Capacitor Voltages For Various Shoot Through Duty Cycle For Single Stage and Two stage

V_C	stage	D_{ST}=0.1	$D_{S\,T}$=0.2	D_{ST} =0.205	D_{ST} =0.25	D_{ST} =0.3
V_{C1}	1	44.8	52.89	54	62	69.5
	2	53.8	57.7	42.59	72	165
V_{C2}	1	4.9	14.12	4.1	22	29.8
	2	19.3	33.6	44.5	77	175.3
V_{C3}	1	-	-	-	-	-
	2	59.4	72.36	89	117	216.1
V_{C4}	1	-	-	-	-	-
	2	14.5	18.94	24	38	128.1

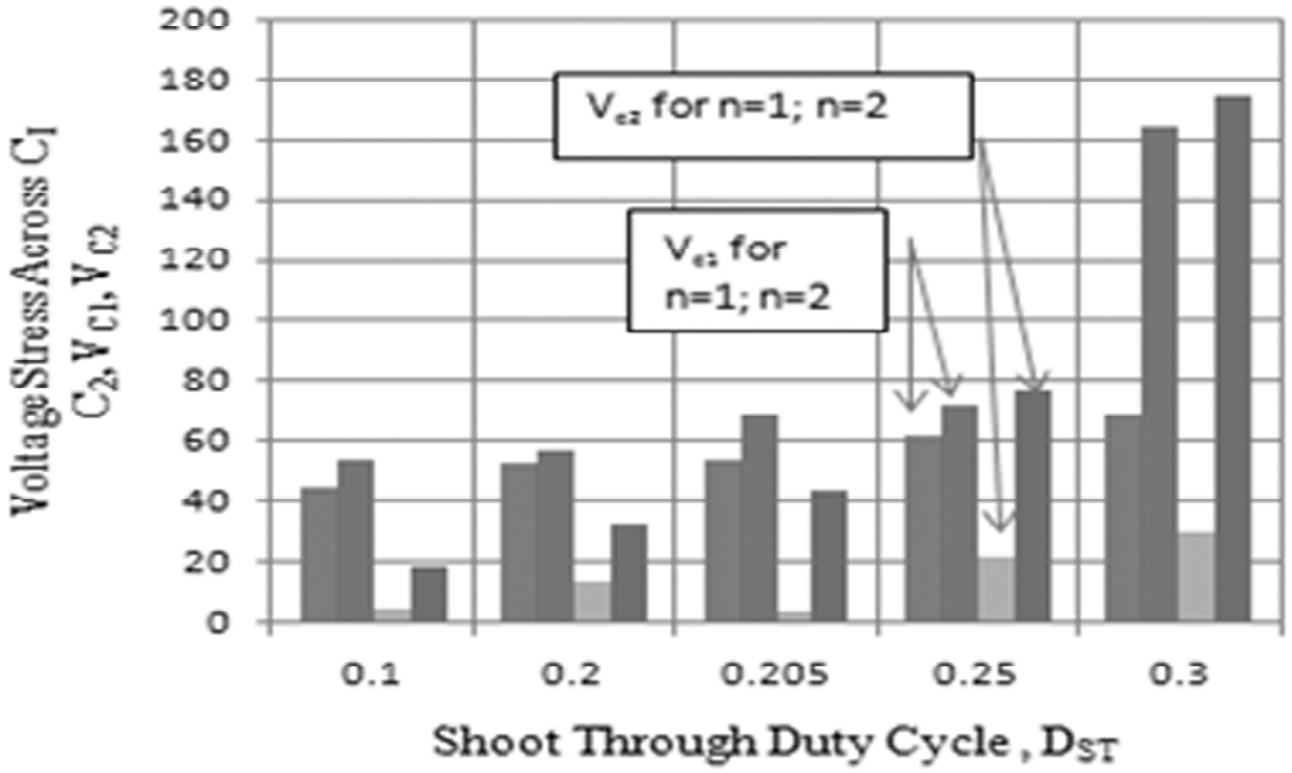


Figure 11: Relationship between D_{ST} and Voltage stress across C_1 to C_2 for n=1 & n=2

Furthermore Fig.11 & 12 shows the capacitor voltage simulation outcome that reduced voltage stress across the capacitors with increased voltage gain and boost factor for the same output voltage in support of reduced shoot through duty ratio D_{ST} = 0. 205 and the modulation index M=0.795. Thus the main objective is to reach high efficiency and higher power density with simple structure. This enhanced technique of could be a good solution for the performance of impedance source inverter and promoting their future industrial application.

6. CONCLUSION

The simple boost through PWM scheme is comprehensively analyzed in DC/DC converter and their performances are obtained in simulation. By using quasi ZSI, the energy losses can be greatly reduced in output. While converting ac-dc, it contains energy loss that also reduced in this method The proposed cascaded quasi Z Source network converter with two transformer, primary rectifier and VDR has a higher modulation index, lower shoot through duty cycle with high output voltage gain, high boost inversion ability and reduced voltage stress flow to the transformer winding and diode when compared with single stage converter for same PWM techniques. If the modulation index is kept fixed voltage spike across the impedance network capacitance are prominently reduced. Further, the output ripples can be reduced by use capacitors to improve the efficiency of output. The Z source inverter based DC/DC can be extended to any topology with suitable rectifier and modulation strategies.

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