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Implementation of Clock and Data Recovery Circuit Using dual slope phase Frequency Detector

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Abstract : In this paper the acquisition time of Phase Locked Loop (PLL) in Clock And Data Recovery Circuit (CDR) is reduced by using a dual slope Phase Frequency Detector (PFD).

Methods/Statistical Analysis : In proposed technology dual slope Phase Frequency Detector (PFD) has two tuning loops, a fine-tuning loop and a coarse-tuning loop. Fast convergence is due to coarse- tuning loop, and a fine-tuning loop is used to complete fine adjustments.

Findings : In cadence environment the clock and data recovery circuit block has been simulated using spectre simulator under 180nm technology. PLL is operated at 1GHz using 2.5V as supply voltage. In Clock and data recovery architecture the PLL acquisition time was measured to be 350ns and jitter reduces by 20% which is 20ps due to fine tuning of dual slope PFD. Power dissipation of proposed circuit is 240mW. Application: This fast locking PLL is used in a CDR circuit which plays an important role in backplane routing and optical communication.

Keywords : Phase Frequency Detector(PFD), Phase Locked Lop (PLL), Clock and Data Recovery(CDR) , Voltage Controlled Oscillator (VCO), acquisition time.

1. INTRODUCTION

Clock And Data recovery circuits (CDRs) played an important role in data communication systems where it has a wide range, which includes backplane routing, optical communications disk drive read channels and chip-to-chip interconnects. In our applications increased data transfer efficiency is important since data are sent in bursts to the destinations through backplanes or combinatorial cross point switches. The ratio of data transferred to the overhead plus data transferred is data transfer efficiency If the bursts are short, fast acquisition times are needed to achieve high efficiency. Fast acquisition CDRs tend to have higher jitter thus more coding is required to correct for bit errors, and thus efficiency gets limited[3],[4],[9],[7],[8]. A dual slope phase frequency detector (PFD) significantly increases acquisition range and thus PLL speed increases, compared to a conventional PLL using phase detector [1],[2],[3]. This paper describes a fast acquisition CDR by using which optimum data transfer efficiencies regardless of burst size is achieved. Thus data transfer efficiency of combined CDR is higher than the maximum of the CDR.

Phase locked loop (PLL) is the heart of the many modern electronics as well as communication system. The most versatile application of the phase locked loops (PLL) is for clock generation and clock recovery in communication systems. In this paper, proposed design based on a dual-slope phase frequency detector (PFD) and charge-pump technology which helps the PLL to achieve a fast locking in[1],[7],[8],[9]. A fine-tuning loop and a coarse-tuning loop, these two tuning loops are used in proposed technology. A coarse-tuning loop is used for fast frequency lock to accelerate the lock time and complete fine adjustments are done by a fine-tuning loop[1],[5],[6].

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2. CONVENTIONAL CIRCUIT

The lag and lead control signal is generated by PFD and this is comparing different clock phase output of Voltage Controlled Oscillator (VCO) and data input phase in the phase locked loop. The circuit operates under 2.5V.

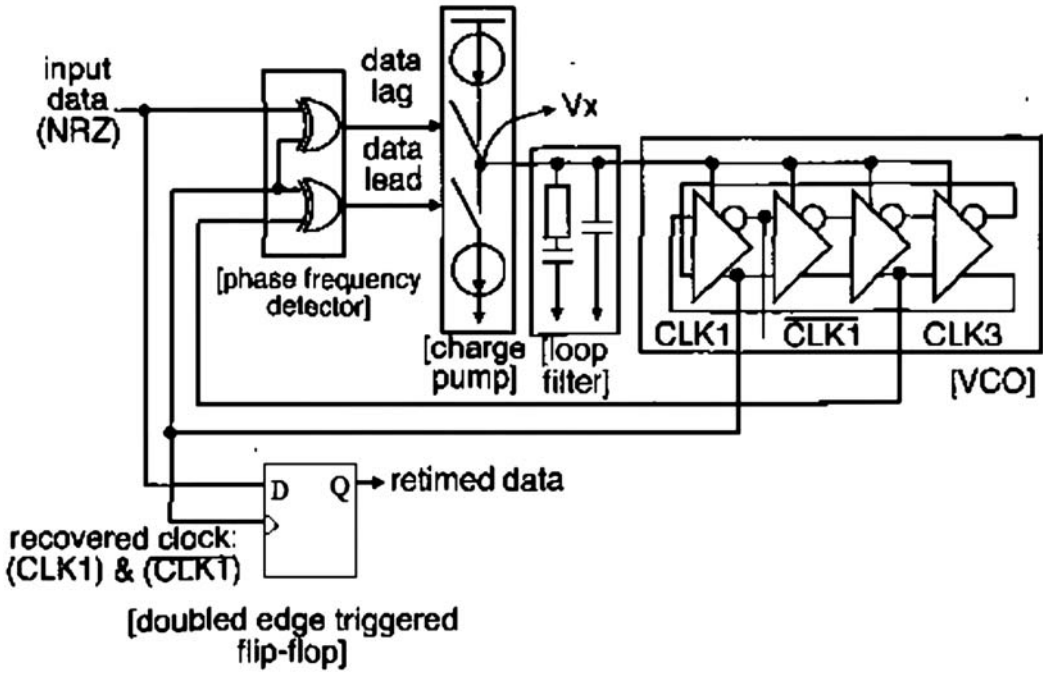

Figure 1: Clock and Data Recovery circuit

It is very difficult to design high-speed CMOS clock and data recovery circuits in data communication systems since the Phase Frequency Detector (PFD) in this simple conventional PLL uses two XOR gates which has problem in phase detecting and frequency detecting simultaneously [2]. This difficulty is overcomed in proposed circuit where data recovery circuit (CDR) that requires high-speed multi-phase clock generation and the ability to detect phase and frequency variation simultaneously. The architecture of conventional CDR with two XOR gate in Phase Frequency Detector is shown in Fig.1[2]. Phase Frequency Detector comprises of two XOR which have an output of lead and lag. The output current of charge pump and the control voltage of VCO are controlled by these two lead and lag inputs from PFD. These combine to cancel the phase and frequency error between the input data and recovered clock. The recovered clock is generated by four stages of VCO .The output of delay stage of the VCO is used as recovered clock in the D Flip Flop and thus helps in getting retimed data.

Another problem in conventional is it cannot detect the phase difference properly, that is when there is much difference between phase of two inputs then it requires large bandwidth and when phase difference is very less then it requires narrow bandwidth but these XOR gates are inefficient in controlling the charge pump current to provide the desired bandwidth for detecting the phase differences. And since this conventional circuit is inefficient to adapt these conditions thus PLL requires more time to get locked and thus acquisition time is also more that is 800ns after the PLL acquires lock.

3. PROPOSED PLL CIRCUIT STRUCTURE AND OPERATION PRINCIPLES

For the proposed CDR block Charge Pump and Dual-slope phase frequency detector is used in the proposed PLL using which phase detection and frequency detection and frequency detection can be done simultaneously which is not possible using XOR in PFD. In Fig. 2 where it is depicted, a Phase Frequency detector in CDR architecture has two loops fine-tuning and the coarse-tuning loop which controls PLL bandwidth. And the bandwidth which is automatically controlled by these two loops fine and coarse tunings reduces locking time while maintaining stability.

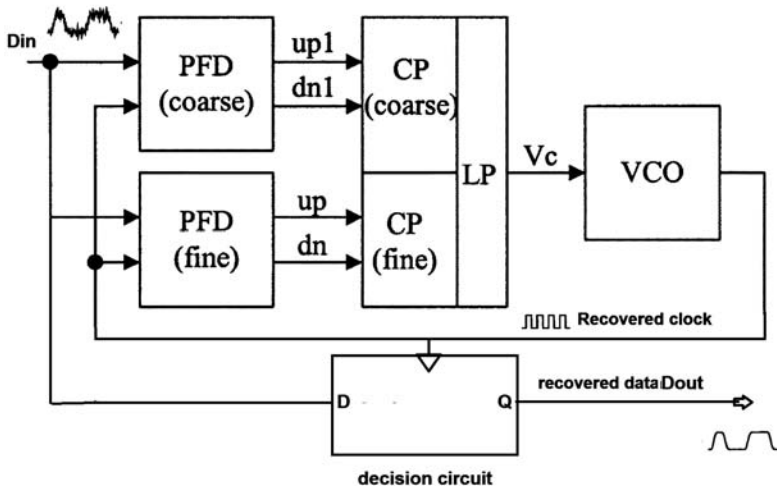

Figure 2: Proposed PLL and CDR circuit

In the out-of-lock state of the PLL that is when there is much phase difference between two inputs f_{ref} and f_{fd} shown in Fig. 3(*a*)[1] then it requires large bandwidth and thus coarse-tuning PFD is used to acquire the wide bandwidth . On the other hand, when the PLL is close to being settled that is when phase difference is very less then it requires narrow bandwidth and we use fine-tuning PFD for acquiring narrow bandwidth . The operation principles of these two loops are described below:

4. PROPOSED PHASE FREQUENCY DETECTOR

A. Coarse-Tuning Loop

In proposed coarse and fine PFD a dynamic true single phase clock (TSPC) CMOS circuit is used as shown in

Fig. 3(*a*)[1]. The locked time of the PLL would be longer without the coarse-tuning loop, due to the smaller charge/discharge current of the fine-tuning loop. Thus when the PLL is in out-of-lock state the coarse-tuning loop is activated ,using which we increase the charge or discharge current of the charge-pump.

Thus the gain of the PFD increases and we achieve a wide bandwidth which settles large phase difference at a faster rate and reduces the locking time of PLL. The coarse PFD and charge-pump compose the coarse-tuning loop as illustrated in Fig. 2 where the charge/discharge current I_c of the charge-pump is much large. The average current I_{ch} in the continuous-time approximation is given as

$$I_{ch} = (I_c/2\pi)*\phi \quad (1)$$

The phase difference between two input signals f_{ref} and f_{fd} is given by $\varnothing$ and for the loop filter I_c is the charge-pump current. The transfer function curve of the coarse-tuning loop is shown in Fig. 3(*b*)[1]. The delay width $\varnothing_d$ is the dead zone of the coarse PFD. The operation of the coarse PFD can be divided into two cases. The coarse charge-pump will give as output the corresponding current I_c controlled by the coarse PFD when the phase difference $\varnothing > \varnothing_d$. On the other hand, if phase difference $\varnothing < \varnothing_d$, then the coarse charge-pump will give no current as output.

B. Fine-Tuning Loop

When the PLL is in or near locking stage the fine-tuning loop is activated ,using which we reduce the charge or discharge current of the charge-pump. Thus the gain of the PFD gets reduced and we achieve a narrow bandwidth which settles phase difference at small dead zone. In the fine PFD a dynamic true single phase clock (TSPC) CMOS circuit is used as shown in Fig. 3(*a*)[1] to reduce the dead zone (~10 *p*/*s*) and to minimize the PLL jitter and phase error. The proposed dual-slope PFD in conjunction with a charge-pump loop-filter is shown in Fig.2. The average current I_{ch}, in the continuous-time approximation can be given as:

$$I_{ch} = (I_f / 2\pi)*\phi \quad (2)$$

where $\varnothing$ is the phase difference between two input signals

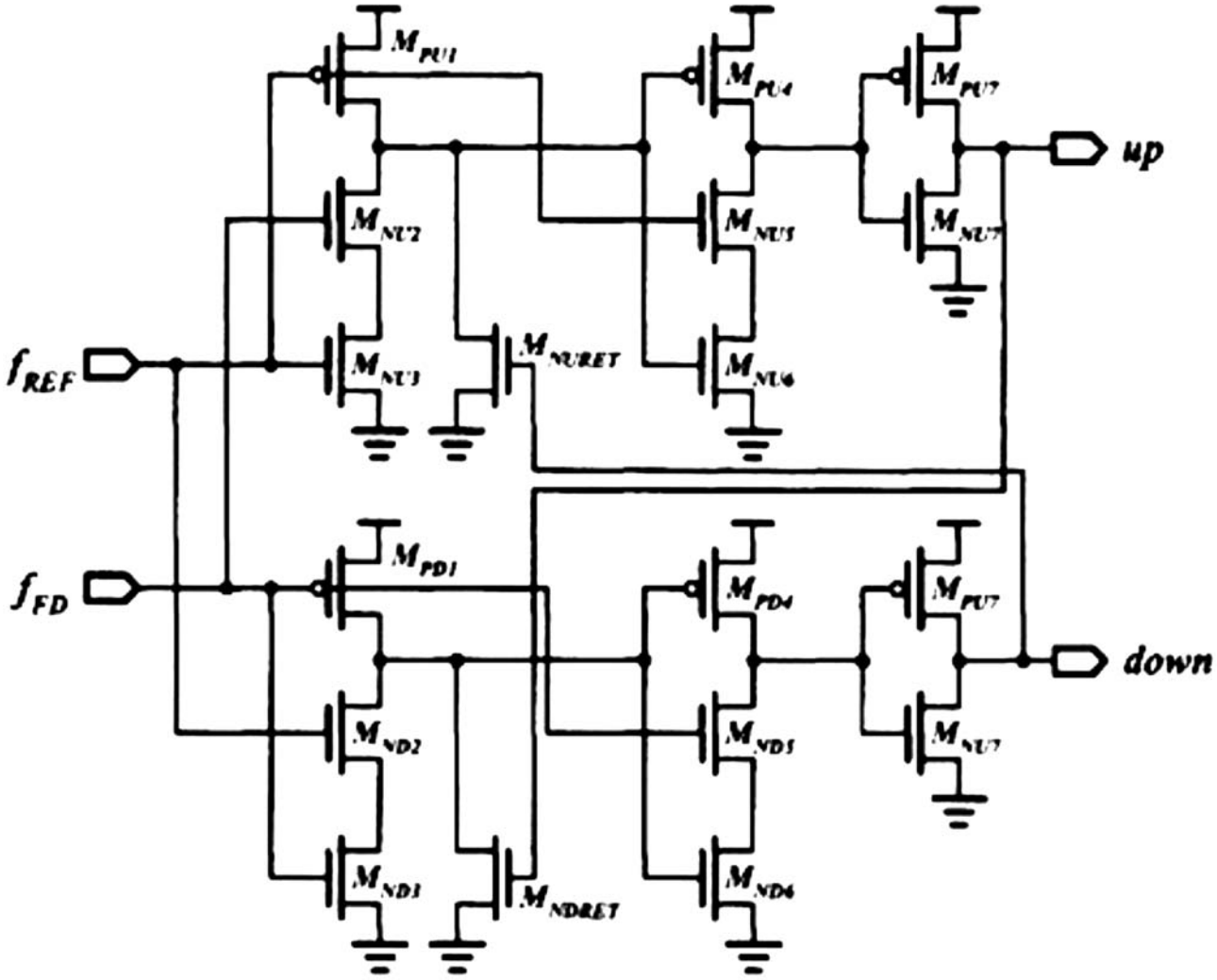

Figure 3: (*a*) Proposed course and fine PFD

f_{ref} and f_{fd}, and when the coarse-tuning loop is turned off I_f is the charge-pump current of the fine-tuning loop. The charge/discharge current I_f is a few μA. The transfer function curve is shown in Fig. 3(*c*) [1], where the vertical axis represents the average current I_{ch} in the loop filter (LP) during phase deviation. In order to provide a good flexibility in the choice of the PLL bandwidth and its damping factor in this design, a second-order low-pass filter is used .

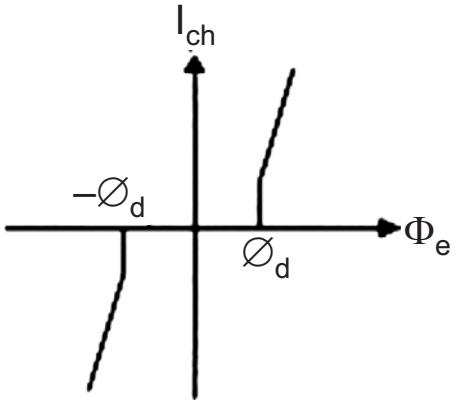

Figure 3: (*b*) Transfer function curve of coarse-tuning loop

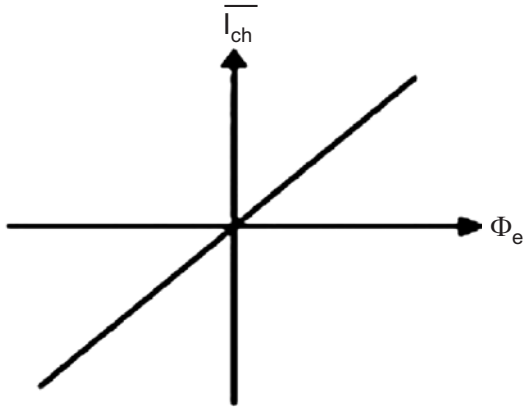

Figure 3: (*c*) Transfer function curve of fine tuning loop

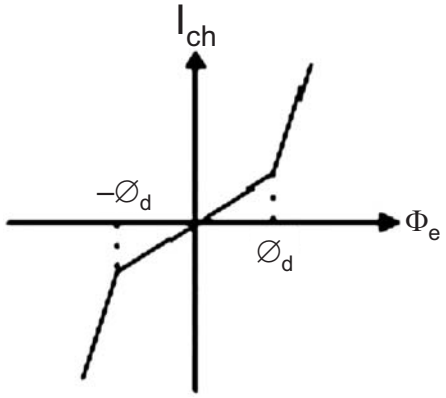

Figure 3: (*d*) Transfer function curve of two loops

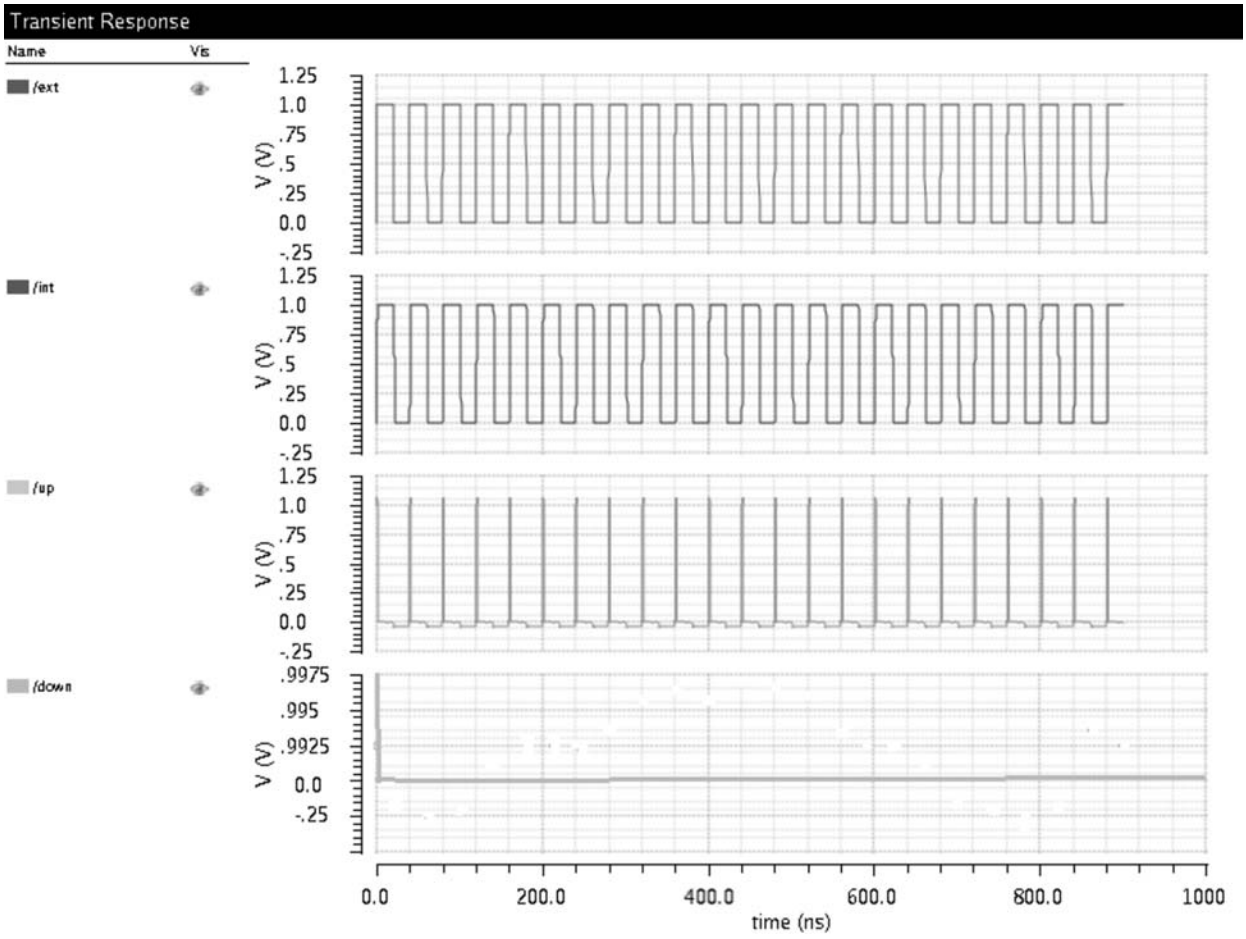

Figure 4: (*a*) PFD transient in fine tuning loop

Phase frequency Detector transient analysis is shown, where fine tuning analysis is shown in fig. 4(*a*) and that of course tuning shown in fig. 4(*b*).

It will generate "UP" or "DOWN "synchronized signals if between the two input signals there is a phase difference, "UP" signal goes high while keeping "DOWN" signal low when the reference clock rising edge leads the feedback input clock rising edge. On the other hand "DOWN" signal goes high and "UP" signal goes low if the feedback input clock rising edge leads the reference clock rising edge.

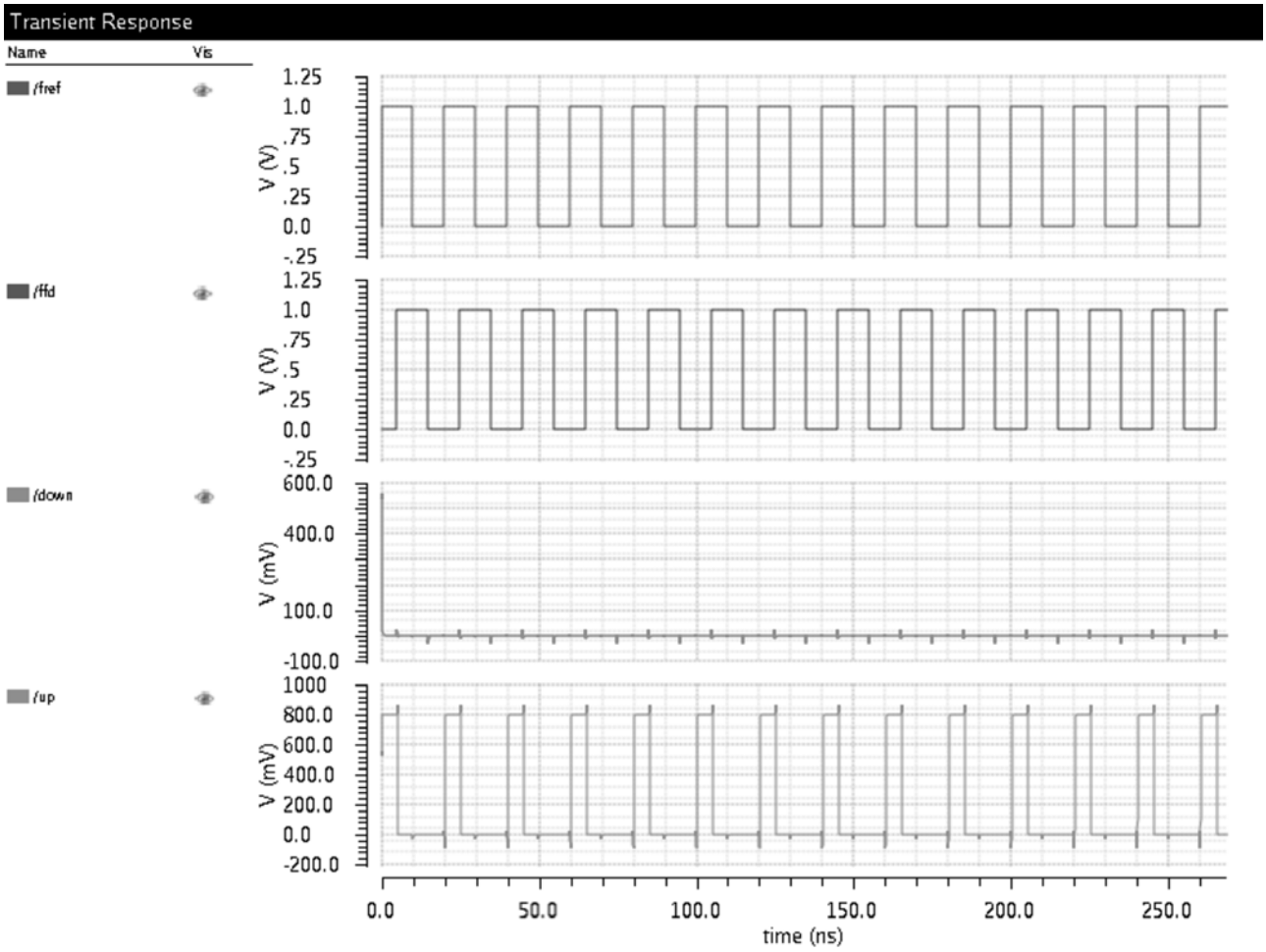

Figure 4: (*b*) PFD Transient in Course tuning loop

5. CHARGE PUMP CIRCUIT

In Charge-Pump output pulses of PD are converted to current I_{out} which controls the capacitance of low Pass Filter V_c and thus by controlling the Charge pump we can control the current and thus controlling V_c of Voltage controlled oscillator (VCO).

Here the PFD has two tuning fine tuning and course tuning which will control the charge pump output current .In course tuning Phase width are large so we get large I_{out} and this I_{out} increases the bandwidth of LPF and we get wide bandwidth . We get narrow bandwidth when Phase widths in fine tuning are small. In the whole PLL system Charge pump circuit is an important block which converts the phase or frequency difference information into a current and then into a voltage using Low Pass Filter, this voltage V_c is used to tune the VCO. Both the outputs of the PFD are combined by the Charge Pump and thus give a single output which is fed to the input of the Low Pass filter. Supply voltage variation does not affect the constant current of value I_{out} generated by Charge pump circuit. The value of "UP" and "DOWN" signal of PFD controls the change in polarity of current I_{out} keeping the amplitude of current same. The circuit diagram

of the charge pump circuit with loop filter is shown in the Fig. 5(a) [3] and transient shown in Fig 5(b). The charge pump current is converted back into the voltage by using the passive low pass loop filter. The filter should be as compact as possible. The oscillation frequency of the VCO is controlled by the output voltage of the loop filter V_c. If the PLL is in locked state it maintains a constant value. The VCO input voltage is given by:

$$V_c = K_f * I_{out} \quad (3)$$

Where K_f is the gain of the loop filter.

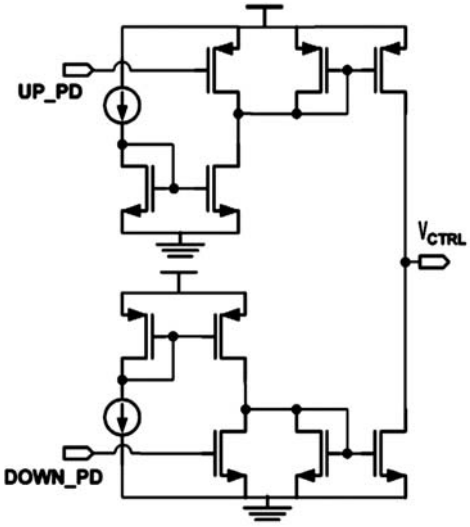

Figure 5: (*a*) Circuit diagram of Charge Pump

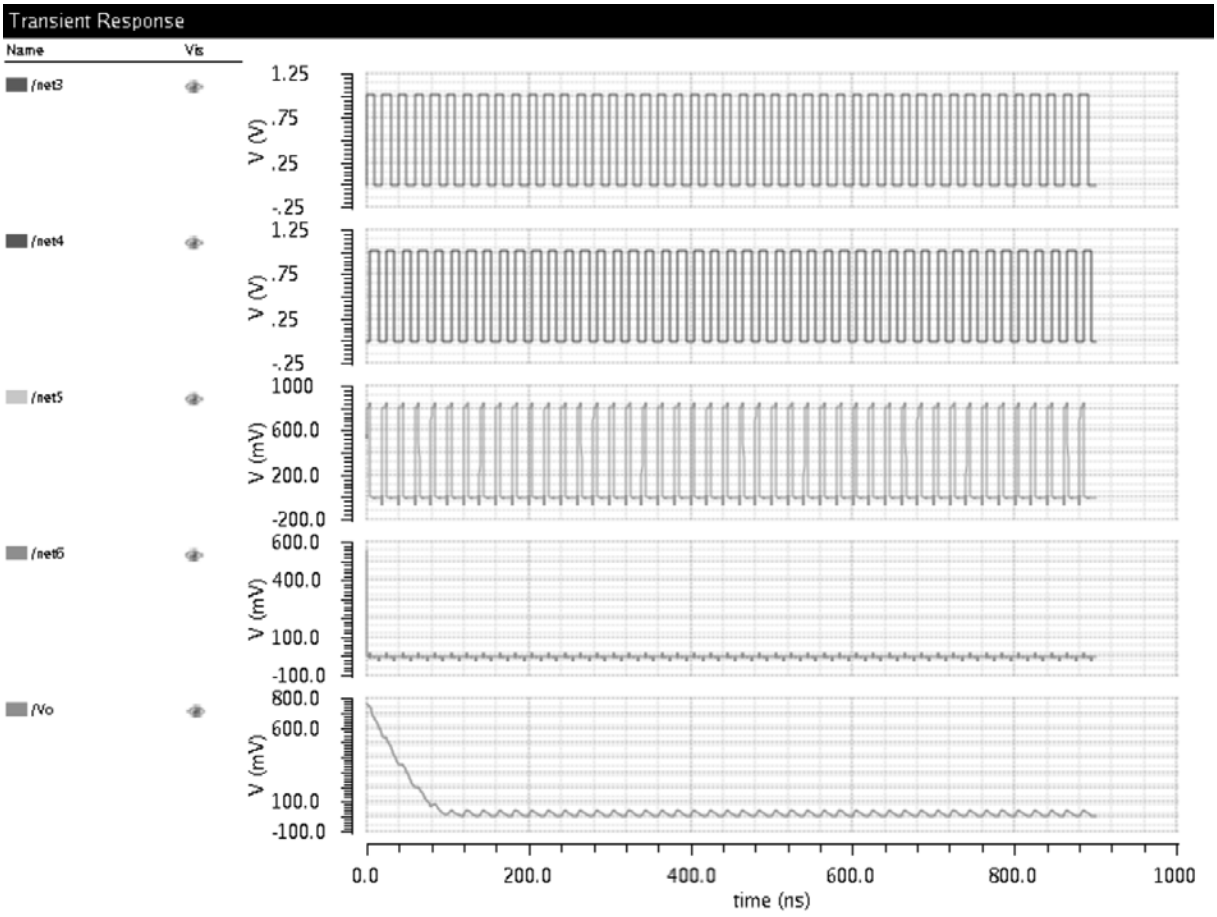

Figure 5: (*b*) Transient Analysis of Charge Pump with LPF

6. VOLTAGE CONTROLLED OSCILLATOR

The control voltage V_c generated by charge pump and Low Pass Filter controls the frequency of output signal generated from VCO. In VCO output frequency ω_{out} depends only on V_c as shown in Fig. 6(*a*). Here in the proposed VCO the number of inverter stages is fixed with 4. A single stage current starved oscillator simplified view is shown in the Fig. 6(*b*). [3] The frequency verses control voltage graph Fig.6(*c*). shows how frequency varies by varying V_C of VCO. Table 1 shows the VCO design specifications. Transient analysis of VCO is shown in Fig.6(*d*).

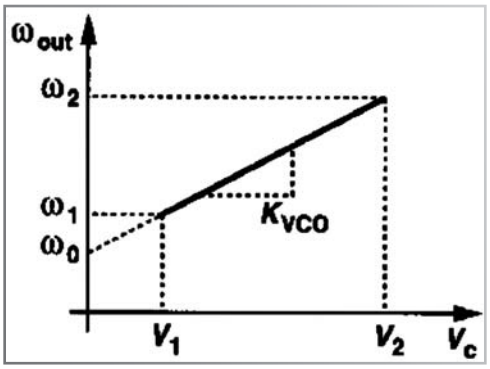

Figure 6: (*a*). ω_{out} Verses V_c graph

Output frequency w_{out} is :

$$\omega_{out} = K_{vco} * V_c + \omega_o \quad (4)$$

where K_{vco} is gain of VCO and ω_o intercept in Y axis

Table 1

VCO design specification

Parameter	*Value*
Center Frequency	1GHz
No. of stages	4
Stage delay	50ps
Supply voltage	2.5V

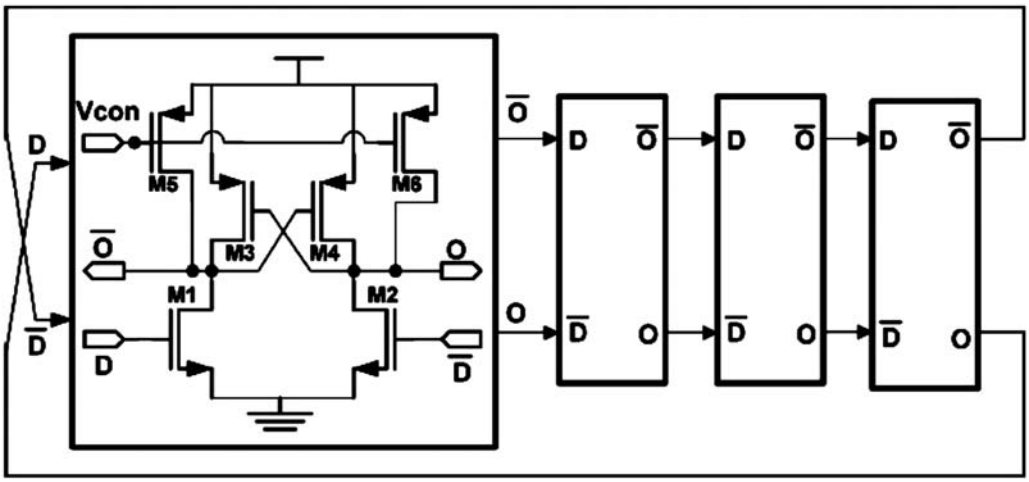

Figure 6: (*b*) VCO circuit diagram

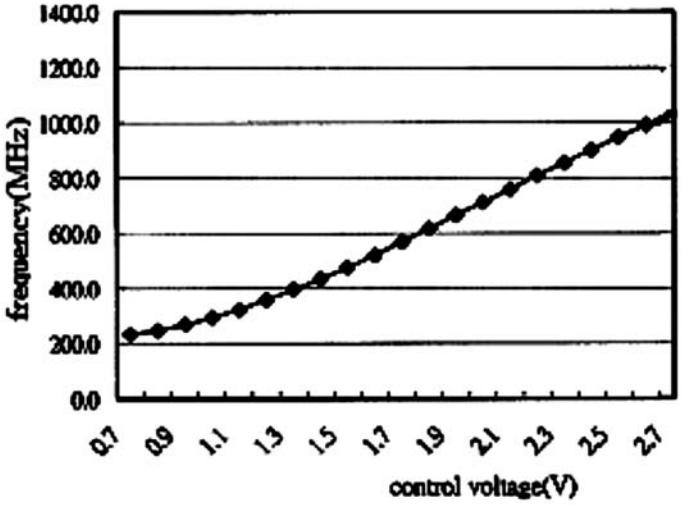

Figure 6: (*c*) Simulation result of control voltage to oscillation frequency

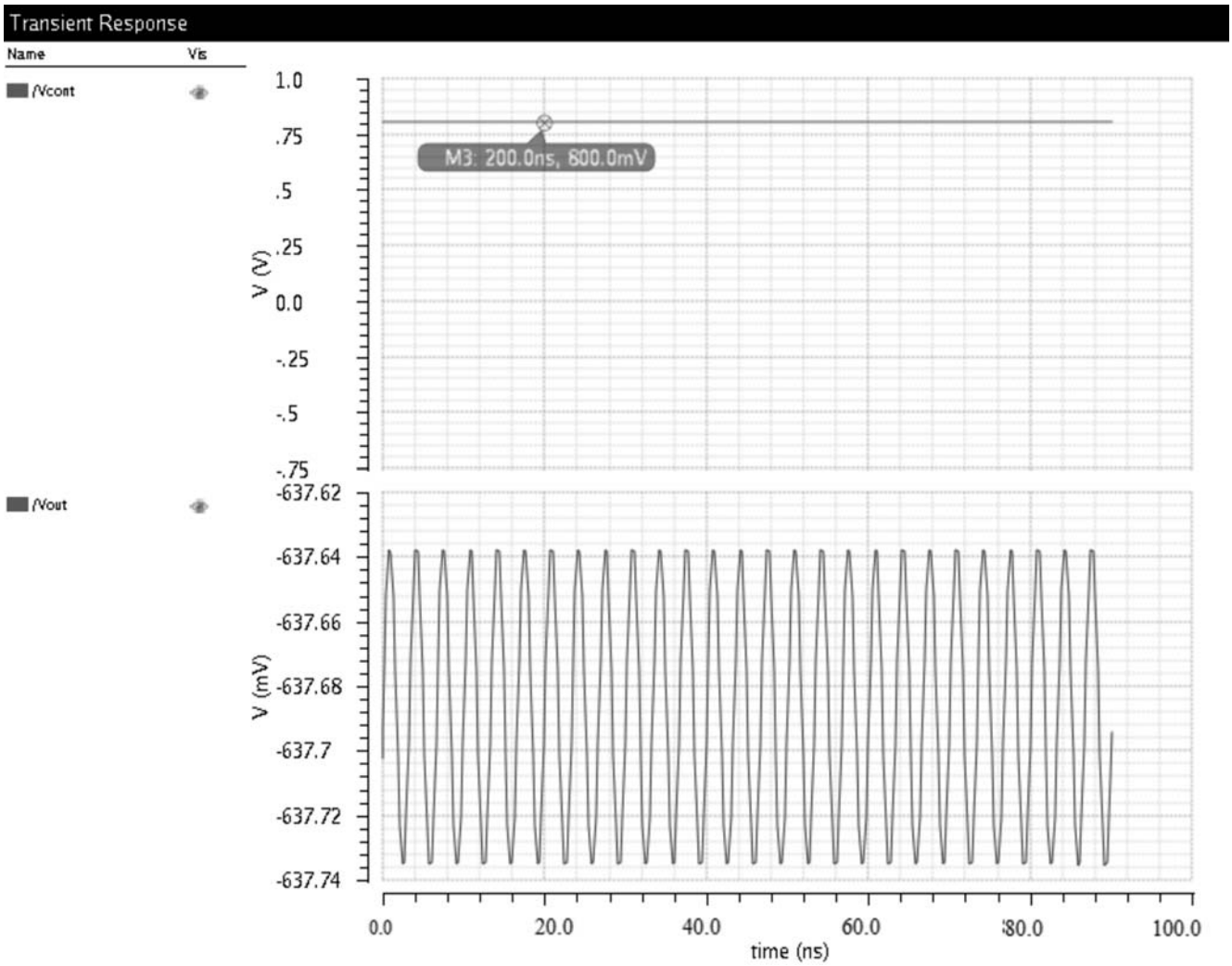

Figure 6: (*d*) Transient Analysis of VCO

7. MEASUREMENT RESULTS

The clock and data recovery circuit has been simulated in cadence environment using spectre simulator under 180nm technology.

Table 2

Proposed PLL design specification

Parameter	*Value*
Operating frequency(F_{out})	1GHz
Capture Range	800MHz–1.2GHz
Lock in range	200MHz–1.8GHz
Supply Voltage	2.5 V
Charge pump current (I_{pump})	600 μA

Table 2 shows design specification of proposed PLL. The PLL transient analysis is shown in Fig.7. In this paper PLL is operated at 1 GHz using 2.5V as supply voltage. The output waveforms of CDR were simulated and its transient analysis is shown in Fig.8. The acquisition time was measured to be 350ns after which PLL is locked at 1 GHz as shown in Fig.7. Rms jitter was greater before locking-in of PLL since there is wide bandwidth of LPF due to coarse tuning of PFD, but after that jitter reduces by 20% which is 20ps due to fine tuning of PFD as bandwidth of LPF becomes narrow. Power dissipation of proposed circuit is 240mW.

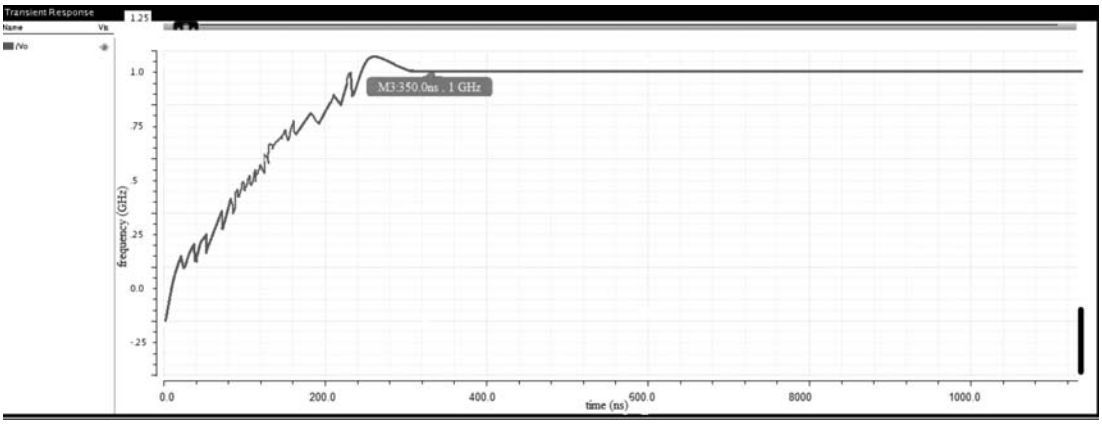

Figure 7: Transient Analysis of PLL

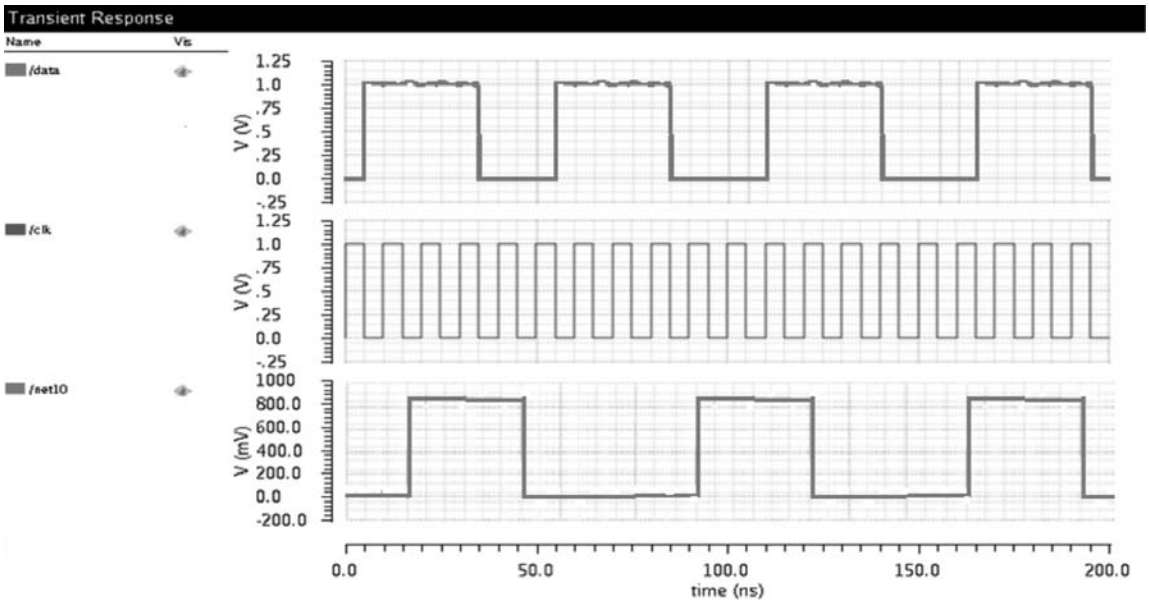

Figure 8: Recovered Data and Clock

8. CONCLUSION

In the conventional circuit acquisition time was measured to be 800 ns and jitter measured is 25ps.

CDR design is simulated in cadence environment using spectre simulator under 180nm technology. Proposed CDR block conclude that CDR using combined dual slope PFD in PLL have fast acquisition time of a few clock cycles and low jitter since the acquisition time is reduced to 350ns and jitter reduces to 20ps where PLL is operated at 1GHz using 2.5V as supply voltage. Power dissipation of proposed circuit is 240mW.

9. REFERENCES

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