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A REVIEW PAPER ON HIGH PERFORMANCE 1- BIT FULL ADDERS DESIGN AT 90NM TECHNOLOGY

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Abstract: This paper provides a comparative analysis of various full adders in terms of power, delay and PDP. From the survey of literature, conventional 28T full adder, SERF 10T full adder, domino 22T, 8T full adder are implemented in GPDK 90nm technology on cadence virtuoso tool using spectre simulator. Full adder is the basic unit for many complex athematic operations like multiplication, division and exponentiation and it is used as basic building block in multipliers, comparator and parity checker. Power and delay are two important design constraints but there is always a trade-off between them, so power delay product (PDP) is the better constrain to evaluate the circuit performance. The variation of W/L ratios of the MOS transistors can causes the incremental change in average power and it also overcome the threshold loss problems. The average power, delay, PDP are calculated at supply voltages with range of 1.1v to 1.6v. Based on the Simulation results, domino 22T full adder having better delay and PDP values. This design is having good performance over all three designs.

Keywords: XOR gate, Domino logic, Threshold loss, Power delay product, Energy Recovery.

1. INTRODUCTION

With the rapid growth in the VLSI (Very Large Scale Integration) semiconductor Technology, There is a need of high speed devices with less power consumption and capable of computing multiple operations at a time. So ultimately it can leads to an increase the number of transistor in an integrated circuit. Power and speed are the two most important design parameter objectives in integrated circuit. While designing a circuit, Designer should be aware of design constraints like power, delay and area. There is always a trade-off between power and delay. Getting the optimised value of both power and delay. Of the circuit is the challenging task for designer.

The basic operation of adder is the addition of binary numbers and it is the basic unit for many complex arthematic operations like multiplication, division and exponentiation and it is used as basic block in multipliers, comparator and parity checker. The full adder is realised by using XOR, AND logic gates. XOR gate is heart of the full adder circuit. Designing of XOR gate with minimal number of transistor influences the performance of the full adder circuit. The truth table of XOR gate is given below.

Table 1
XOR gate truth table

A (input)	*B (input)*	*Y (output)*
0	0	0
0	1	1
1	0	1
1	1	0

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This paper is organized section wise in the following way, section II describes the theoretical background on full adder. Section III gives the simulation results of conventional 28T full adder, 8T full adder, and self-energy recovery logic 10T, domino 22T full adder. Section IV compares the obtained results in terms of power, delay and PDP. Finally, the last section covers conclusion and references.

2. THEORITICAL BACKGROUND OF FULL ADDER

Binary addition is the basic operation found in most arthematic components like multipliers, parity checker and comparator. Basically full adder consists of three inputs and two outputs (.i.e. sum and carry). The truth table of full adder is given below.

Sum = A B C

Carry = (A.B) + C (A B)

Table 2
Truth Table of Full Adder

A	*B*	*C*	*Sum*	*Carry*
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

In VLSI hierarchical design modelling, there are two types of design methodologies, one is Top–Down and other one is bottom – up methodology. In Bottom - up design methodology, designed sub module blocks using leaf cells .i.e. logic gates, which cannot be reduced further and these sub module blocks are treated as a basic blocks for higher level blocks. Here leaf cell and sub module block are XOR gate, adder circuit respectively. The higher level blocks are multipliers, comparators, etc.

There are several works done in order to decrease the transistor count and subsequently it can leads to decrease the area and power of the design. Basically, full adders are divided into two kinds depending upon the output voltage swing. 1. Full swing and 2. Non full swing. Non full swing full adders had a threshold loss problem and it is having low speed and low noise immunity when they are connected in cascaded manner. To meet the required design constraints, we are going for scaling the transistor sizes and reduction in the supply voltages, ultimately it causes a severe threshold loss problems.

Typically, full adder can be implemented in two logic styles. One is static other one is dynamic. Static logic full adders are reliable and simpler. Generally, it consumes less power than the dynamic full adders. Dynamic full adders are faster than the static one. It requires an additional controlling signal i.e. clock signal, which limits the speed of the operation of the design.

3. SIMULATION RESULTS OF PREVIOUS LITERATURE

In this section, we implemented different types of full adder designs .i.e. conventional 28T full adder, self-energy recovery logic 10T, domino 22T full adder, 8T full adder using MOS transistors in 90nm technology using cadence virtuoso on spectre simulator.

(a) ***Conventional 28T Full Adder:*** This full adder design [4] is realized by 28 MOS transistors using both pull up network and pull down network. It is basic static full adder. It is implemented on 90nm technology with power supply 1.1v as shown in below figure 1. The 28T adder consists A, B and C as inputs and sum, carry as outputs. The output transient responses along with power waveform of conventional 28T adder is shown in figure 2.

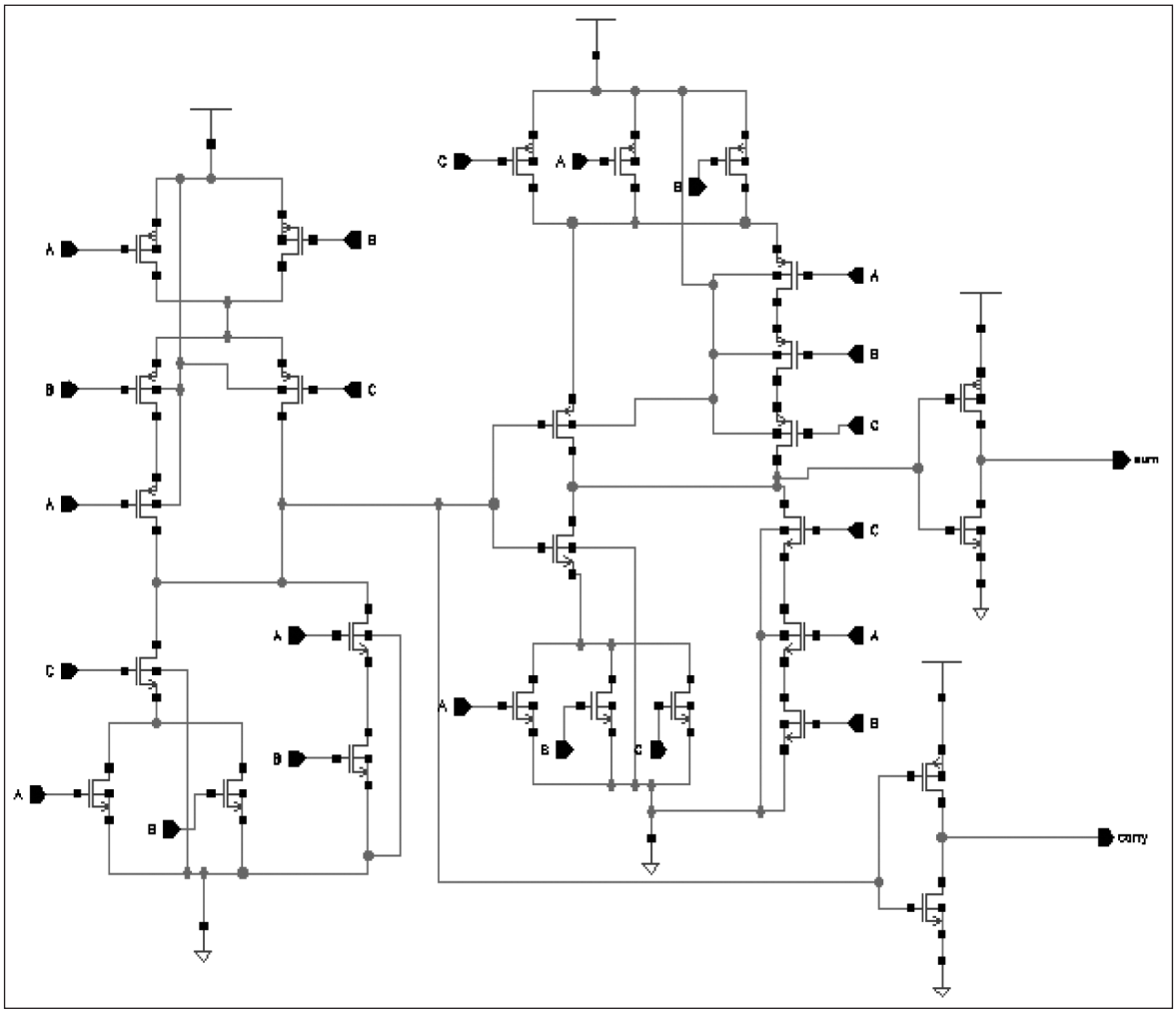

Figure 1. Schematic of conventional 28T full adder

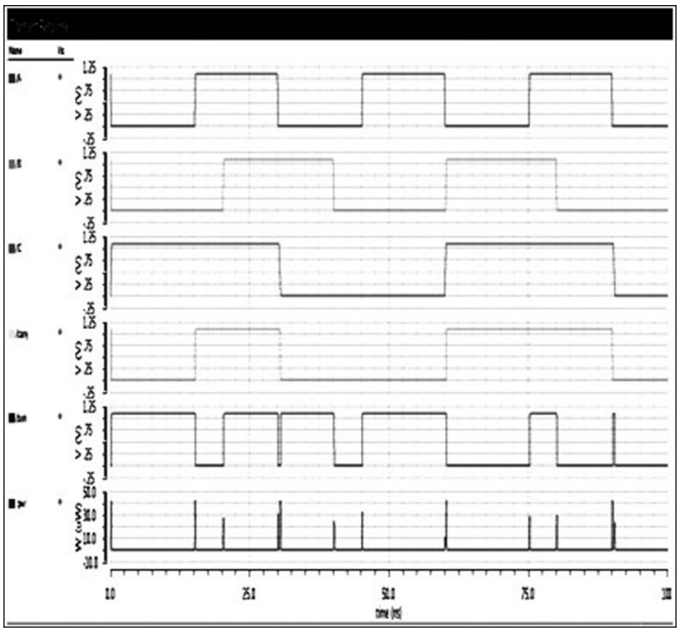

Figure 2. Output and power waveforms of conventional 28T adder

(b) ***10T Self Energy Recovery Full adder (SERF):*** This full adder [2] reuses the energy and consumes less power. It requires only 10 transistors to implement 1 bit full adder. The literature review reveals that the XOR and XNOR gates are realized by different techniques over the past decades. In this circuit, sum output is obtained by two XNOR gates and carry output is taken from the pass transistor. Each XNOR gate having the 4 MOS transistors. This design is capable of operating at higher voltages but it having the problem of driving the intermediate node transistors is difficult when it operates at lower voltages. The implementation of full adder and transient output responses are shown in below figure.3 and figure.4 respectively.

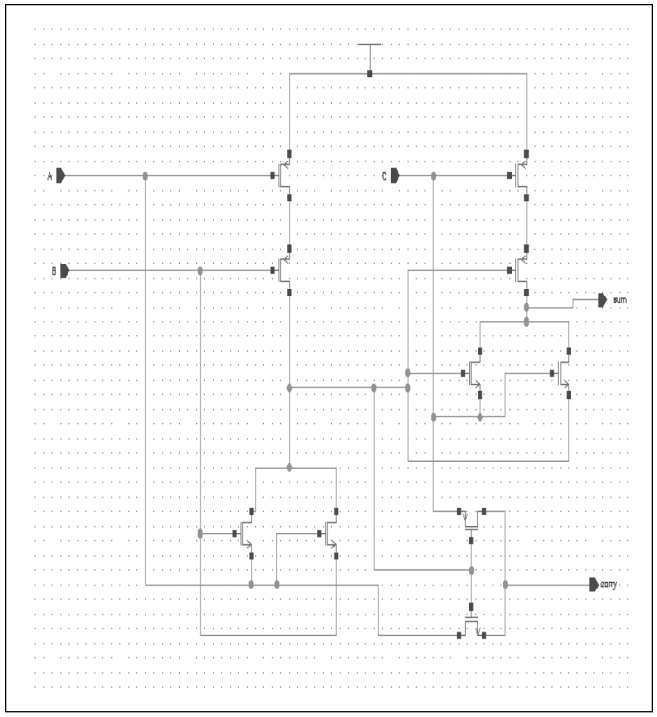

Figure.3. Schematic of SERF 10T full adder

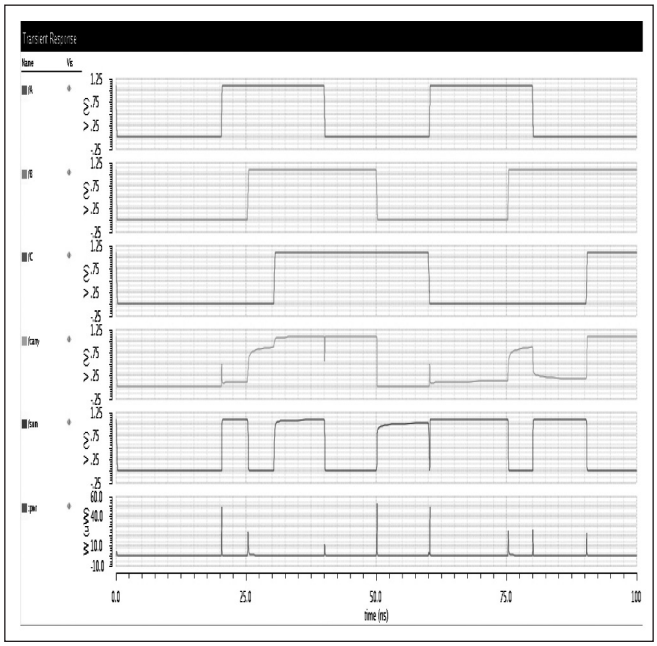

Figure 4. Transient output waveforms of SERF 10T adder

(c) ***Domino 22T full adder:*** This full adder [4] is designed with domino logic and consists of 22 MOS transistors. Domino logic is one type of dynamic Technique. This logic requires an additional controlling signal .i.e. clock signal. It has two phase's i.e. one is pre charge phase and the other one is evaluation phase. During the pre-charge phase, the output capacitance is loaded with supply voltage and in the evaluation phase evaluating the given inputs. This below figure shows the implementation of 22T full adder design. This design reduces the leakage currents because it is not having the direct path between VDD and GND. It can process only low (logic 0) to high (logic 1) transition due to termination of path between VDD to dynamic node when the clock is in the evaluation phase. The threshold loss problems overcome by adding feedback weak PMOS transistor. The output response and power signal is shown in below figure.

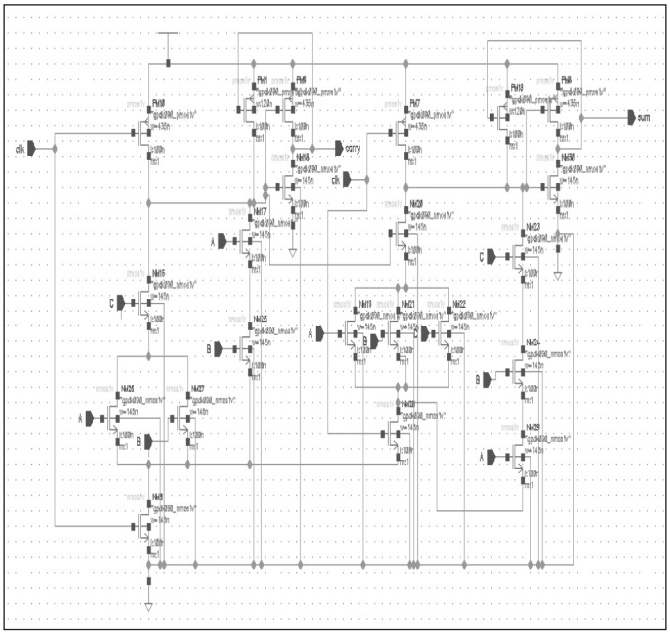

Figure 5. Schematic of domino 22T full adder

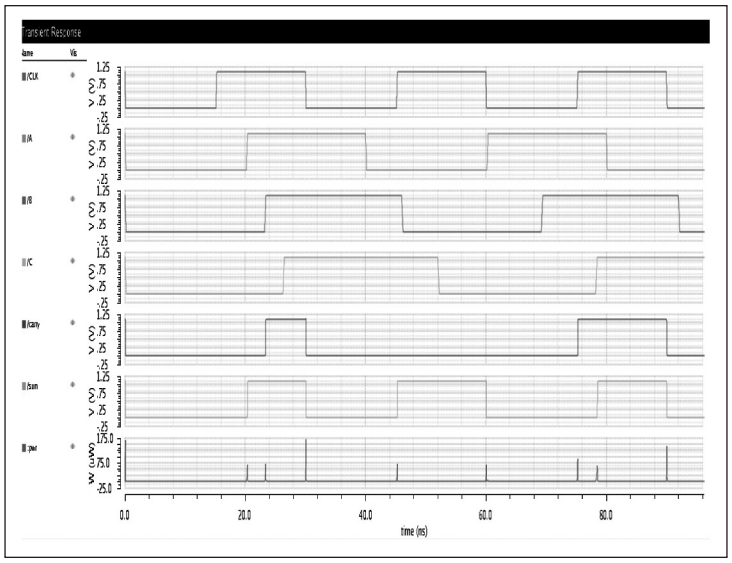

Figure 6. Transient output waveforms of domino 22T adder

(d) ***8T Full adder:*** In the literature survey, This 1-bit full adder design [1] has least transistor count among all different type of adders. The advantage of the design is area of the full adder cell is compacted to a greater extent caused by having less number of transistors. Here, an additional fixed negative supply voltage is given to drive the two PMOS transistors into a slightly turned on. By doing so, it improves the output responses of an adder. By selecting the proper size of W/L ratios of selective transistors to reduce the threshold loss and improved the driving capabilities. Due to increase the W/L ratio of transistors, substantially it leads to an increase in the power consumption of a cell. The schematic of 8T full adder and it's transient output responses are shown in below figure 7 and figure 8 respectively.

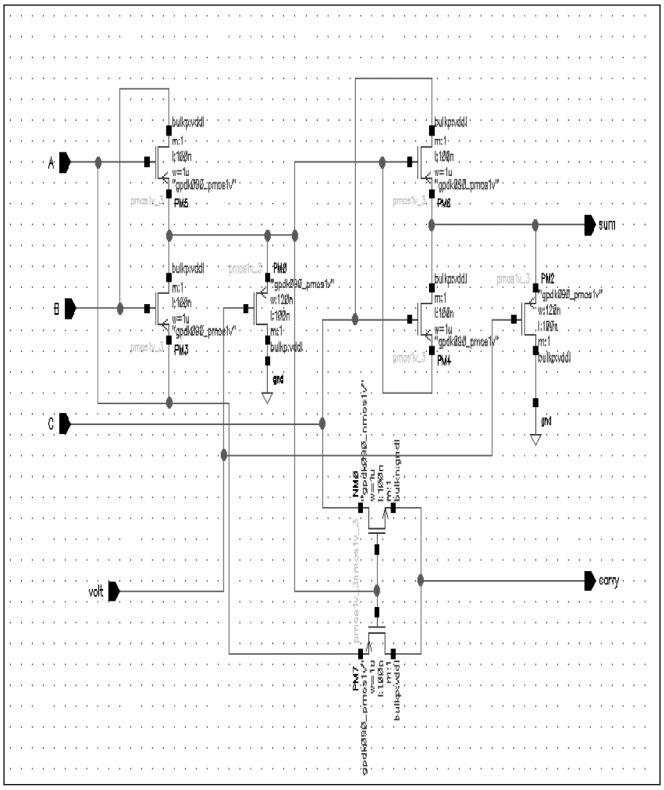

Figure 7. Schematic of 8T full adder

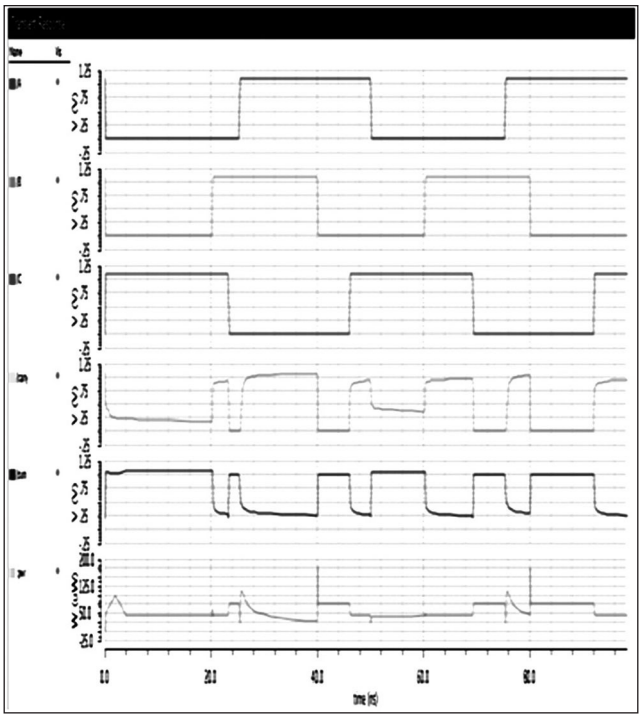

Figure 8. Transient output waveforms of 8T adder

4. COMPARISION OF SIMULATION RESULTS

The above four types of full adders are implemented in 90nm technology on spectre simulator using cadence virtuoso at various supply voltages with a range of 1.1v to 1.8v. Power consumption and delay are the two required design constraints for any CMOS circuits. The average power is calculated from the obtained transient output response. Propagation delay of circuit is calculated based on the critical path. It is a measure of speed performance of design. PDP is also known as power delay product and it is the product of both power and propagation delay. PDP is also one of the important design parameter while designing an circuit. It gives better performance of circuit. The power, delay and PDP of the above four types of full adders are observed at various supply voltages and it is given in the below table 3.

Table 3
Average power consumption of adder cells

		Average Power (μW)			
S.No	*Supply (v)*	*28T*	*10T*	*22T*	*8T*
1	1.1	0.476	0.342	0.668	59.40
2	1.2	0.745	0.477	0.846	77.25
3	1.3	0.971	0.659	1.066	97.50
4	1.4	1.07	0.899	1.327	120.2
5	1.5	1.37	1.218	1.644	145.2
6	1.6	1.75	1.635	2.029	172.8

Table 4
Propagation delay of adder cells

Propagation Delay (ns)					
S.No	*Supply (v)*	*28T*	*10T*	*22T*	*8T*
1	1.1	15.23	0.07224	0.03256	20.38
2	1.2	15.22	0.06576	0.02297	20.39
3	1.3	15.20	0.06547	0.01501	20.39
4	1.4	15.20	0.06726	0.00838	20.40
5	1.5	15.19	0.06935	0.00273	20.40
6	1.6	15.18	0.07143	0.00219	20.40

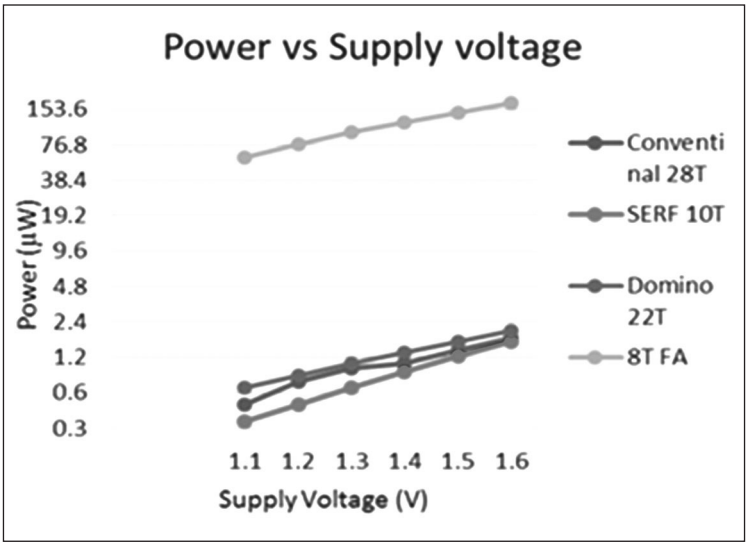

Figure 9. Average power comparison of full adder cezlls

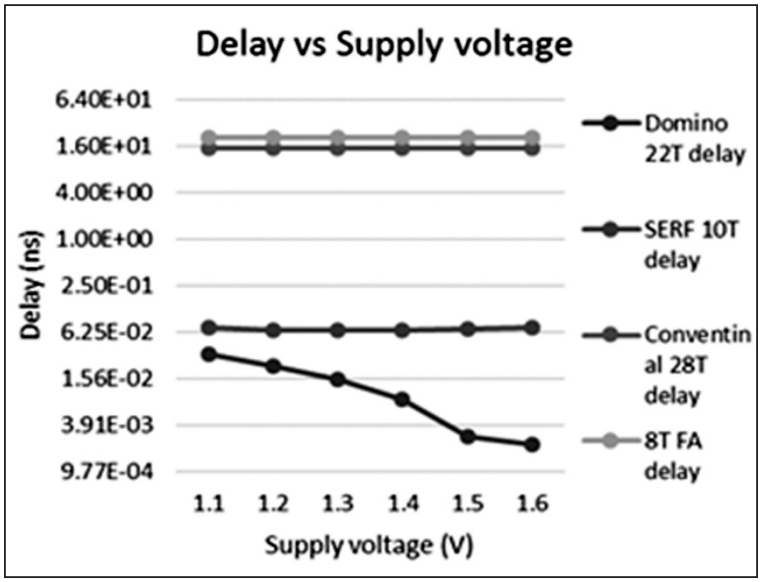

Figure 10. Propagation delay comparison of full adder cells

From the power and delay analysis, 8T full adder having higher power and propagation delay than the others. So here the comparison of PDP is made among the three full adder cells .i.e. conventional 28T full adder, self-energy recovery logic 10T, domino 22T full adder and it is shown in below figure.

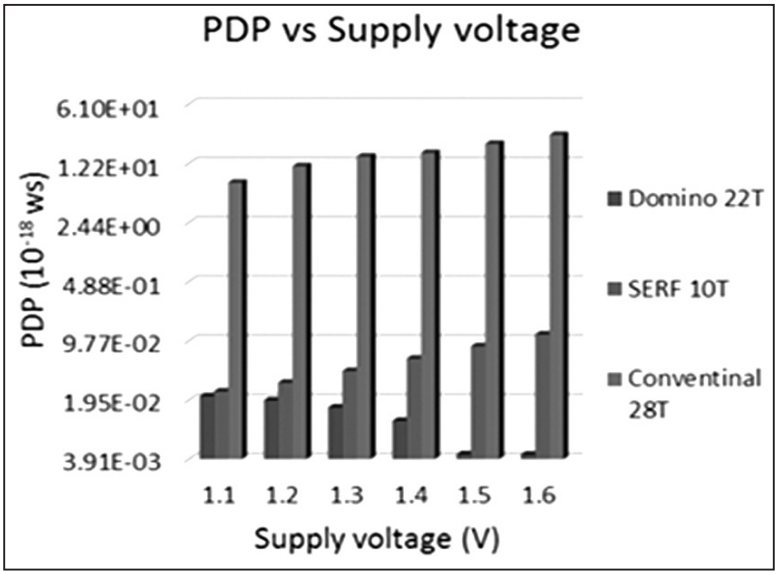

Figure 11. PDP comparison of full adder cells

5. CONCLUSION

In this paper we implemented and compared the simulation results of four different logic full adders. These Full adder designs are implemented in 90nm technology on spectre simulator using cadence virtuoso. According to the simulation results, domino 22T full adder having better delay and PDP values than the others. This adder operates at frequency 33 MHz in CMOS 90nm technology. It is observed that effect of variations of the transistor sizes causes the increment of average power and it also overcome the threshold loss problems. SERF 10T full adder consumed less power than the conventional full adder. The power consumption and delay are depends upon the operating frequency. From the delay analysis, the delay of the domino 22T full adder gradually decreases with increase of supply voltage. Based on the Simulation results Domino 22T is preferred adder circuit for arthematic operations.

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