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A Comparative Performance Analysis of I_d-I_q and Artificial Neural Network based Control Strategies for Current Harmonic Mitigation in three Phase Four Wire System

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ABSTRACT

Shunt active power filter (SAPF) have been used to compensate current harmonics generated by nonlinear loads. The key issue is control schemes for SAPF. The present work proposes a PI-Artificial Neural Network (PI-ANN) based control strategy for extracting the three phase reference currents. The performance of the proposed controller is compared current (I_d–I_q) control strategies under different source voltage conditions in MATLAB/Simulink environment and also implemented using Real-Time Digital Simulator Hardware (RTDS). When the supply voltages are balanced and sinusoidal, then all control strategies converge to the same compensation characteristics. However, when the supply voltages are distorted and/or unbalanced sinusoidal, these control strategies result in different degrees of compensation. The p–q control strategy unable to yield an adequate solution when source voltages are not ideal. Extensive simulations are carried out with PI-Neural Network controller by considering different voltage conditions and adequate results were presented. The performance of the proposed controller outperform that of the I_d–I_q method under balanced, un-balanced and non-sinusoidal supply conditions. The detailed simulation and RTDS Hardware results are included.

Key Word: Shunt Active Power Filter (SAPF), harmonic Compensation, Neural Network (NN), RTDS, I_d–I_q control strategy

1. INTRODUCTION

Over the past few years Electrical power quality [1] has beenan important and growing problem because of the proliferation of nonlinear loads such as power electronic converters in typical power distribution systems. Particularly, voltage harmonics and power distribution equipment problems result from current harmonics produced by nonlinear loads. Harmonics surfaced as a buzz word from 1980s which always threaten the normal operation of power system and user equipment. Highly automatic electric equipment, in particular, cause enormous economic loss every year. Because of the huge amount of harmonics injected into the line by nonlinear loads, there is harmonic voltage drop and the source voltage becomes non-sinusoidal. The deviation is in the form of an episodic function, and by definition, the voltage distortion contains harmonics [2].

It is noted that non-sinusoidal current results in many problems for the utility power supply company, such as: low power factor, low energy efficiency, electromagnetic interference (EMI), distortion of line voltage, etc. It is well known that when neutral wire is overheated then excessive harmonic current will pass through the neutral line, which is three times that of zero sequence current. Thus a perfect compensator

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is necessary to avoid the consequences due to harmonics. Though several control techniques and strategies [3] have been developed but still performance of filters are not satisfactory, there is scope to develop new controller to handle severe nonlinearity in the system, these became the primarily motivation for the current paper.

Instantaneous active and reactive theory (p–q theory) was introduced by Akagi, Kawakawa, and Nabae in 1984 [4]. Since then, many scientists [5–8] and engineers made significant contributions to its modifications in three-phase four-wire circuits and its applications to power electronic equipment. The p–q theory [6] based on a set of instantaneous powers defined in the time domain. No restrictions are imposed on the voltage and current waveforms, and it can be applied to three phase systems with or without neutral wire for three phase generic voltage and current waveforms. Thus it is valid not only in the steady state but also in the transient state. p–q theory needs additional PLL circuit for synchronization, so p–q method is frequency variant.

In i_d–i_q method [7] angle 'θ' is calculated directly from main voltages and thus enables the method to be frequency independent. Thus large numbers of synchronization problems with un-balanced and non-sinusoidal voltages are also avoided.

Recently, ANNs have attracted much attention in different applications, including SAPF due to its parallel computing nature and high learning capability. Different ANN structures have been reported for the fundamental or harmonic load current extraction for APF control, such as adaptive neuro-fuzzy interference system (ANFIS) [15], Adaptive Linear Neuron (ADALINE) [16]–[21], the feed-forward multilayer neural network (MNN) [21]–[24], the radial-basis-function neural network (RBFNN) [25], [26], and the recurrent neural network (RNN) [27]–[28]. Among these methods, feed-forward MNN and ADALINE are the most widely used ANN structures [16]–[24].

In this paper, a PI-Artificial Neural Network (PI-ANN) based controller is implemented and results are compared with PI- (I_d–I_q) reference current extraction techniques under balanced, un-balanced, balanced and non-sinusoidal supply conditions. Since it is already reported that the performance of PI- (I_d–I_q) is far better than PI-(p-q) techniques [9], we have chosen PI- (I_d–I_q) control strategy to be compared with PI-Neural Network based controller. The simulation results are validated with using Real-Time Digital Simulator Hardware [10] (RTDS).

2. SHUNT ACTIVE POWER FILTER CONFIGURATION

Fig. 1 shows a three leg structure with the neutral conductor being connected to midpoint of dc-link capacitor. The configuration of the shunt active power (SAPF) filter and the control blocks are also shown in Fig.1.

The active power filter (APF) is controlled to generate the compensating current [11-12] to compensate the current harmonics on AC side and reactive power flow to the source, thereby making the source current almost harmonic free and in phase with source voltage.

3. INSTANTANEOUS ACTIVE AND REACTIVE CURRENT COMPONENT (i_d – i) METHOD

Initially, the mains voltages (v_{sa}, v_{sb}, v_s and load currents (i_{La}, i_{Lb}, i_l in a – b – coordinates are transformed into a stationary reference frame of α – β coordinates.

$$\begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \tag{1}$$

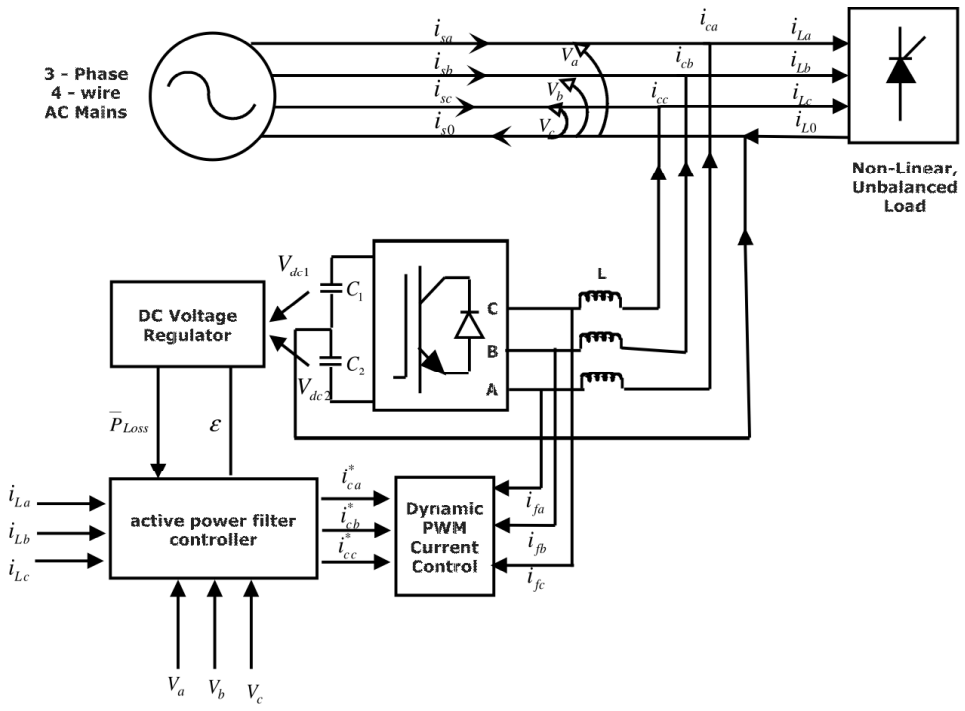

Figure 1: Shunt active power filter configuration in a three phase four wire system

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \\ i_{L0} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{2}$$

The load current is decoupled into its respective active and reactive components in $d - q$ reference frame using Park's transformation.

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} \tag{3}$$

Angle θ is obtained from instantaneous voltage vectors as follows,

$$\theta = \omega t = \tan^{-1}\left(\frac{v_{s\beta}}{v_{s\alpha}}\right) \tag{4}$$

Here ω represents the speed of synchronously rotating $d - q$ frame. The voltage vector angle θ is a constantly increasing function of time under ideal mains condition, whereas this is not the case under non-ideal supply, as it is sensitive to the presence of harmonics and/or unbalance in supply voltage. The voltage and current space vectors in stationary (α – β) and synchronous (d–q) reference frames are illustrated in the Fig. 2.

The d-axis component of mains voltage is given by,

$$v_{sd} = |\bar{v}_{sdq}| = |\bar{v}_{s\alpha\beta}| = \sqrt{(v_{s\alpha})^2 + (v_{s\beta})^2} \tag{5}$$

The q-axis component is always null i.e. $v_{sq} = 0$.

Hence, instantaneous $d - q$ axes currents can be calculated as,

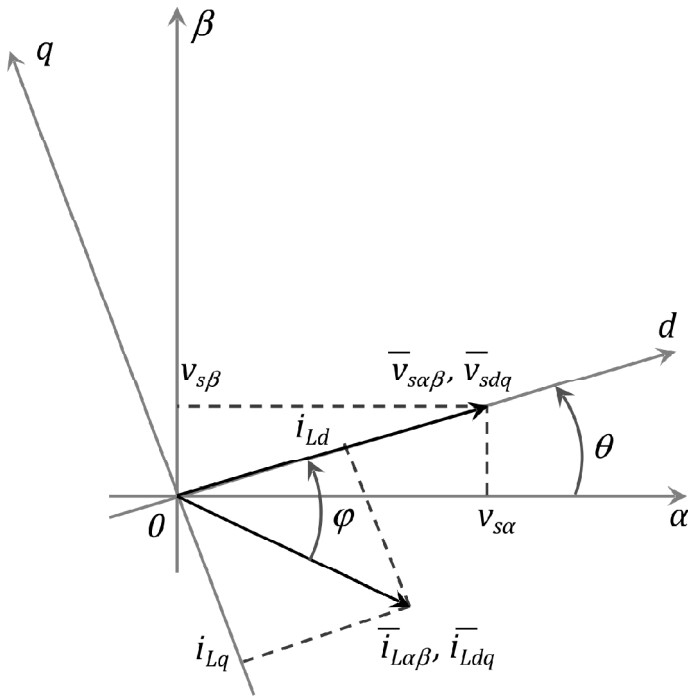

Figure 2: Voltage and current space vectors in the stationary (α–β) and synchronous (*d*–*q*) reference frames

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \frac{1}{\sqrt{(v_{s\alpha})^2 + (v_{s\beta})^2}} \begin{bmatrix} v_{s\alpha} & v_{s\beta} \\ -v_{s\beta} & v_{s\alpha} \end{bmatrix} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} \tag{6}$$

Both i_{Ld} and i_{Lq} consist of an average/DC component and an oscillating/AC component as indicated in (7).

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \begin{bmatrix} i_{Ld1h} + i_{Ldnh} \\ i_{Lq1h} + i_{Lqnh} \end{bmatrix} \tag{7}$$

Where, i_{Ld1h} and i_{Lq1h} indicate the fundamental frequency components of i_{Ld} and i_{Lq}.

The oscillating components of i_{Ld} and i_{Lq} i.e., i_{Ldnh} and i_{Lqnh} are filtered out using 2nd order Butterworth type low-pass filters with cut-off frequency of 25 Hz each.

The total active current required to maintain a constant DC-link capacitor voltage and to compensate the power losses occurring inside the APF is represented by i_{d1h}. This is the output signal of PI controller used to minimize the DC-link voltage error ΔV_{dc}, as defined in (8).

$$i_{d1h} = K_p \Delta V_{dc} + K_i \int \Delta V_{dc} \cdot dt \tag{8}$$

According to $i_d - i_q$ control strategy, only the average value of *d*-axis component of load current should be drawn from the supply. Hence, the currents i_{Ldnh} and i_{Lqnh} along with i_{d1h} are utilized to generate reference filter currents i_{cd}^* and i_{cq}^* in $d - q$ coordinates.

$$i_{cd}^* = -i_{Ldnh} + i_{d1h} \tag{9}$$

$$i_{cq}^* = -i_{Lqnh} \tag{10}$$

This is followed by inverse Park's transformation giving away the compensation currents i_{ca}^*, i_{cb}^*, i_{cc}^* and in the four wires as described in (11) and (12).

$$\begin{bmatrix} i_{ca}^{*} \\ i_{cb}^{*} \\ i_{cc}^{*} \end{bmatrix} = \begin{bmatrix} \sin\omega t & \cos\omega t & 1 \\ \sin\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t - \frac{2\pi}{3}\right) & 1 \\ \sin\left(\omega t + \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \begin{bmatrix} i_{cd}^{*} \\ i_{cq}^{*} \\ i_{c0}^{*} \end{bmatrix} \tag{11}$$

$$i_{cn}^{*} = i_{ca}^{*} + i_{cb}^{*} + i_{cc}^{*} \tag{12}$$

The zero-sequence reference compensation current i_{c0}^{*} in (11) can be obtained by using the expression, $i_{c0}^{*} = -i_0$. In Fig. 3, the block diagram for reference current generation employing $i_d - i_q$ control scheme has been illustrated.

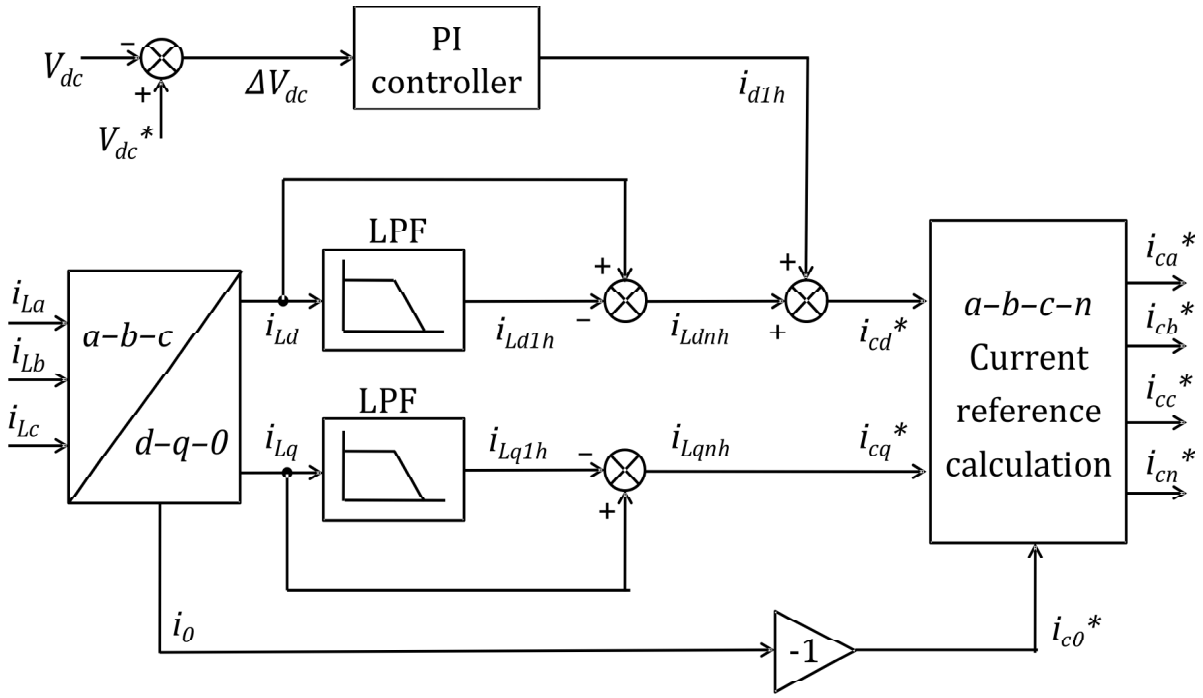

Figure 3: Reference current extraction diagram for i_d–i_q schemewith PI controller

In order to maintain DC link voltage constant, a PI branch is added to the d axis in d–q frame to control the active current component. The PI controls this small amount of active current and then the current controller regulates this current to maintain the DC link capacitor voltage [8].

The reference signals thus obtained are compared with the actual compensating filter currents in a hysteresis comparator, where the actual current is forced to follow the reference and provides instantaneous compensation by the APF [13] on account of its easy implementation and quick prevail over fast current transitions. This consequently provides switching signals to trigger the IGBTs inside the inverter. Ultimately, the filter provides necessary compensation for harmonics in the source current and reactive power unbalance in the system.

One of the major advantages of this method is that angle è is calculated directly from main voltages and thus makes this method frequency independent by avoiding the PLL in the control circuit. Consequently synchronising problems with unbalanced and distorted input voltage situations are evaded. Thus i_d–i_q scheme achieves large frequency operating limit [14].

4. DC LINK VOLTAGE REGULATION WITH PI CONTROLLER

For regulating and maintaining the DC link capacitor voltage [12], the active power flowing into the active filter needs to be controlled. If the active power flowing into the filter can be controlled equal to the losses

inside the filter, the DC link voltage can be maintained at the desired value. The quality and performance of the SAF depend mainly on the method implemented to generate the compensating reference currents. In order to maintain DC link voltage constant and to generate the compensating reference currents we have implement PI controller.

Fig. 4 shows the internal structure of the control circuit. The control scheme consists of PI controller, limiter, and three phase sine wave generator for reference current generation and generation of switching signals [8]. The peak value of reference currentsis estimated by regulating the DC link voltage. The actual capacitor voltage is compared with a set reference value.

The error signal is then processed through a PI controller, which contributes to zero steady error in tracking the reference current signal. The output of the PI controller is considered as peak value of the supply current (I_{max}), which is composed of two components: (a) fundamental active power component of load current, and (b) loss component of APF; to maintain the average capacitor voltage to a constant value. Peak value of the current (I_{max}) so obtained, is multiplied by the unit sine vectors in phase with the respective source voltages to obtain the reference compensating currents. These estimated reference currents I_{sa}; I_{sb}; I_{sc} and sensed actual currents (Isa, Isb, Isc) are compared at a hysteresis band, which gives the error signal for the modulation technique. This error signal decides the operation of the converter switches. In this current control circuit configuration, the source/supply currents I_{sabc} are made to follow the sinusoidal reference current I_{abc}, within a fixed hysteretic band. The width of hysteresis window determines the source current pattern, its harmonic spectrum and the switching frequency of the devices.

The DC link capacitor voltage is kept constant throughout the operating range of the converter. In this scheme, each phase of the converter is controlled independently. To increase the current of a particular phase, the lower switch of the converter associated with that particular phase is turned on while to decrease the current the upper switch of the respective converter phase is turned on. With this one can realize, potential and feasibility of PI controller [13].

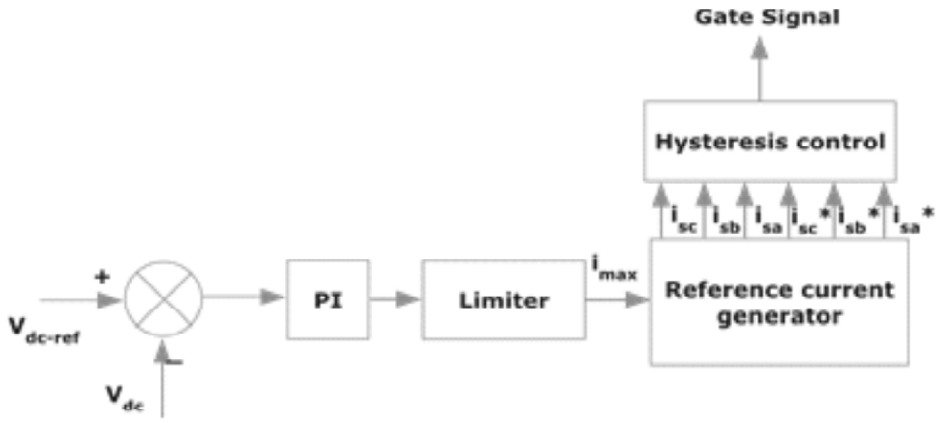

Figure 4: PI Controller

5. ARTIFICIAL NEURAL NETWORK

Fig. 5 shows the structure most commonly used feedforward, multilayer, back propagation type network. The name back propagation comes from its training method. Often it is called a multilayer perception (MLP) type network. The input signals ae shown as (x_1, x_2, x_3……x_n) and the the output signals are shown as (z_1, z_2, z_3……z_m). In general these signals may be logical, discrete bi-directional, or continuous signals. The links shown always carry the signals in the forward direction. In fact, the circles contains the summing node of the neuron with the activation function and the synaptic weights are shown by dots in the links (often dots are omitted).

The network shown has three layers of neurons; input layer, hidden layer, and output layer. The hidden layer functions to associate the input and output layers. The input and output layers have neurons equal to the respective number of signals. The input layer neurons have linear activation functions with unity slope (or no activation function), but there is a scale factor with each input to convert them to per unit (normalization) signals. Similarly, the output signals are converted from per unit signals to actual signals by renormalisation. Since the input layer acts as a distributor of signals to the hidden layer, it is often defined as a two layer network. A constant bias source supplies the bias signals to the hidden layer and output layer (not shown) neurons through a weight. The bias circuit are often omitted for simplicity. There may be more than one hidden layer depend on the complexity of the problem to be solved.

The architecture of the neural network makes it evident that basically, it is fast and massive parallel output multidimensional computing system, where computation is done in a distributed manner.

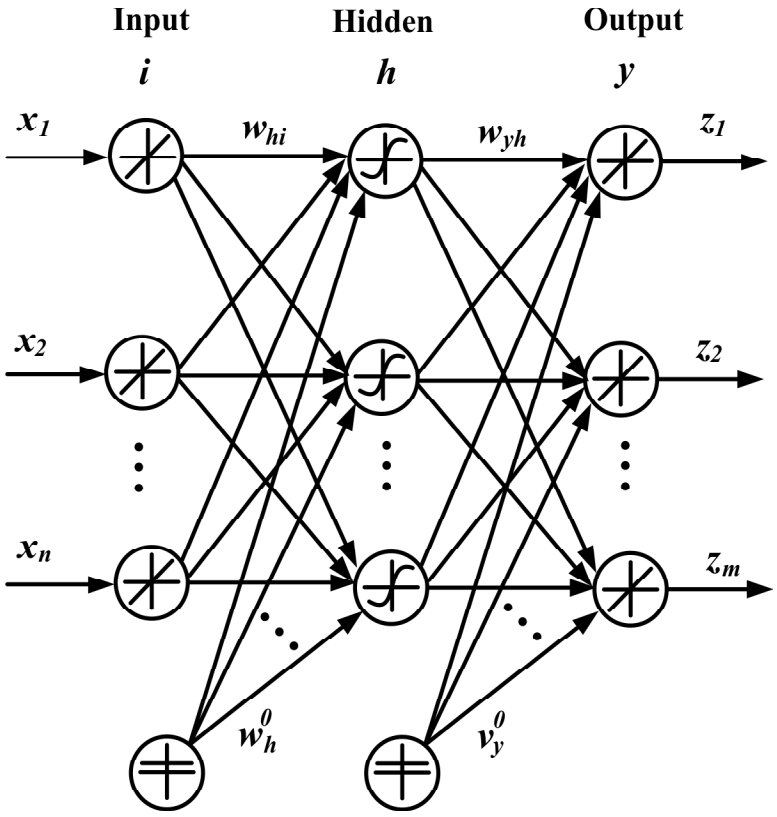

Figure 5: Structure of Feed- forward three layer neural network

Consider the vector x as a d- dimensional input pattern vector with the unity bias augmented to it. The input vector *x* presented to the input layer can be expressed as [27]

$$x = [x_1 x_2 \dots \dots x_n \; 1]^T \tag{13}$$

The weights connecting the input neurons to the h[th] hidden neuron can be expressed in the vector format (w_h) as

$$w_h^T = [w_{h1} w_{h2} \dots \; w_{hn} w_h^0] \tag{14}$$

Each hidden unit (h) computes the weighted sum of its inputs to produce its scalar net activation, denoted as net_h. Therefore, the output of the hidden unit h can be expressed as

$$net_h = w_h^T x = \sum_{i=1}^{n} w_{hi}\, x_i + w_h^0 \tag{15}$$

Where the subscript (i) denotes the i[th] neuron, and (n) the number of features in the input vector

Each hidden neuron emits a nonlinear output (O_i) of its net activation (net_y), which can be expressed as

$$O_k = f(net_h) \tag{16}$$

Where f is the tan-sigmoidal function that can be expressed as

$$f(net_h) = \tanh(net_h) \approx \frac{2}{1+e^{-2net_h}} - 1 \tag{17}$$

Similarly, each output neuron (y) computes its net activation (net_y) as the weighted sum of the hidden neurons outputs as follows:

$$net_y = v_y^T O = \begin{bmatrix} v_{y1} \\ v_{y2} \\ \vdots \\ v_{yh} \\ v_y^0 \end{bmatrix} [o_1 o_2 \dots \ o_k \ \ 1] = \sum_{h=1}^{k} v_{yh} O_h + v_y^0 \tag{18}$$

Where v_{yh} denotes to the weight connecting the h[th] hidden neuron to the y[th] output neuron, v_y^0 the bias at the output neuron (y), and k represents the number of hidden neurons.

In function approximation and estimation applications, the output neuron net activation (net_y) is processed by a pure linear operator. Therefore, the estimated output (z_y) at the y[th] output neuron is equal to its input net activation (net_y). The estimated output can therefore be written as

$$z_y = net_y = \sum_{h=1}^{k} v_{yh} f(\sum_{i=1}^{n} w_{hi} x_i + w_h^0) + v_y^0 \tag{19}$$

Now the objective is to train the network weights (w_{hi}, v_{yh}) such that the estimated outputs (z_y) are equal to the targets (tg_y) (supervised learning). In feed- forward MNN, the weights are trained by the so- called back propagation algorithm.

The aim is to minimize some form of the error function between z_y and tg_y. The training error (e_y) of one sample can be simply defined as

$$h_y = \frac{1}{2}(e_y)^2 = \frac{1}{2}(t_{gy} - z_y)^2 \tag{20}$$

Where h_y the criterion function at the y[th] is output node and e_y is the sample error at the output node y.

The back propagation algorithm is based on the GD procedure. The gradient of the criterion function is taken with the respect to the input- hidden weights(w_{hi}, w_h^0) and hidden- output(v_{yh}, v_y^0) weights. Since the output neuron has a direct teacher (tg_y), let us first apply the GD on the output layer as follows:

$$\nabla h\left(v_{yh}\right) = -e_y . \frac{\partial z_y}{\partial v_{yh}} = -e_y . o_h \tag{21}$$

$$\nabla h\left(v_y^0\right) = -e_y . \frac{\partial z_y}{\partial v_y^0} = -e_y \tag{22}$$

The input- hidden weights are updated by computing the gradient with respect to w_{hi} through the chain rule

$$\nabla h\left(w_{hi}\right) = -e_y . \frac{\partial z_y}{\partial w_{hi}} = -e_y . \frac{\partial z_y}{\partial net_h} . \frac{\partial net_h}{\partial w_{hi}} = -e_y . v_{yh} . f'(net_h) . x_i \tag{23}$$

Similarly

$$J\left(w_h^0\right) = -e_y . \frac{\partial z_y}{\partial w_h^0} = -e_y . v_{yh} . f'(net_h) \tag{24}$$

Where

$$f'(net_h) = \frac{4e^{-2net_h}}{(1+e^{-2net_h})^2} = 1 - [f(net_h)]^2 \quad (25)$$

The update terms contain the training error sample (e_y) computed at the output layer. This explains the name back propagation as the error at the output layer, during training, propagates back from the output layer to the hidden layer to update the input- hidden neurons.

The update rules for the hidden- output and input hidden synapses can thus be summarized as

$$v_{oh}^{p} = v_{oh}^{p-1} - \eta_v . \nabla h^p(v_{oh}) = v_{oh}{}^{p-1} + \eta_v . e_o . o_h \quad (26)$$

$$(v_y^0) = (v_y^0)^{p-1} - \eta_v . \nabla h^p(v_y^0) = v_{yh}^{p-1} + \eta_v . e_y \quad (27)$$

$$w_{hi}^{p} = w_{hi}^{p-1} + \eta_w . e_y . v_{yh} . f'(net_h) . x_i \quad (28)$$

$$(w_h^0)^p = (w_h^0)^{p-1} + \eta_w . e_y . v_{yh} . f'(net_h) \quad (29)$$

Where η_v and η_w are the learning rates for the hidden-output and input-hidden weight update rules respectively.

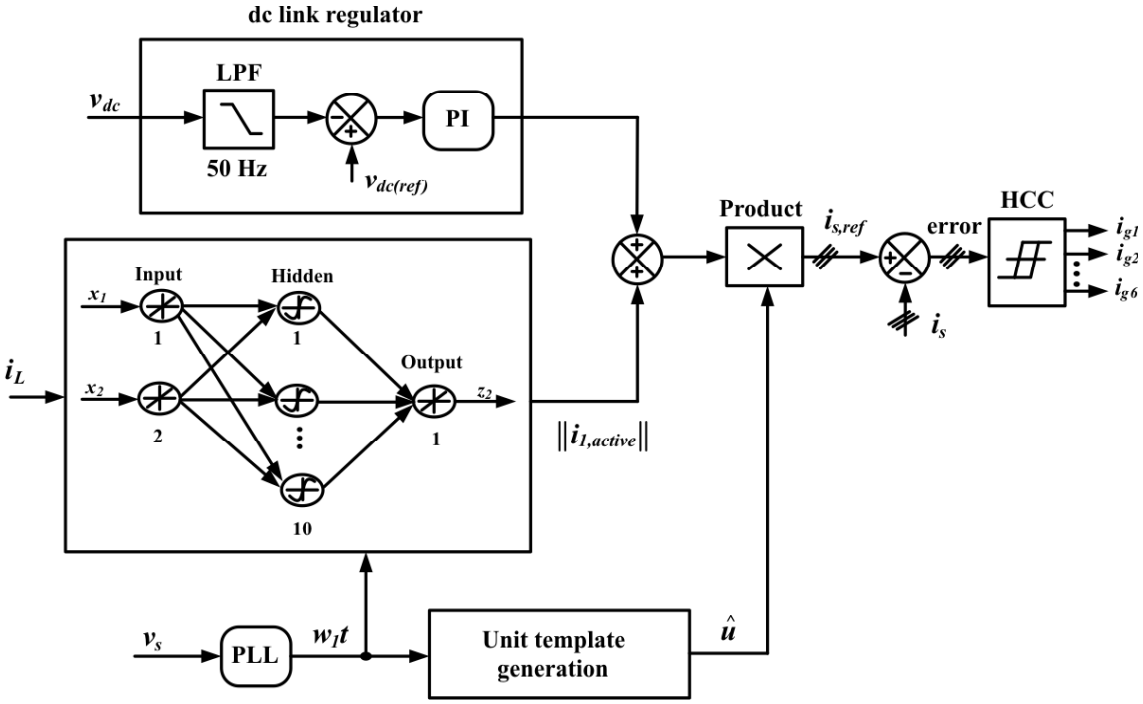

Figure 6: Shunt APF control configuration using ANN structure

6. RTDS HARDWARE

Real-time digital simulator (Fig. 7a) was developed with the aim of meeting the transient simulation needs of electromechanical drives and electric systems while solving the limitations of traditional real-time simulators. It is based on a central principle: the use of widely available, user-friendly, highly competitive commercial products (PC platform, Simulink™). The real-time simulatorconsists of two main tools: a real-time distributed simulation package (RT-LAB) for the execution of Simulink block diagrams on a PC-cluster, and algorithmic toolboxes designed for the fixedtime-step simulation of stiff electric circuits and their controllers. Real-time simulation and Hardware-In-the-Loop (HIL) applications are increasingly

recognized as essential tools for engineering design and especially in power electronics and electrical systems.

The real-time digital simulator hardware used in the implementation of the RTDS [28] is modular, hence making it possible to size the processing power to the simulation tasks at hand. The OP5142 shown in Fig.7b is one of the key building blocks in the modular OP5000 I/ O system from Opal-RT Technologies. It allows the incorporation of FPGA technologies in RT-LAB simulation clusters for distributed execution of HDL functions and high-speed, high-density digital I/O in real-time models. Based on the highest density Xilinx Spartan-3 FPGAs, the OP5142 can be attached to the backplane of an I/O module of either a Wanda 3U- or Wanda 4U-based Opal-RT simulation system. It communicates with the target PC via a PCI-Express ultra-low-latency real-time bus interface. As can be seen, the simulator can take on several forms including a new portable version which can easily be transported to a power-plant or substation for on-site pre-commissioning tests. Each rack of simulation hardware contains both processing and communication modules. The mathematical computations for individual power system components and for network equations are performed using one of two different processor modules.

7. SIMULATION AND RTDS RESULTS

Figs. 8a, 8b and 8c give the details of Source Voltage, Load Current, Compensation current, Source Current with filter, DC Link Voltage, T.H.D (Total harmonic distortion) under balanced, un-balanced and non-

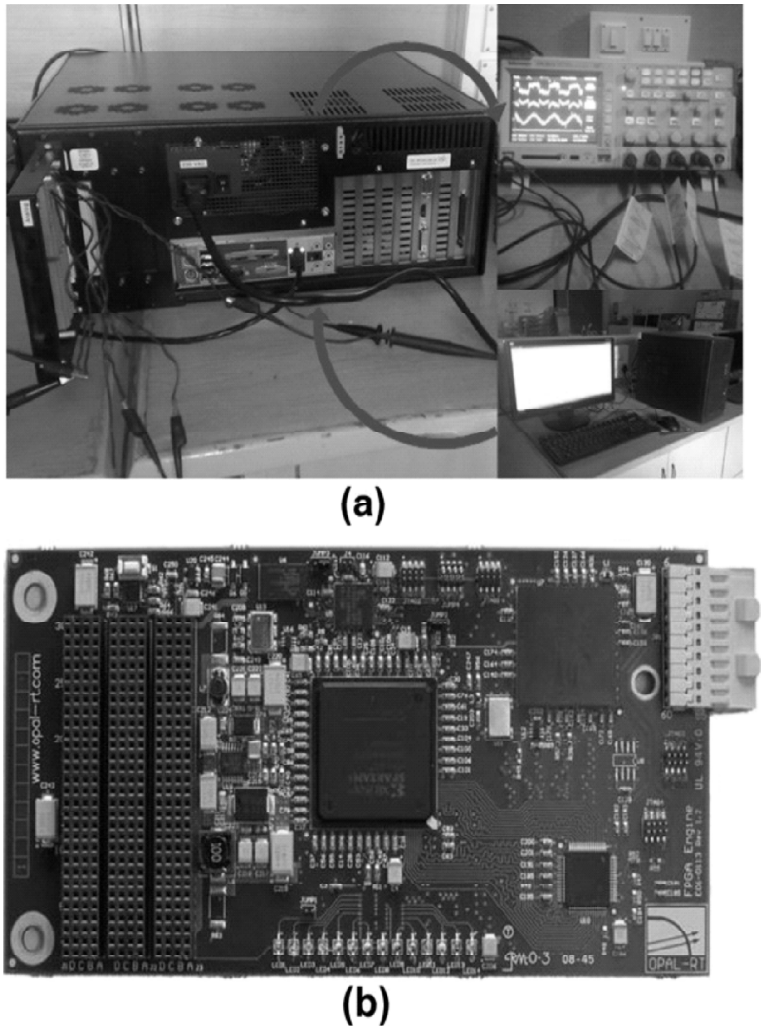

Figure 7: (a) RTDS Hardware. (b) OP5142 layout and connectors

sinusoidal supply voltage condition using I_d–I_q control strategy with PI and ANN with PI controllers using Matlab and RTDS Hardware respectively.

Fig. 8a illustrates the performance of shunt active power filter under balanced sinusoidal voltage condition, THD for i_d–i_q method with PI Controller using Matlab simulation is 1.97% and using RTDS Hardware is 2.04%; THD for ANN with PI using Matlab simulation is 0.97% and using RTDS Hardware is 1.26%.

Fig. 8b illustrates the performance of shunt active power filter under un-balanced sinusoidal voltage condition, THD for i_d–i_q method with PI Controller using Matlab simulation is 3.11% and using RTDS Hardware is 3.26%; THD for ANN with PI using Matlab simulation is 1.64% and using RTDS Hardware is 1.94%.

Fig. 8c illustrates the performance of shunt active power filter under distorted (non-sinusoidal) voltage condition, THD for i_d–i_q method with PI Controller using Matlab simulation is 4.92% and using RTDS Hardware is 5.05%; THD for ANN with PI using Matlab simulation is 3.01% and using RTDS Hardware is 3.54%.

Table II clearly illustrates the amount of THD reduced from method to method under balanced, unbalanced and non-sinusoidal conditions using Matlab and RTDS Hardware. When the supply voltages are balanced and sinusoidal, PI and Fuzzy logic controllers are converging to the same compensation characteristics. However, under unbalanced and non-sinusoidal conditions the I_d–I_q method with FLC shows superior performance.

While considering p–q control strategy using FLC with triangular M.F. SHAF succeeded in compensating harmonic currents, but notches are observed in the source current. The main reason behind the notches is that the controller failed to track the current correctly and thereby APF fails to compensate completely. It is observed that, source current waveform is good; notches in the waveform are eliminated by using I_d–I_q control strategy with FLC triangular M.F. The system parameters are given in Table I.

Table I
System parameters

Parameter	*Value*
Supply voltage	V_s = 230 V
Source resistance	R_s = 0.1 X
Source inductance	L_s = 1 mH
Filter phase-branch resistance	R_f = 0.01 X
Filter phase-branch inductance	L_f = 0.1 mH
DC link capacitance	C_{dc} = 3000 lf
DC link voltage	V_{dc} = 800 V
Hysterisis band	±0.2 A
Load resistance	R_L = l5 Ω
Load inductance	L_L = 60 mH

Performance of shunt active power filter under balanced sinusoidal voltage condition

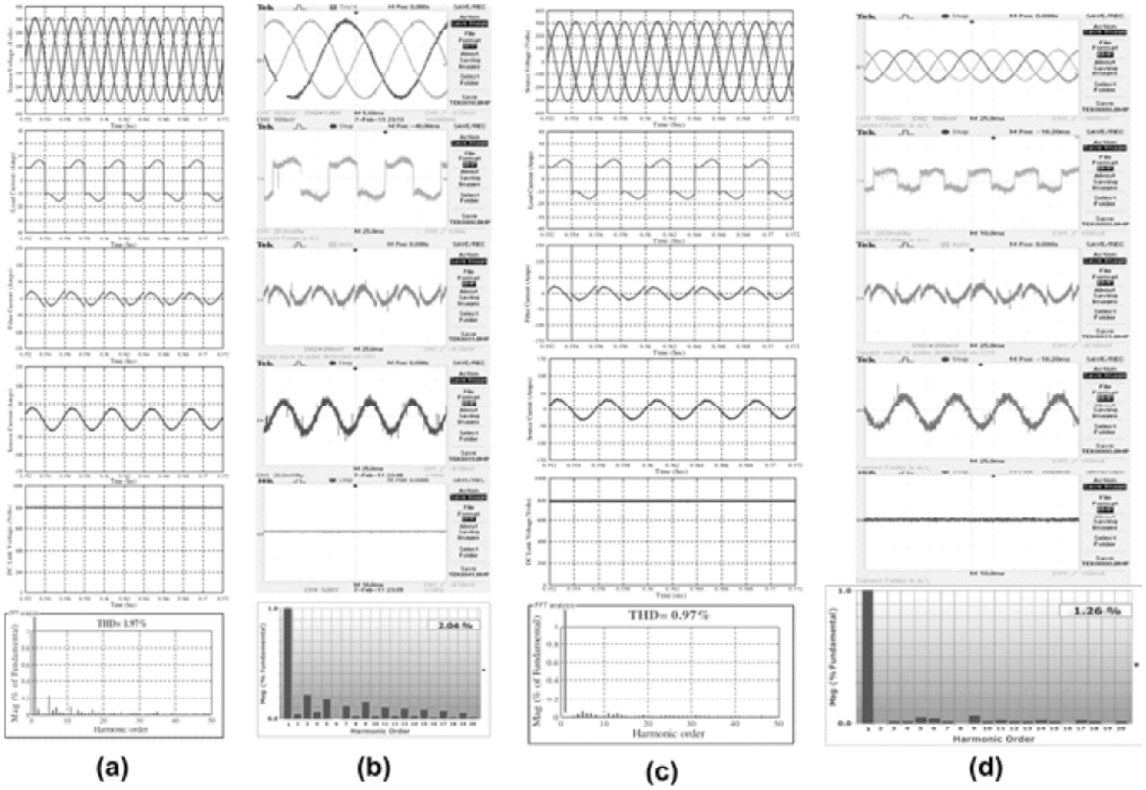

Figure 8a: Performance of SAPF under balanced sinusoidal condition: (a) i_d–i_q with PI in Matlab, (b)) i_d–i_q withPI in RTDS, (c) ANN with PI in Matlab, and (d) ANN with PI in RTDS

Performance of shunt active power filter under unbalanced sinusoidal voltage condition

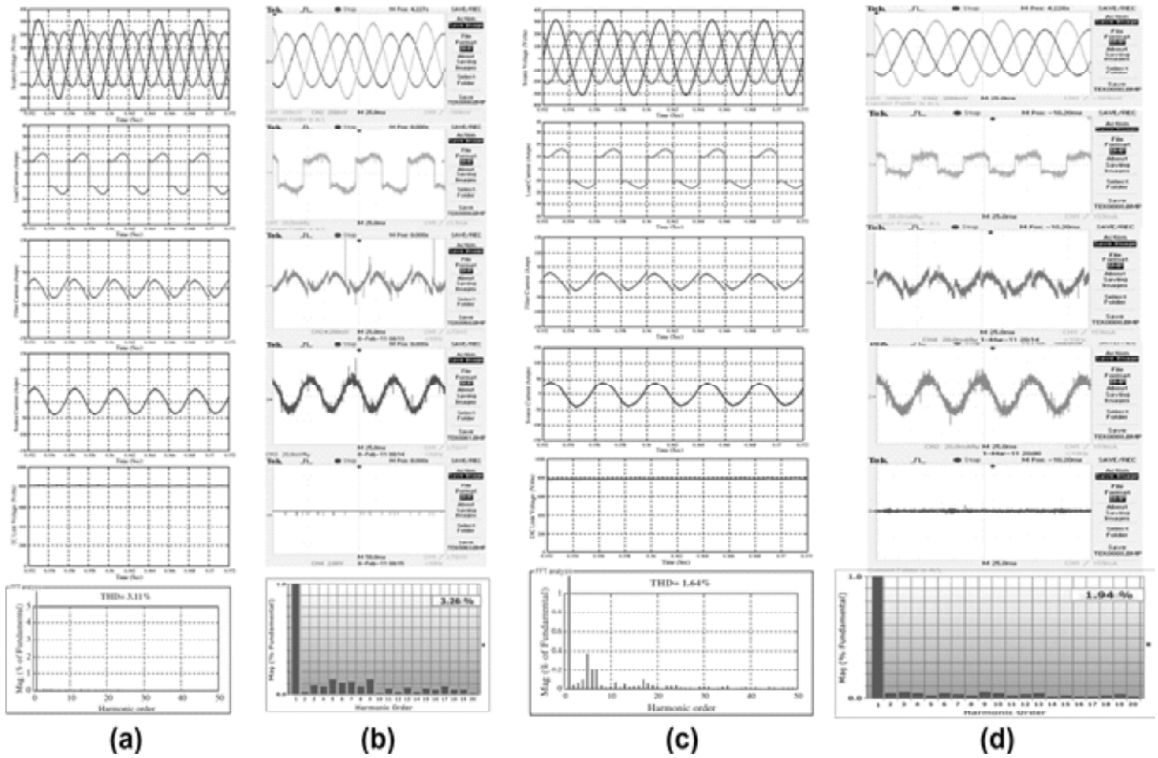

Figure 8b: Performance of SAPF under un-balanced sinusoidal condition: (a))i_d–i_q withPI in Matlab, (b) i_d–i_q withPI in RTDS, (c) ANN with PI in Matlab, and (d) ANN with PI in RTDS

Performance of shunt active power filter under distorted(non-sinusoidal)voltage condition

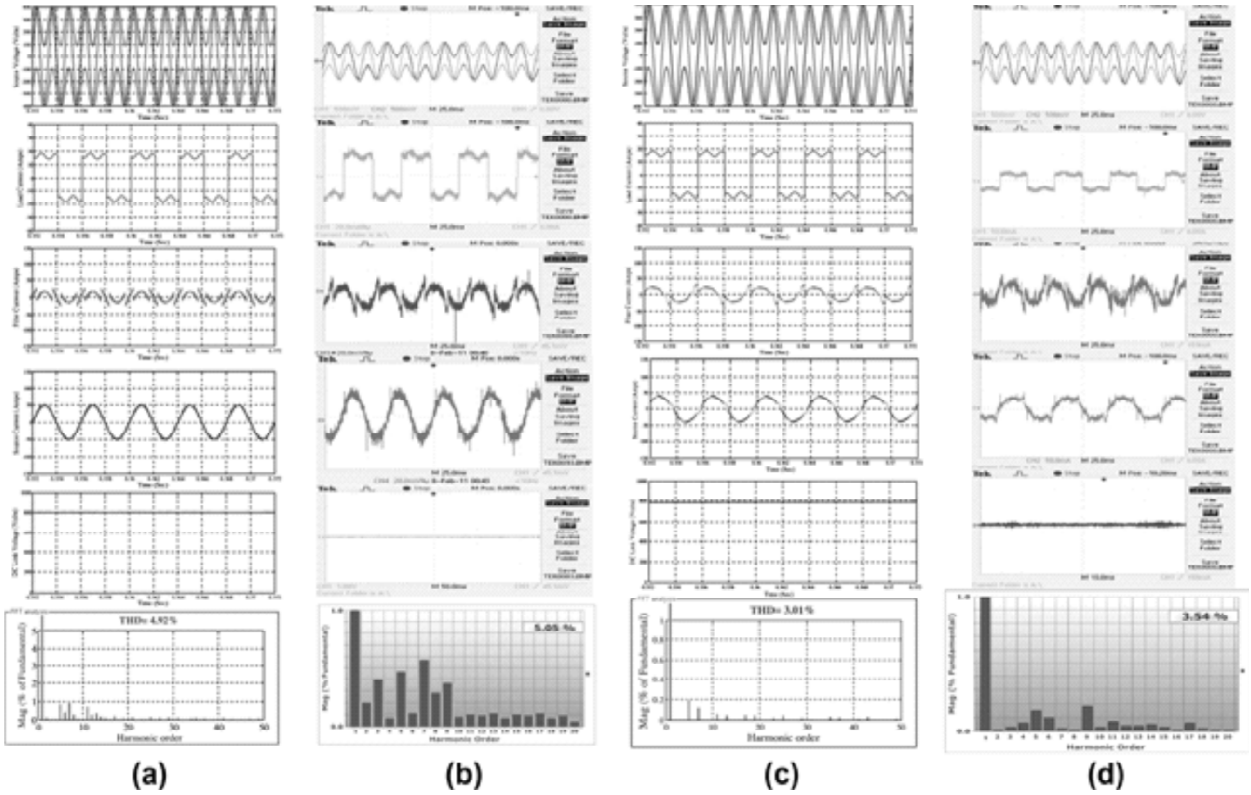

Figure 8c: Performance of SAPF under distorted (non-sinusoidal) condition:(a))i_d–i_q with PI in Matlab, (b) i_d–i_q with PI in RTDS, (c) ANN with PI in Matlab, and (d) ANN with PI in RTDS

Table II
% THD Comparison

	I_d–I_q with PI		*ANN with PI*	
	%THD in MATLAB	*%THD in RTDS*	*%THD in MATLAB*	*%THD in RTDS*
Balanced Sinusoidal Input	1.97	2.04	0.97	1.26
Unbalanced Sinusoidal input	3.11	3.26	1.64	1.94
Distorted (non-sinusoidal) Input	4.92	5.05	3.01	3.54

8. CONCLUSION

In the present paper two control strategies; current control strategies (i_d– i_q) with PI and ANN with PI have been implemented for the three-phase four-wire distribution SAPF system to improve the performance under balanced, un-balanced and non-ideal supply voltage condition. The control scheme using three independent hysteresis current controllers has been implemented. The operation and modelling of the SAPF have been described. A real-time implementation SAPF has been carried out on RTDS.The Real-time implementation and simulation results showed that even if the supply voltage is non-sinusoidal the ANN with PI shows better performance in mitigating the current harmonic than that of i_d–i_q theory with PI controller.

While considering the ANN with PI controller the SAPF has been found to meet IEEE 519-1992 standard recommendations on harmonic levels during balanced, un-balanced and non-ideal supply voltage conditions. The control approach has compensated the neutral and harmonic currents and the dc bus voltage of SHAF is almost maintained to the reference value under all disturbances.

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