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A Novel Clock Divided Address Generator with Hamming Encoder for Implementing the LFSR for Low Power Memory BIST Applications

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ABSTRACT

In recent advancement in field of high speed computation in VLSI technology, the testing was essential for the Memory. Also the Network on chip memory cores the Build in Self-Test (BIST) was essential while manufacturing. There have been lots of research schemes are proposed for testing of memory circuits. Major testing element for the testing of memory was Linear Feedback shift Register (LFSR). LFSR used for generating random address at constant speed while testing of the Memory circuits. The main problem of using LFSR was it using switching activity for the operating the switching activity directionally proportional to the power dissipation. In this paper we are suggesting the novel clock splitting logic based LFSR for low power testing applications with this we are adding hamming distance based data encoder for the purpose of the detecting stuck at faults usually presents in the Memory circuits. Here we are design and implemented the proposed scheme using the Xilinx ISE tool and the outcome results are showing that the proposed scheme having nearly 90% power efficiency, 50% of Area efficiency and nearly 98% High Fault coverage when compares to conventional systems.

Keywords: BIST, LFSR, Hamming Error Correction, Stuck at Fault, Low Power, Clock Divison

INTRODUCTION

During the production of Integrated Chips enormous of failures will occur due to the production error and design error. However we applied lot of expert peoples working line we can’t eliminate these IC failures. The detection and elimination of these failure ICs was too difficult in real time we can’t test these IC individually. In manufacturing department these fault models are grouped into different clusters depending upon the fault type. The fault present in ICs was classified into three different types namely PermanentFault, Temporary Fault, and Delay Fault. The permanent Fault will effect for the Long time in the IC and we can’t eliminate this Fault easily unless recreation of ICs. And temporary Fault will appear and disappear at short period of time due to the time varying IC property. Finally the Delay Fault depends upon the operating speed of the ICs. Testing and debugging of the Circuits was more important and complex task in the very large scale integration industry. Lot of methodsis practically used to test the circuits at the manufacturing stages. The two major schemes for testing was follows DFT (Design for Test), ATPG (Automatic Test Pattern Generation). DFT scheme having more advantages compare to the ATPG due to its fast processing rate, testability rate and high complexity. In recent times VLSI semiconductor industry effects lot of advancement which leads to the hundreds to thousand number of in build transistor count. It leads to increased complexity are in the testing schemes. In VLSI Industry Power and Overall delay were the major factors in the Design concern. In recent years emergence in portable Mobile devices leads to the reduction in the power dissipation not only the circuit power also in testing Power.

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During Testing Process we have to optimize the testing speed and testing power. If these testing vectors are not optimized for the Power Means these CUT (Circuits under Test) will dissipate the double the amount of power when compare to the Normal operating Conditions. While researching this reason we found that these testing circuits need large amount of testing vectors its leads to the high power dissipation.These testing vectors produced by the test circuit were independent of the CUT and its leads to the higher clocking period also effect that higher power dissipation.

As a result we have to optimize these testing parameters, these parameters includes testing speed, power dissipation while Testing, Fault Coverage Rate and Overall Testing Circuit Area.Reduction and these factors like Testing Power, Testing Time, Fault Coverage and Overall Area was complex for Designing Industry Concern.So that many researchers have focused improvement in the existing LFSR to reduce the Overall Testing Delay and Testing Power. In such a way the researchers reduced the overall Testing Power as well as Testing Time of the BIST (Build inSelf-Test).

The major issue for the testing engineers was higher power consumption while testing the circuit. Nearly 200% power will power will use when compare to the normal usage. There are two kind of the power dissipation problem present in the testing circuits.

The overall testing power directly depends on the switching logic of the circuit. It can describe by the following formula,

$$P_{avg} = \alpha T \,.\, C_{load} V^2_{dd} f_{Clk}$$

Where P avg means that average power usage and αT means that switching that switching pulses for the Logic Testing Circuit.

Memory cores are playing important roles in the system on chip as well as network on chip cores. Also memories are important factors in the DSP related circuits also.

The testing of memory circuits was highly important in the VLSI application due to its application. However previous works MBIST are discussed about the testing of the memory cores. The ATPG (Automatic Test pattern Generator) plays a significant role in the testing of Memory Cores. The main limitation of the MBIST technique was it using Large area as well as testing speed was too slow when compare to the Other testing techniques used rather than the Memory Circuits.

While testing of memory circuit the testing circuit will generate the large amount of the random address patterns as well as continuous working operation cycles. This will need continuous clock or switching pulses.This leads to the higher amount of Power Losses.

Figure (1) describes the overall block diagram of the testing circuit of the memory related testing method. The read write pin describes the operation of the whether we are going to read or write the data to

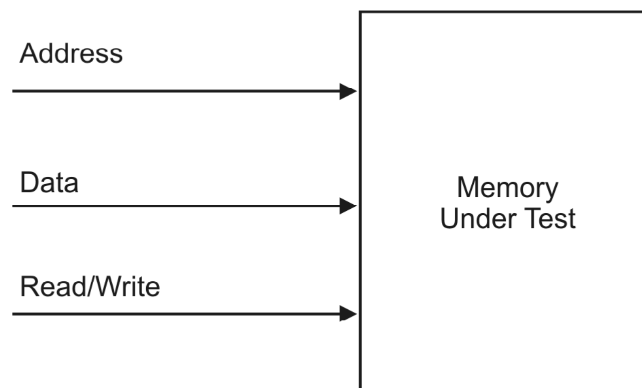

Figure 1: Block diagram of Memory Testing Circuit

memory core. The data pins describethe application of which data we are going to read or write from the memory core. Address port important for the Automatic testing method. Which need continues and random no of address bits to check the Memory cores.

The MBIST testing circuit combines the Multiplier circuit and generates the ungues sable random number that is random address bit as input to the memory under test. In other Memory testing schemes Grey codes and binary updown counters are employed to generate the input address bits to the circuit under test.

The main problem of this conventional methods are they are consuming huge amount of area usage and generates the address bits with cyclic procedures the chance of repeating the address bits was high when compare to the recent methods.

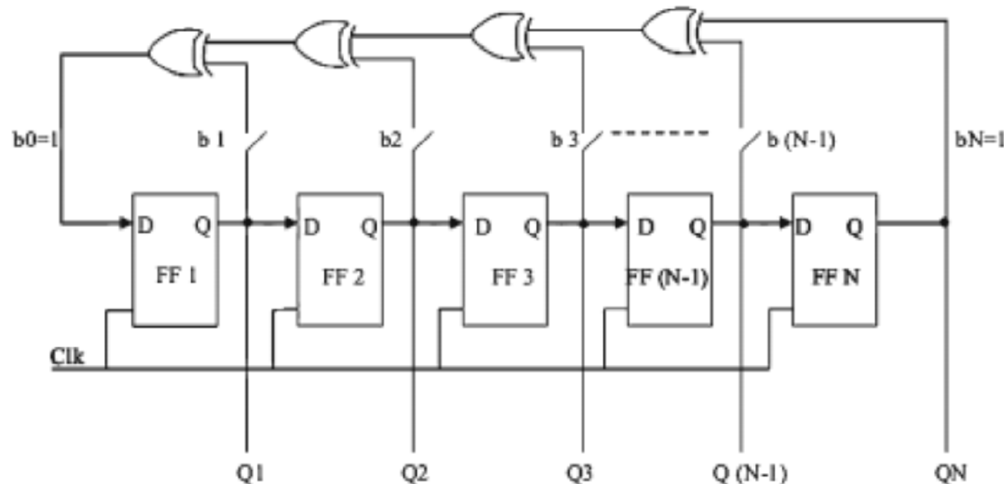

Figure 2: Conventional Circuit of Address Generator

The Above figure (2) describes the overall block diagram of the Traditional LFSR circuit used to generate the random bits to the memory under test circuits. Here the N bit address generating traditional LFSR was presented. The flipflop circuits are used to store and generate q value and each output of the each flipflop circuits were XOR with previous output and by this way the traditional LFSR circuit can generate the random address bits to the Memory under test. The main focus of the circuit was here common clock was applied to switching the circuitfour generating the Nth bit of the LFSR the clock generating circuit should generate the N number of clocking bits to obtain the final output bit. However this traditional LFSR uses the Minimal Hardware area the overall clock applied to the LFSR circuit was too high so that switching activity was higher for this type of LFSR circuit.

The switching activity directly proportional to the Average testing power the so that this circuit uses high power dissipation when compare to our proposed system. Also the major problem for the existing system was to detect the stuck at “1” fault and stuck at ‘0’ fault. The meaning of those faults refers to the if we stored the data ‘1’ in the memory while reading the data the outputs shows the “0”, these faults called as the stuck at “0” faults.

Same like if we stored “0” in memory but it shows “0” while reading means this is called as the stuck at “0” fault. These type of faults are called as stuck at faults. In our proposed system we are going to design a LFSR with clock splitting logic in this method we are going to design a LFSR system by dual spilling logic. The LFSR designed by the N/2 logic, where N stands for the total size of LFSR address generator. We are splitting the LFSR into 2 units where we are applying the two different clock logics for LFSR units. And then after generating random address using the LFSR unit we are encoding the another data generated by the LFSR unit, here we are applying the hamming distance based encoding scheme using that we are

adding parity bits to our data before storing that into our memory. And the while reading that data we are applying the applying the hamming decoding to detect that stuck at fault of the memory's.

Literature Survey

In previous research works, Researches proposed lot of testing schemes to produce the better efficient testing factor results. In section briefly describes the conventional research scheme with their algorithm.

Stuck at Fault detection tool (Yu Zhang et al 2005, Bei Zhang Leeet al)used to obtain the testing results of testing delay by using the automatic test pattern generation algorithm. In this scheme the testing scheme contains the two different type of testing modes described as launch off capture (LOC) or launch off shift (LOS) mode. Depending upon the two different operating modes complexity of the test pattern generated to the testing circuit was controlled reduced. Also this method reduced the transitiontesting delay of the Circuit under Test as well as this method reduces the overall testing power.

Efficient LFSR Reseeding Technique (Wei-Cheng Lien et al 2005 Kuen-Jong Lee et al 2005) suggestedtoeliminate the storage cost of the testing circuit for storing all the generated testing seeds. This method controls the test pattern circuit by using the control logic and inversion based LFSR Module. The real time generated seeds are compared with output response with internal and external memory cost.

WeizhengWang(2012) in this technique, and innovative Digital Fourier Transform (DFT) based scheme to eliminate the testing delay and overall testing power. ATPG generated testing seeds are applied to the DFT circuit it will compress the testing seeds into the minimum range of seeds, by this technique overall number of test patterns was reduced. Also the DFT passed testing pattern having the property of the multiple testing seeds. So that overall power and testing delay was reduced to obtain the better result.

Jiri Balcarek et al[2014] suggested the compression based algorithm which compresses the testing seeds into lesser number of seeds which benefits in reduction of testing time as well as processing power which is discussed in earlier. But the main drawback of the process was it don't care about the fault coverage of the algorithm as well it leads to poor experimental results.

K. Murali Krishna et al [2014] suggested MemoryBuilt in Self-Test Address Generator with address module with LFSR generated Seeds operating under two different clock signal. It helps to reduce the switching complexity of the testing circuit. Switching time directionally proportional to the power consumption of the circuit.So that overall power usage of the circuit was reduced into lesser value.

Fundamental types of faults in VLSI circuits (Needham et al 2005) are the following: particles (small bits of material that bridge two lines), incorrect implant value, incorrect spacing, holes (exposed area that is unexpectedly etched), misalignment, weak oxides, and contamination. These defects leads to flawed behavior of the circuit which can be determined either by logic testing (Abramovici et al 2006) or parametrical testing (Rajsuman et al 2006). Parametric testing includes measuring the current flowing through the power supply in the quiescent or static state (Rajsuman et al 2007).

ToubaNA(2008) All the test data compression techniques fell into any one of this category: Code-based schemes, Linear-decompression-based schemes and Broadcast-scan-based schemes. Code-based scheme compression involves partitioning the original test data into symbols and replaces it by a code word according to its specific property to encode the data. In the decompression area the decoder simply replace the code word by the specific symbols . A variable-to-variable length GOLOMB coding is proposed which give a low cost, very high compression with a scalable on-chip decoder. Another variable-to variable length compression technique called frequency-directed run-length (FDR) codes distributes the runs of 0's in the test sequence.

The maximum run-length can be limited to tradeoff compression ratio by combining both run-length and Huffman coding called RL-HC. A block merging technique is used to merge many consecutive test blocks to reduce the test data volume in D. Czysz, G. Mrugalski(2012).

Both test data volume and dictionary volume are reduced by having smaller number of codeword for larger block size . A new horizontal compression technique is used M. F. Wu et.al,(2009) for multiple cores. A new encoding technique by X. Liu and Q. Xu, (2009) with more flexible control code to attain high data compression is called scan slice encoding. A compression technique is proposed which combines hamming Distance Based Reordering (HDR), Column wise Bit Stuffing (CBS) and Difference Vector (DV). The scheme preprocesses the test data before applying any other compression technique for giving better compression].

PROBLEM DEFINITION

The main problem of the previous research methods was they are focusing only on the scaling of the circuit the scaling will reduce the overall power but main drawback of the existing system was it can affect the overall performance of the circuit, scaling will leads to the performance reductions in the circuits.

Normally the over power of the circuit was nearly 200% when compare to normal usage because it can handle the large amount of the data while under the testing mode also while testing the circuit we need large number of clock for operating. Usually clocking and switching directionally proportional to the overall power dissipation, testing will leads to the higher amount of power dissipation while testing the circuit.

Also testing will need additional circuit of processing, although it needs additional circuits it unable to process the power efficient process and fault coverage process simultaneously. So the stuck at faults have been major problem in the Ram memory element. Usually stuck at fault will be the major fault in the RAM circuits.

Single Event Upset (SEU) single event upset also the major concern in the RAM memory element. The SEU stands for the photovoltaic disorder happens on the RAM circuits. It will arise due the unmoral radiation on the Memory Area. It will changes the stored data's form "0" to "1" as well as "1" to "0". Usually there are no testing methods available for the type of the problems. This will leads to the higher fault possibility in the RAM circuits.

The proposed testimg circuit capable of reducing the overall testing power as well as it can capable of overcoming the stuck at faults and Single Event Upset usually happens in the RAM memory cells. The proposed circuit capable of having inbuilt hamming encoder and decoder circuit and using that it can encode the data which is going to store be store in the memory. As well as it having clock splitting logic for reducing the overall power dissipation of the circuit.

Research Methodology

Switching activity of the testing was playing the major role in the power reduction technique. Due to the unwanted switching of the sequential circuits will leads to the unnecessary power wastage. The relationship between the overall power and switching activity described as following formula

$$P=CV2\ f$$

Where P stands for the overall power consumption of the circuit while testing and F stands for the switching activity of the circuit. Using that relationship we can stat that the switching activity directionally proportional to the overall testing power. To efficiently handle the switching activity we need to apply the clock splitting logic in LFSR circuit. To achieve the superior power reduction the major clock using unit was LFSR. Here LFSR used for the purpose of the generating the random address for the memory under test. So that we have apply improvised clocking scheme for the LFSR circuit and have to reduce the overall power consumption.

Also the stuck at faults also the major concern in the testing of Memory circuit, now a days the size of memory cells are dramatically increased due to the transistor scaling advancement. So the stuck at faults

are the usual faults randomly occurs in the memory cells.The proposed method capable of handling the high fault coverage on the RAM memory cell. Hamming technique was the reliable technology for the parity related codes. In our proposed system we are applying the hamming distance codes to encode the data which we are going to store and also we are applying the appropriate decoding scheme to detect the stuck at faults in stored or data which read form the Memory.

The switching activity in LFSR can be greatly reduced by decreasing the bit transition between the consecutive memory address and also by an appropriate clock gating. A decrease in the correlation in the model also has a resultant effect of keeping down the switching activity.

PROPOSED SYSTEM

The proposed LFSR design generally concentrate on the clock splitting logic which was based on the N-2 logic where N stands for the overall bit size of LFSR unit. If our memory cell having 32 bit size means the LFSR step will be calculating by the following formula $2^N = 32$ so that N = 5.the Step size of the LFSR unit was 5 the for generating the clock splitting logic we are applying that N-2 formula so the final proposed LFSR address generator divided into 3,2 units.

We applying the different clock for the 3 unit LFSR and different switching clock for the 2 unit LFSR. The output of the 2 bit LFSR considered as the MSB of the Final generated address and output of the 3 bit LFSR considered as the LSB of the generated address.

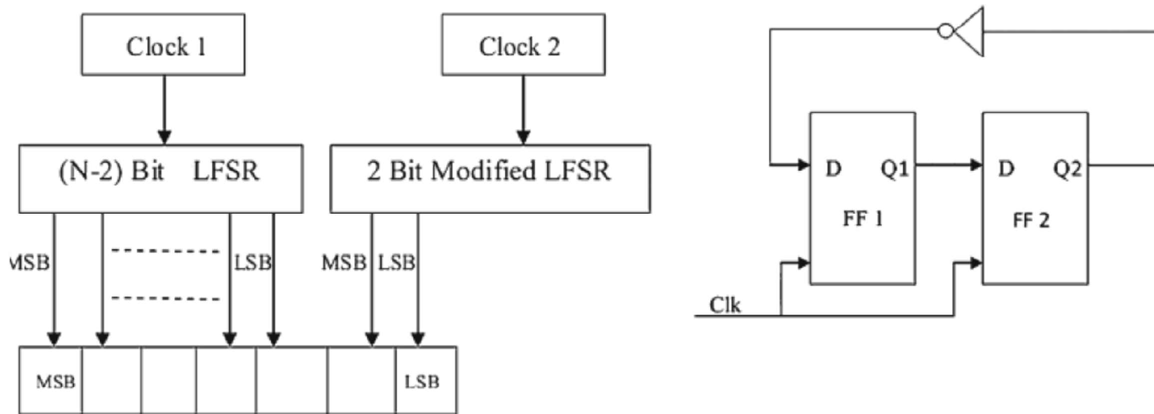

Figure (3a): Proposed Clock Splitting LFSR address Generator Figure (3b) 2 Bit LFSR

The figure (3a) represents the overall working of the proposed LFSR design and here we are separating the LFSR into 3,2 unit the figure (3)b represents the splits logic of the 2 bit LFSR here we are applying the two different clock pulses to the 2 bit LFSR and using that 2 Bit LFSR we are deriving the following operation. When the initial stage of first Flipflop equal to 1 then the next flipflop also getting 1 as a output. The final output for the first cycle clock was Q1=0 then the second cycle output was Q2=1. Then the these Q1 and Q2 are taken as the MSB of the final LFSR generated address and the second operation we needs to divide the clock for second stage LFSR and the resultant of the overall LSB and MSB of the LFSR generated outputs are considered as the final Address of testing of the memory processor. The different between the two clock pulses are shown in the figure(4) below.

Then second module of our project was we have detect the stuck at faults present in the memory cell for that we are generating the random data for saving in the memory and then we are encoding those bits using the hamming distance based encoding here we are adding parity bits between the data which was generated using the LFSR circuit. We are converting the 4 bits data into 7 bits and we are storing those data's into memory cell after storing of that data we are giving input address and we are verifying the data with

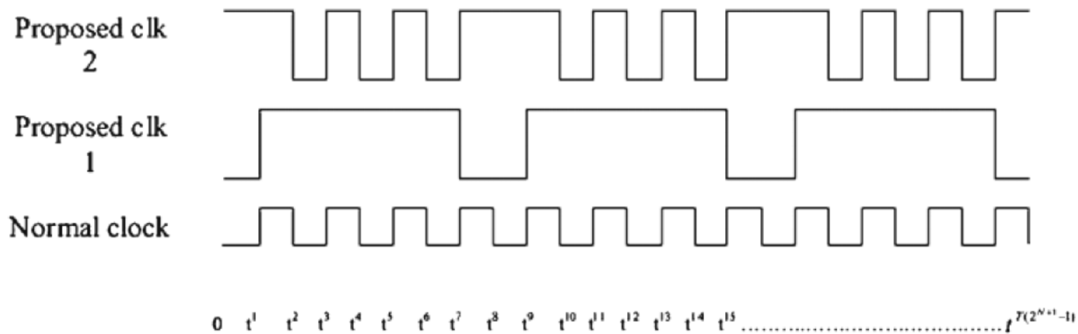

Figure 4: Comparison of Clock splitting Logic with Normal Clock

hamming decoding technique for stcu at fault detection.we are implementing separate LFSR for the purpose of generating the random data bits for storing of the data , here we are using the 4 bit LFSR circuit for the purpose of generating the random data bits. Andwe are applying the hamming encoder for encoding those bits into parity added format. We are adding 3 parity bits to the 4 bit data. And then we are storing those data in the RAM memory cell. While retrieving the data for ram memory cell we are randomly adding the stuck at fault model for creating the random error in stored data. This can be done by the changing any bit value from “1” to “0” or else “0” to “1” for that we are adding the ring counter module and XOR the last out value into new one. This module can create a random stuck at fault in stored data. Finally we are decoding those retrieving data using hamming decoding technique while decoding we are removing the parity which we are added earlier by using that we can findout the stuck at fault present in the memory cells. Thedetailed working of the stuck at fault detection shown in the figure(5) below.

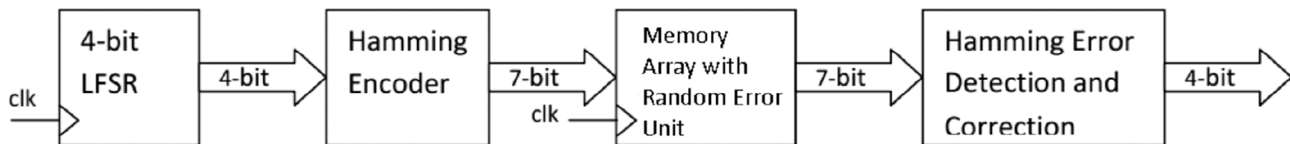

Figure 5: Proposed LFSR Data Generator with Hamming based Stuck at Fault Detector

Performance Discussion

The proposed scheme was implemented and simulated using the Xilinx 14.2 tool and results obtained clearly showing that the overall power was reduced when compare to the conventional switching schemes and also the proposed hamming distance based having the best fault coverage ratio against the stuck at faults in memory circuits.The following figure (6) shows the overall Area utilized by the proposed switching logic and the proposed hamming distance based fault coverage scheme. Theseresults showing that the overall Area utilized by the proposed Logic was having very low area when compare to the existing systems.

And the below figure(7) shows that the overall power usage of the proposed clock spilling logic and hamming distance based stuck fault detection scheme.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	3	4800	0%
Number of Slice LUTs	4	2400	0%
Number of fully used LUT-FF pairs	0	7	0%
Number of bonded IOBs	4	102	3%
Number of BUFG/BUFGCTRLs	1	16	6%

Figure 6: Overall Area ofProposed system having Nearly Zero percentage Area Usage

These results shows that power dissipation of the proposed scheme was 0.571W that is extremely reduced compare to previous conventional schemes.

Name	Power (W)	Used	Total Available	Utilization (%)
Clocks	0.123	1	---	---
Logic	0.003	33	21504	0.2
Signals	0.018	44	---	---
IOs	0.002	4	450	0.9
DCMs	0.000	0	8	0.0
Total Quiescent Power	**0.425**			
Total Dynamic Power	**0.146**			
Total Power	**0.571**			

Figure 7: Overall Power of Proposed system having nearly 0.5W Power Usage

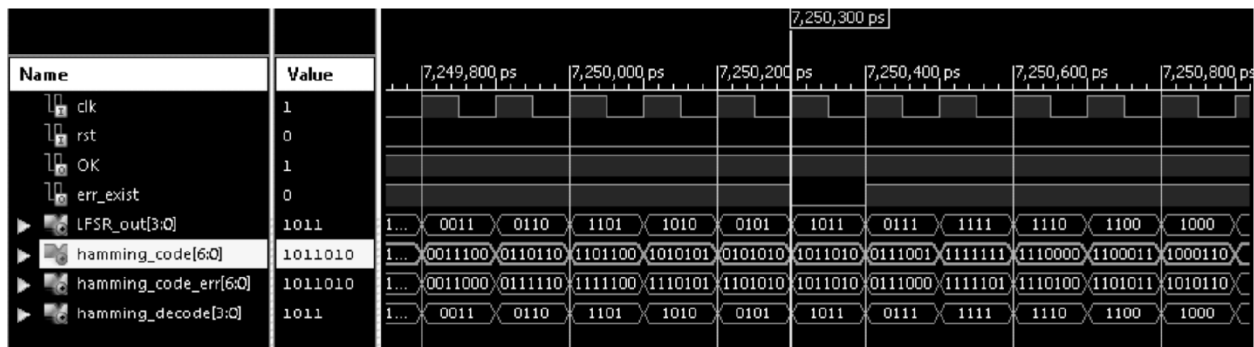

Figure 8: Overall Simulation Results of Proposed LFSR with Hamming Encoder with High Stuck Fault Coverage

CONCLUSION

We have implemented this as research methodology, to design a power efficient random address generator for testing a Memory and Efficient Stuck at fault detection scheme using hamming distance based encoder design with extremely lower power with the help of clock splitting logic was implemented. The Overall area utilization of the proposed scheme was nearly 50% minimum compare to conventional schemes. Also overall power consumption of our proposed clock splitting logic was nearly 92 % reduced. The suggested scheme nearly having the 98 % of fault coverage against the both the Stuck at faults presents in the Memory circuits. With the help of these optimized results we will employ this proposed LFSR address generator and Hamming Distance based Stuck at Fault detector at low power testing applications with high fault coverage Purpose.

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