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Design Enhanced Hynoc Router for Efficient On-Chip Communication

V. A. Saravanan* and K. Paramasivam**

Abstract : Network-on-Chip (NoC) gives a proficient communication for the computing energy on on-chip applications. In this paper, the hybrid router structure bandwidth resourceful routing, runtime disputation, low power and low latency in introduced in order to give a very good communication. The new hybrid methodology is known as Enhanced HyNoC (E-HyNoC) and it grouping the merits of source routing and distributed routing in developing adaptive routing algorithm. There are three source routing algorithms are decided to use the particular process at the same time as the Dynamic XYZ (DyXYZ) methodology is used as the adaptive routing algorithm. This method reduces the latency with large scalability and it consumes the minimum power. In a hybrid methodology, the E-HyNoC improve the hardware overhead of distributed routing methodologies and huge amount of data overhead of source routing at a constant price of data redundancy. Therefore, the unique algorithm using only merits of the method. Finally, the result of the simulation process proves that the E-HyNoC enhances the performance in better communication with low latency and low power consumption than the other algorithms.

Keywords : Network-on-Chip, Dynamic XYZ, source routing, distributed routing, adaptive routing.

1. INTRODUCTION

The entire components of a computer are integrated by using a System on Chip (SoC) or extra electronic systems into a single integrated circuit. In this system hold digital, combined signal, analog and a lot of radio frequency functions on the entire single chip substrate. Suppose in the specified application there is no possible to create a SoC means than the System in Package (SiP) is used a choice and it has a lot of chips in a single package. On the other hand, in the VLSI designs, the entire price is higher for one big chip than for the similar process and it is distributed in the excess of more number of little chips, for the reason that of lower yields and higher design price [1]. A lot of standards and the requirement for very high performance and reliability thus motivated the implementation of interconnection networks for multi-computers.

In System on Chip (SoC), the number of IP modules are increases, bus based interconnection structure may protect from these systems to meet the performance needed by more number of applications. In the system with parallel communication buses may not give the needed bandwidth, power consumption and latency. A result for such as communication bottleneck is the use of an embedded switching network and it known as Network-on- Chip (NoC) and it is interconnected with the IP modules in SoCs. NoCs design is occupy the bigger space when compared to a bus based design, because the various routing and negotiation methods can be developed and also in the various environment of the communication transportations. The scalability of SoCs is enhanced by using the NoCs method as well as the power efficiency of difficult SoCs differentiated to other methodology. Therefore, the NoC method is the popular method for the communication within the VLSI systems is developed on a single silicon chip. Another

* Assistant Professor, ECE department, A.S.L Paul College of Engineering and Technology, Coimbatore.

** Professor, ECE department, Kumaraguru College of Technology, Coimbatore.

name of Noc method is layered stack methodology to the design of the on chip inter core communication. The modules in the NoC system like memories, processor core and IP blocks share the data by using a public transportation in the sub system for the data about traffic. A NoC method is specifically created from the multiple point to point data links and it is interconnected by switched or routers like that information can be transferred from source module to termination module in the excess of more number of links by creating routing choices at the switched or routers.

A NoC method is same as the present telecommunication network by using digital bit packet switching in the excess of multiplex links. Even if it is implemented for the required communication requirements of multi-computers, NoC is a suitable method to grip the troubles by changing the global wires and on-chip buses with packet routing networks. The merits of NoCs are decreases the electromagnetic effects by proposing structured interconnect among the layouts with a better scalability and usage of network. The merits of suitable NoCs are that since of their common speed, power, noise, reliability and so on. A NoC can give the division among the computation and communication; the modularity and IP supported the concept of reused through the standard interface, and it manage the synchronization trouble and it is used to test the system platform, and therefore it enhances the engineering productivity [2].

The NoCs design depends on the topology method; the routing protocol and the flow control have been developed. With the fundamental topology as the roadmap, the routing protocol calculated the original route taken by a packet. The routing protocol is significantly important as it impacts of the entire network metrics namely latency, throughput, and power dissipation ad reliability. Latency means the hop count is affected directly by the route. A congestion method is based on the capability of the routing protocol to manage the load is known as throughput. The entire hop is incur the route energy overhead is known as power dissipation. At last reliability means the routing protocol required to select the proper route to avoid the error. There are two types of routing algorithms. One is deterministic and another one is adaptive. The deterministic methodology routes the packets in the way calculated by the source based on the termination address. The adaptive methods routes the packets based on the level of the network such as available buffer space and conditions of the congestion and so on.

A routing algorithm is mainly balance among the inconsistent aim of giving low latency on local traffic and giving high throughput on adversarial traffic. In the most traffic patterns, the congestion routers are not able to balance the load. Since, it does not concentrate the status of the congestion in the ports. In most of congestion routing rules [3], [4] and [5] have been introduced that route the packets suitable manner all the way through the low distance paths. Even if, the non-minimal routing has a difficult development and it can worked to analyze the performance of the NoCs while the network is congested. The NoC method has been only developed for the result for both the communication obligations and complexity of global interconnections. So in this proposed work, the new result for the router trouble in NoC is implemented and it grouping the source routing and distributed routing by the side of with the suitable routing methodology for highly efficient router structure. The proposed system named as E-HyNoC combines the adaptive routing algorithm DyXYZ along with the distributed routing algorithm and the source routing algorithms for enhanced performance. This approach also reduces the latency and power consumption considerably.

2. RELATED WORK

Different scientist developed the previous NoC routers are at a standstill it is difficult to sustain the communication between the different modules within a system with a lot of different workloads and constraints alternation. In the previous model description is based on the low power consumption methodology and also the current environment in various runtime.

The NoC router [6] is based on accumulate and forward methods and the loop back system. The new NoC router is based on the novel fault detection methods and it is appropriate for the dynamic NoC, while the number and location of processor components or error blocks to be different for the period of runtime. It preserves the throughput, the data packet latency and the network load [7].

The 8 port router for NoC using Verilog HDL model is introduced by Ranjitha et al. [8]. In this case, the buffering method is to store and forward process. By using the control logic the random choices can be created. Therefore the communication is implemented among the input and output ports. From the data input the data are taking out by using the data registers and it is based on the state and status of the control signals. And the data is latched and it is sent to in the method of First in First out (FIFO) to store in the database. The error signal is created when the packet parity is not same to the manipulated parity. This enhances the routing performance for on-chip communication.

A low-latency wormhole router for packet switched NoC model, for Field Programmable Gate Array (FPGA) is introduced in [9]. This model is designed to be scalable at system level to entirely develop in the features and the corresponding constraints of FPGA based model to a certain extent on the ASIC methodology. It reaches a low packet broadcast latency of only the two cycles per hop as well as the router pipeline delay and the link traversal delay. This method is also configured in different network topologies together with 1-D, 2-D, and 3-D. there are two parameters are used to achieve the goal that are 1) high scalability, it is mostly used in the router radix with respect to the topologies and 2) optimized pipeline.

Guoyue Jiang et al [10] developed an On Chip Networks model using the Hybrid methodology. The regular physical channel are sharing process is permitted by the multiple virtual circuit switched (VCS) connections. The scientist used the traffic workload algorithm and it reaches a goal up to 20.3% latency reduction and 33.2% power saving can be acquired while distinguished with the baseline NoC system. The Aging Aware Adaptive Routing Algorithm is introduced by Dean Michael Ancajas *et al*. [11] for NoC system. This algorithm is decrease the power consumption overheads caused owing to the aging degradation as well as it decrease the stress experience by heavily utilized routers and links. The researchers achieve a goal up to 13% and 12.17% average overhead reduction in network latency and delay of the power product per flit, a performance is increased to 10.4% and a mean time to failure is enhanced to 60% using aging-aware routing algorithm.

The Unified Scheduling and Mapping algorithm is used by the Ou He *et al*. [12] for the network on chip router. In the proposed method the Heuristic methodology was integrated and it is speed up the network on chip. The scientist reaches a goal the enhancement of the execution time with lower energy. The NoC model is designed by Lee et al. [13] for the data transfer by using the virtual channels can eliminate the trouble of data loss and deadlock. The Smart Power-Saving (SPS) structural design was implemented for low power consumption and low area in virtual channels.

The Network on Chip (NoC) developed by the Rajesh Nema *et al*. [14] for the communication subsystem among the intelligent property (IP) cores in a system on chip (SoC). The NoC Router Architecture is introduced by Minakshi M. Wanjari *et al*. [15] and it acts as the communication backbone in NoC. The fundamental channel buffer used by this router and it give the good channel utilization and also this router has low latency and needed low area compared to the other routers. The permanent priority trendsetter can be used for a small number of customers and there was no limit to the low priority request should wait in anticipation of it receive a contribution so this can affect the network performance.

Soteriou *et al*. [16] employed on router for NoC to improve the throughput of the network. The result of this process is 94% of throughput except power consumption is greater than before by the factor of 1.28. The buffer less flow control is focused by the Lin *et al*. [17] for lightly loaded networks. On the other hand, the buffer less flow control has a great effect on communication latency. The entire channel controller had two extra responsibilities: the channel directions are dynamically configuring than the typical NoC router structural design was obtained owing to double crossbar propose and control logic. From the literature, it can be seen that many researchers focused on improving on-chip performance through novel ideas. However still there are certain issues which seem to be never ending and the proposed method in this paper aims to improve the performance than its predecessors.

3. PROPOSED METHODOLOGY

The Hybrid router model on the NoC is described in this segment. In common, by using the deterministic or adaptive way the routing algorithm can be completed. The more number of scientists observed on implementing the adaptive routing for NoC as the error and it is removed and multiple best options are obtainable for routing process. Larger networks have multifaceted topologies that can modify quickly, building the physical structure of routing tables impracticable. To overcome this trouble the Adaptive routing is creating the routing tables robotically, based on the data conceded by routing protocols, and it permitting the network to proceed almost independent in skip the network failures and obstruction. Adaptive routing has been working in multichip interconnection networks as resources to recover network performance and to endure network link or router failures [4], [18]. Regardless of the extra accomplishment difficulty, adaptive routing is tempting for up-and-coming NoCs with a growing number of associated components.

Developing routers has an important collision on the communication competence. Routing algorithm can be developed as source or disseminated routing. In source routing method the entire pathway from sender to receiver is recalculated at source router and manipulating the accurate router-to-router packet information in the header. This data guide the packets to travel all the way through the middle routers in the direction of their target node and it has sensible overhead for little networks. The packet header required to hold the entire k units of routing information for a network with a diameter of k. this process becomes perceptible as the network size increases and it is a major trouble for on-chip routing. On the other hand, the routing choices are created by the entire routers in distributed routing technique, in which the packet header needed to hold the only one address of the destination node. This address is distinguished from the every middle router to select the proper channel to forward the packet. The router difficulty of the concluding method is higher than the previous one even if it imposes scalable information redundancy [19]. The TagNoC has been implemented in [20], as a hybrid system grouping the source and distributed routing, for decreasing the information overhead, latency and consumption of the power. On the hand, the adaptive routing algorithm is not suitable for the TagNoC method because there are no adaptive routing elements available in this method. Simply partial adaptive routing like Odd-Even (OE) model [21] is probable owing to permanent and pre-defined environment. For this reason, a new technique observed on totaling the adaptive routing elements in the hybrid model and the entire adaptive routing algorithm is developed. The new method is known as E-HyNoC and it grouping the source and distributed routing protocol with adaptive routing methodology for the development of NoC router structural design.

Adaptive Routing algorithms

In the traffic pattern the deterministic routing algorithms is efficiently performed at the same time as there are very incompetent beneath the non-uniform traffic. On the other hand, the adaptive routing algorithms, the packet is not limited to a single path while the information is transferred from a source to the destination node. In that way, this algorithm reduces the possibility of routing packets all the way through the congested area. More number of partially and entirely adaptive routing algorithms is proposed in two dimensional networks like Odd-Even [21] and DyXY [22]. A lot of them assume local traffic circumstance in the routing choice and the entire router analyses the congestion circumstances of its individual and nearest routers to select an output channel. This combination of algorithms could enhance the performance considerably as distinguished to dimension command routing owing to the distribution of packets in the excess of the network. On the other hand, the routing choice based on local congestion data may guide to a disturbed distribution of traffic load. Other than this algorithm namely CATRA [23] and HARAQ [24] get the data from the global information into decreasing the possibility to creating fault choices. On the other hand, despite the consequences of the imposed difficulty and in this specified domain overhead, giving the global information is difficult. In addition, this algorithm is based on the global congestion information enhances the performance in the excess of the previous technique based on local congestion information.

This performance increase is at the price of a big area overhead, an additional multifaceted routing unit, and the required for congestion detection and proliferation method. There are a small number of partially adaptive methods obtainable in 3D NoCs like MAR [25].

The difficulties of the trouble is reduced by applied in the distributed algorithms at the same time as the particular specified overhead can be decreased by source routing. Therefore, the present E-HyNoC structural design enhances the routing performance than the individual algorithms. The two dimensional Planer Adaptive Routing Algorithm [26] is just appropriate for two-dimensional and for this reason the DyXYZ [27] is used as the adaptive routing algorithm in the planned E-HyNoC.

DyXYZ algorithm

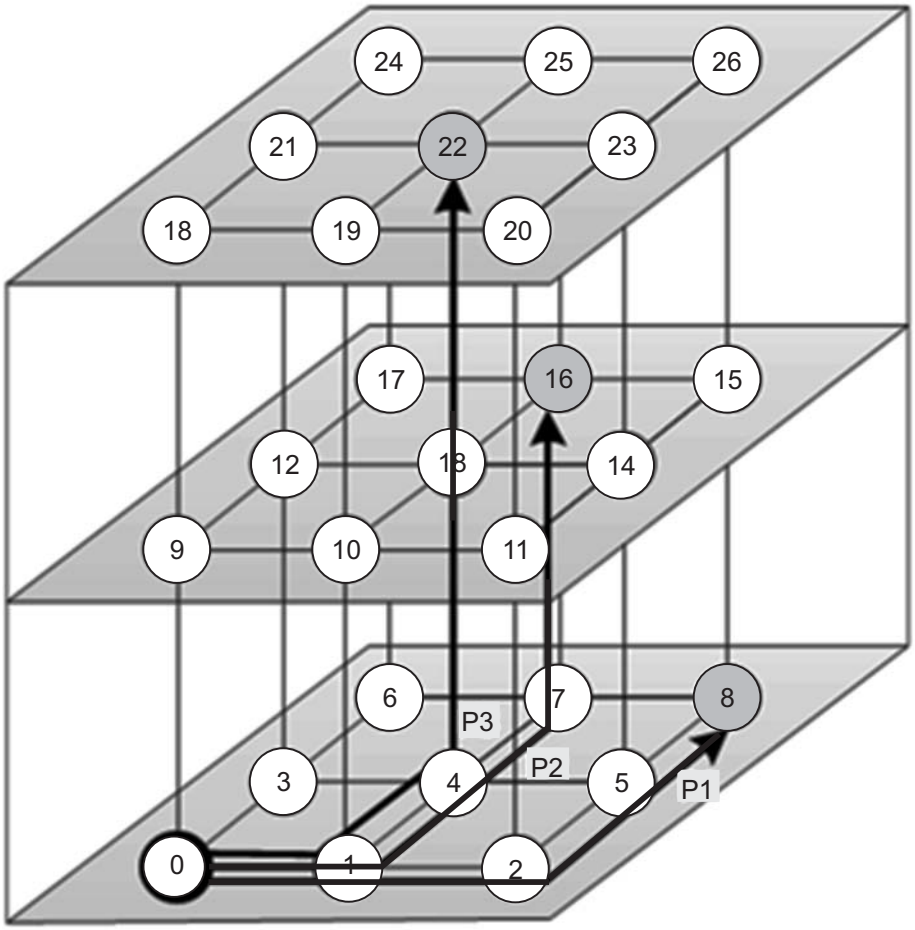

Figure 1: Dynamic XYZ algorithm

Generally there are four virtual channels are used in the adaptive routing for the entire dimensions. On the other hand, the number of virtual channels can be decreased to two virtual channels by the side of a one of dimensions, known as this technique Dynamic XYZ (DyXYZ). Similarly, the entire network can be separated into two important sub networks, every one having four sub networks. Partitioning the network into two segments can be achieved by the side of one dimension, decreasing the number of virtual channels from four to two for that dimensions. Because, the two important sub networks are split, the remaining networks are deadlock free. However, the sub networks within every important sub networks used various sets of virtual channels on the two extra dimensions. Consequently, the eight sub-networks are put out of articulation and the network is deadlock complimentary. The packets can be routed beside X, Y or Z dimension By using DyXYZ at the entire middle node without generating some other cycles. The entire choices for routing for DyXYZ routing algorithm using two virtual channels in the Z dimension and four virtual channels in the X and Y dimensions. This algorithm is confirmed to be

deadlock complimentary by using 4, 4, and 2 virtual channels by the side of the X, Y, and Z dimensions, correspondingly. The fundamental XYZ structural design which is dynamically performed to form DyXYZ is illustrated in figure 1.

Distributed Routing Algorithms

In the previous method the distributed routing algorithm has been used, however it needed a multifaceted circuit and it does not scale proportionally as the number of cores raised. Twist Model routing method based on wormhole switching system gives deadlock and live-lock independence in the mesh topology [28] and it is the well known routing methods utilized in NoC structural design. There are three popular turn methods namely Negative-First (NF), West-First (WF), and North-Last (NL) [19] with six acceptable turns. The XY routing algorithm is a well known dimension organize routing algorithm in which four turns are avoided in order to avert deadlocks. In the entire turn model is supported by the TagNoc method and dimension arrange routing algorithms including XY, NF, WF and NL.

Source Routing Algorithms

Source routing will offer inadequate path adaptively in the occurrence of faulty associations or congestion in the network [29]. There are three source routing techniques are implemented in E-HyNoC method as the baseline routing method namely None Encoded Address (NEA), Encoded Address (EA) and Optimized Encoded Address (OEA).

None Encoded Address (NEA)

NEA method is measured as the especially primary source routing methodology. In this technique, the routing process will be achieved in the source router proceeding to injecting a packet into the network. The header flit holds the coordinated of the entire intermediate routers from source in the direction of its termination as a replacement for the coordinates of the termination node. The routing choice is removed in the middle routers outcomes in low latency and power consumption, at the price of increasing header flit size. On the other hand, NEA is not scalable and imposes a huge amount of information overhead. Header flit size for this technique depends on the network size because the important number of bits for comparing the entire node is a process of the number of routers per every dimension of the network.

Encoded Address (EA)

In the entire middle router output port is represented by only two bits to support the entire remaining ports apart from the incoming input port in a 5-port NoC router. The two bits per hops in the header flit are given by Network Interface (NI) element. The EA approach use a programming and the entire incoming flits has four potential options to select its output port channel and it documented by 0, 90, 180, and 270 degree turns, the local port is forever recognized by 0 degree. The remaining output ports are calculated based on the counterclockwise relative rotation in order to the location of the input channel. In this case, every port receives an incoming header flit; the north output port will be recognized by 90 degree. The EA routing methodology required two bits for every middle node regardless of the size of the network, at the same time as in NEA approach the header size depends on the size of the network. The size of the header flits in EA routing it still biggest by imposing two bits for every middle node.

Optimized Encoded Address (OEA)

The Optimized Encoded Address (OLE) method is the third source routing methodology and in this case the header flits are compacted. In the EA methodology, a header flit transferred all the way through the entire middle routers in one dimension and after that it transferred to the other dimension to reach its receiver node. The basic thought of OEA methodology is to use the similar encoding methodology as EA approach in anticipation of the header alterations its dimension on its individual path identified in the direction of receiver node. After that the header flits has the two choices, selecting the local port or

travelled in the similar directions. In this method, one bit per hop is worked to find the way the header in the direction of destination, just the once the header turns to the additional dimension. For the reason that, the belongings of the dimension arrange routing algorithms in which only one turn is allowed. The OEA algorithm improves the extra overhead of the EA method by 25%. And also saves additional switching power by having just one transition from "0" to "1" in the header flit subsequent to the header turns to be in motion frontward in the second dimension. These algorithms are combined together to develop the proposed E-HyNoC architecture.

E-HyNoC Architecture

In figure 2 the structural design of E-HyNoC is illustrated. It is collected of XNOR gate comparison circuit, multiplexer and a mechanical switch circuit. This approach need an insignificant logic circuit within the NI generate the two Tag bits. The header flit is established once in the input buffer, the X(Y) portion of the destination address of the header flit is distinguished with the present router using XNOR gates. The integration of DyXYZ is demonstrated in the figure 2.

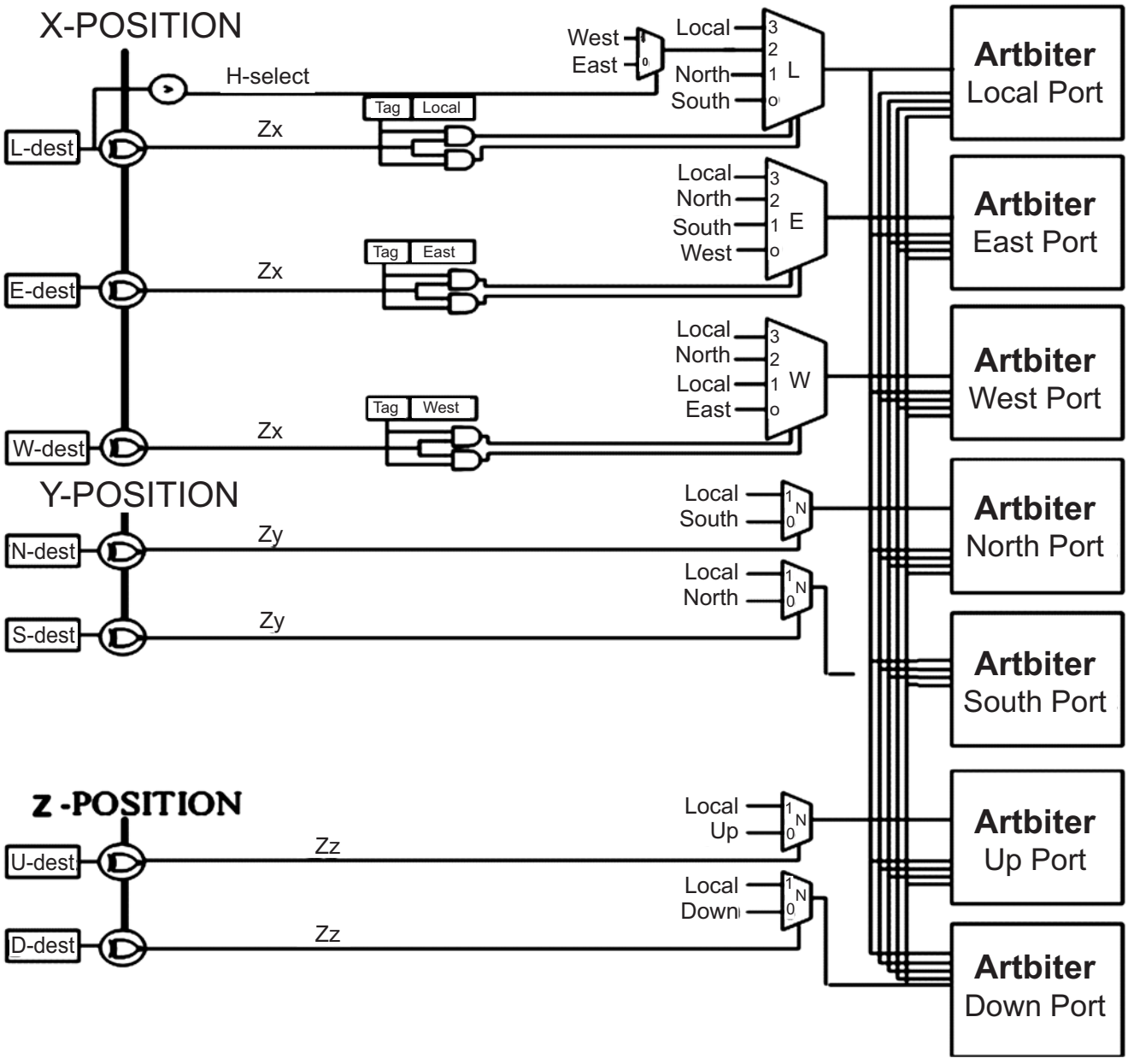

Figure 2: Proposed E-HyNoC architecture

The E-HyNoC design is completely based on the basic NoC architecture. The implementation of NoC is carried out and then the incorporation of DyXYZ is performed. This method needs a negligible logic circuit inside the NI to generate the two *Tag* bits. Once the header has settled in the input buffer, X(Y) portion of destination address of the header flit is compared with the coordinates of the current router using XNOR gates. The output of comparison gates are *Zx* and *Zy* are used to determine if the flit has reached its expected horizontal or vertical coordinates, respectively. If the *Zx* output of XNOR circuit for the X-POSITION is '0', then the packet traverses with 180◦ rotation. It means that if the input port is west (south) bound, the output port will be east (north) bound or vice-versa. The *Zx* will be '1' once header reaches the router with the same X dimension of its destination address. Subsequently, *Tag* bits are examined to choose the appropriate direction based on the values. *Tag* bits will not be considered after the *Zy* is equal to '1'. This method is flexible to support all the turn model based routing algorithms. The header of the packet is provided in the NI of the core and is forwarded to the connected router to navigate the whole packet towards the destination. A *Tag* is computed, just one time regardless of the network size, and appended to the coordinates of the destination router in the header of the packet. Thus the NoC can be implemented. Along with this NoC architecture, the DyXYZ concept is incorporated. By using DyXYZ, packets can be routed along X, Y or Z dimension at each intermediate node without creating any cycles. Thus the power consumption can be reduced along with reduction in latency.

4. PERFORMANCE ANALYSIS

In this section, the E-HyNoC is simulated in Xilinx environment. The HDL compilation is followed by the design hierarchy analysis. Then the HDL synthesis and advanced HDL synthesis are carried out before low level synthesis to provide the device utilization and partition resource analysis. Figure 3 shows the simulated design of the existing NoC without the DyXYZ.

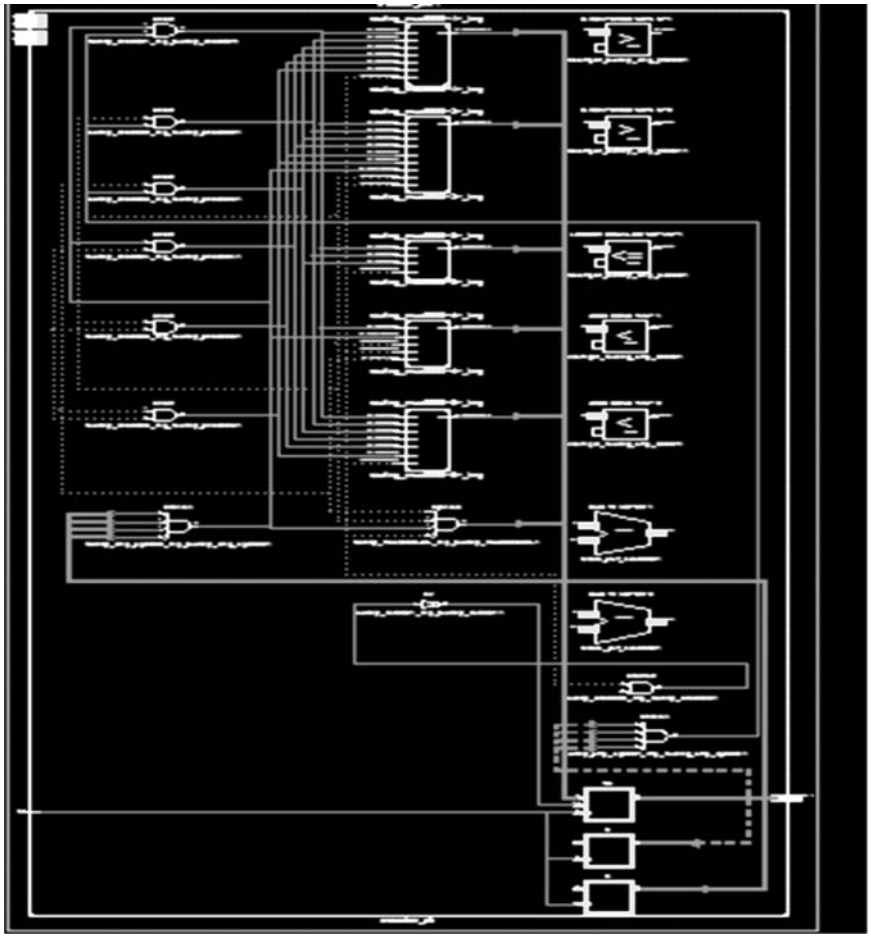

Figure 3: RTL design of NoC without DyNoC

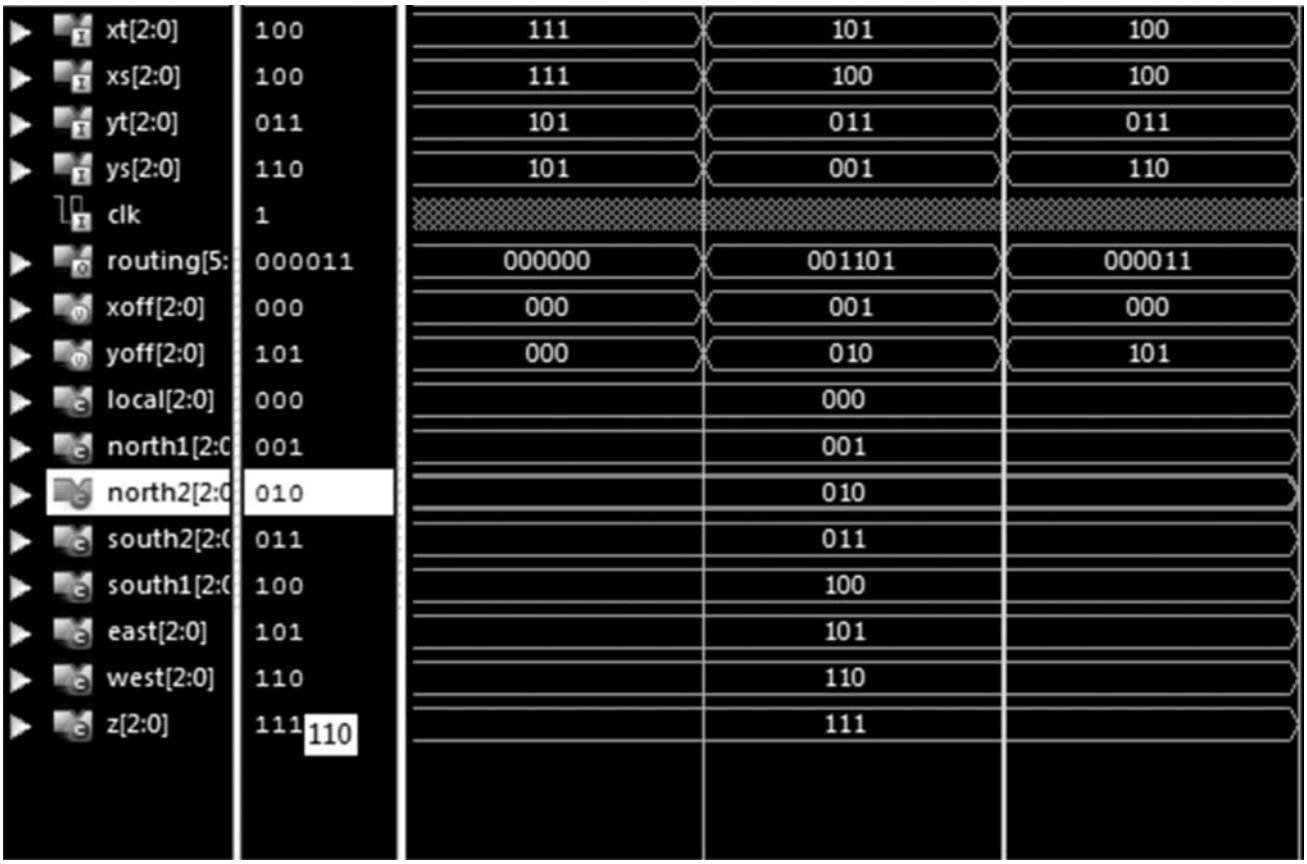

Figure 4: Output of existing NoC design

The output of this design is shown in Figure 4. It shows that the output without DyXYZ has higher latency and power consumption when compared with that of the proposed model. The synthesis report shows that the Real time for completion is 7 seconds while the total CPU time for completion is 6.75 seconds. Similarly the total memory usage is 198640 kilobytes consuming high power.

Table 1

Comparison based on Final Synthesis Report

Design Statistics & Cell Usage	*NoC design*	*E-HyNoC*
Number of IOS	19	33
Number of BELS	17	16
LUT2	2	4
LUT3	4	3
LUT3_D	1	1
LUT4	8	6
LUT4_D	1	2
Flip-flops/Latches	12	18
FD	4	18
FDE	6	–
FDR	2	–
Clock buffers	1	1
BUFGP	1	1
IO Buffers	18	32
IBUF	12	23
OBUF	6	9

Table 1 shows the comparison of the existing and proposed methods based on the final synthesis report of the simulation. Table 2 shows the comparison of existing and proposed methods in terms of time and memory.

Table 2

NoC VS E-HyNoC

Parameters	*NoC design*	*E-HyNoC*
REAL time	7.0s	3.00s
CPU time	6.75s	3.36s
Delay	2.739ns	2.964ns
Net Delay IBUF	0.532	0.509
Net Delay LUT2	0.387	0.303
Input arrival time	3.517ns	3.710ns
Maximum Frequency	337.388MHz	337.388MHz
Total memory usage	249688 kB	198640 kB

From the tables it can be found that the proposed E-HyNoC structure provides better performance. The RTL design of the proposed E-HyNoC architecture which includes the concept of DyXYZ routing is shown in Figure 5.

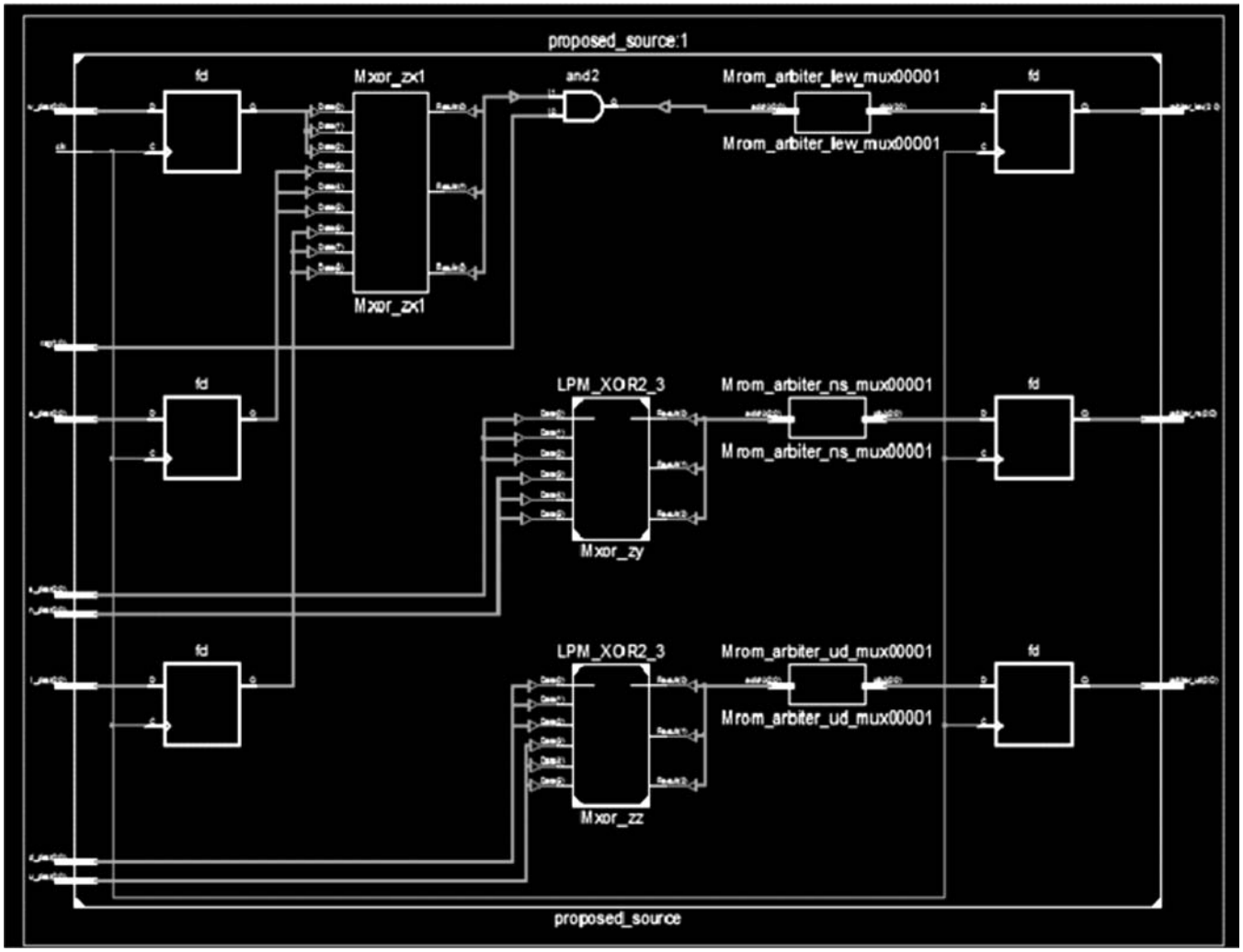

Figure 5: RTL design of E-HyNoC

The output of the proposed E-HyNoC design is shown in Figure 6.

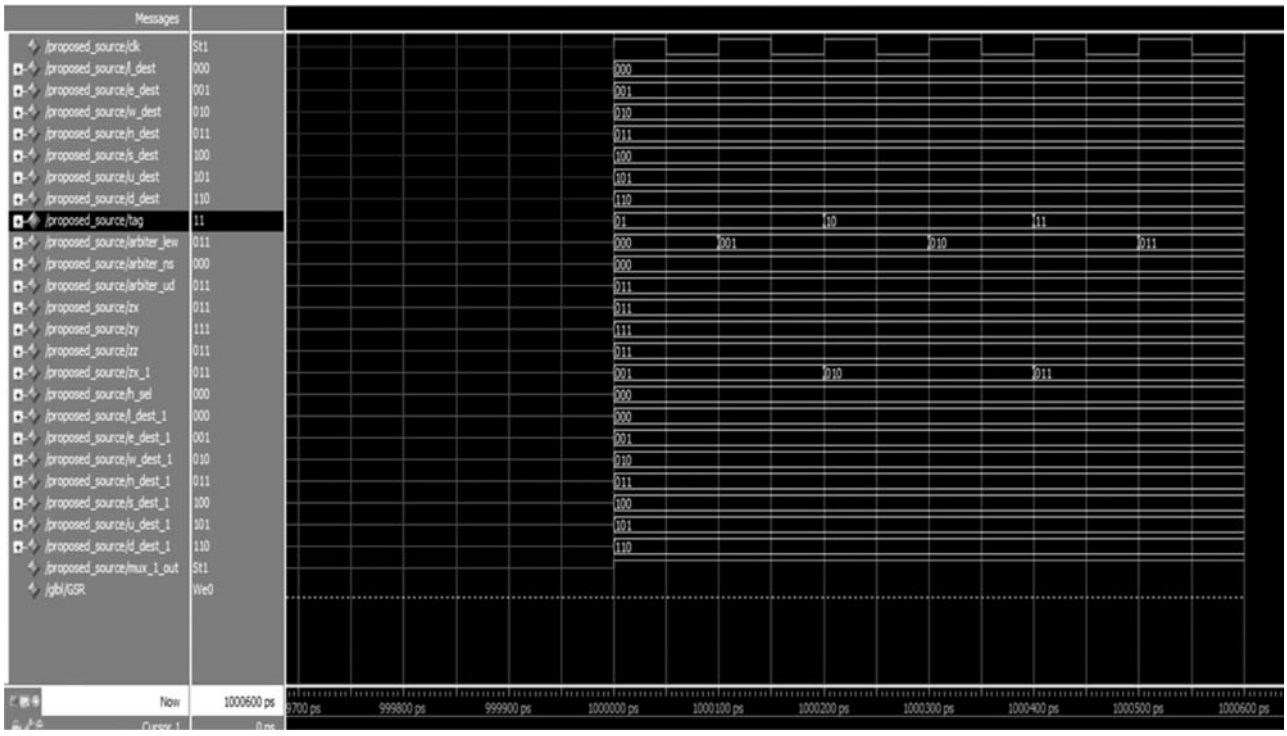

Figure 6: Output of E-HyNoC

From the output of E-HyNoC, it can be seen that the performance is highly improved in E-HyNoC. The synthesis report shows that the total Real time for completion is 3 seconds while the total CPU time for completion is 3.36 seconds. Thus the latency is low in E-HyNoC than the existing NoC. The Total memory usage is 249688 kilobytes which is significantly low than the existing NoC design; thus reducing the total power consumption. Therefore it is proved that the proposed E-HyNoC algorithm improves the communication with minimal delay and low power consumption.

5. CONCLUSION

This paper presents a hybrid router structure called E-HyNoC for bandwidth resourceful routing, runtime disputation, low power and low latency. This proposed E-HyNoC combines the benefits of the source routing and distributed routing along with the adaptive routing algorithm. From extensive research it was found that the DyXYZ routing algorithm is much simpler and superior than the other adaptive routing schemes. Hence E-HyNoC utilizes DyXYZ and reduces the latency with large scalability and it consumes minimum power. The result of the simulation process concludes that the E-HyNoC gives efficient performance in better communication with low latency and low power consumption than the existing NoC design.

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