

Implementation of Low-Power CMOS Voltage to Current Converters

Raisa Thomas* and N. Saraswathi**

ABSTRACT

The paper presents compact CMOS voltage-to-current converters based on OTA/common-source configurations, which attain rail-to-rail input-output operation. Voltage to Current (V-I) converters is used at the input stage of many analog and mixed signal designs, such as integrators, multipliers, continuous-time filters, data converters, high-performance sensor interfaces, or variable gain amplifiers. Measurement results for 2.4- mV 0.09 μ m CMOS implementations confirm rail-to-rail operation with bandwidth up to 2.308 MHz and power consumption below 596nW, which make these basic building blocks suitable for portable applications.

Index Terms: Converters, CMOS analog integrated circuits Low power design, Figure of merit.

1. INTRODUCTION

Voltage to Current converters are fundamental building blocks in many analog and mixed signal designs, such as multipliers, continuous-time filters, data converters, high-performance sensor interfaces, or variable gain amplifiers [1][2]. In these applications, the complete system performance depends mainly on the functioning of the V-I sub circuits. This leads to the need for a time, temperature and supply voltage-independent transconductance, with a highly linear range and a suitable bandwidth.

The need for portable applications is a regularly evolving industry, and as a result, there is a huge demand for low-voltage low-power operation circuits. Hence, these are two necessary requirements for the V-I converter:[3] low-voltage, to be powered with low form factor batteries; and low-power consumption, to expand battery life.

The fondness for attaining rail-to-rail highly linear transconductors is the use of passive resistors for performing the V-I conversion. Recently published linear rail-to-rail V-I converters was made by using passive resistors at the input terminals tied to a virtual ground. On the other hand, these V-I converters always shows a rather small input impedance, as a compromise between area consumption and resistor value. As a result, an auxiliary rail-to-rail input buffer must be added to correctly process the signals, thus increasing the power consumption and the area [4]-[6].

Thus, the idea of this work is to the design of V-I converters with high linearity over the complete input voltage range, which is are not easy features to achieve when low supply voltage and low power consumption are required.

2. CONVENTIONAL VOLTAGE TO CURRENT CONVERTER

In instrumentation circuitry, DC signals are usually used as analog representations of physical measurements such as temperature, pressure, flow, weight, and motion. The current signals used to be precisely equal in magnitude throughout the series circuit loop carrying current from the source to the load, but the volt age

* M. Tech VLSI Design SRM University, Kattankulathur, Email: Raisat316@gmail.com

** ECE Dept., Asst. Professor (S.G) SRM University, Kattankulathur, Email: saraswathy.n@ktr.srmuniv.ac.in

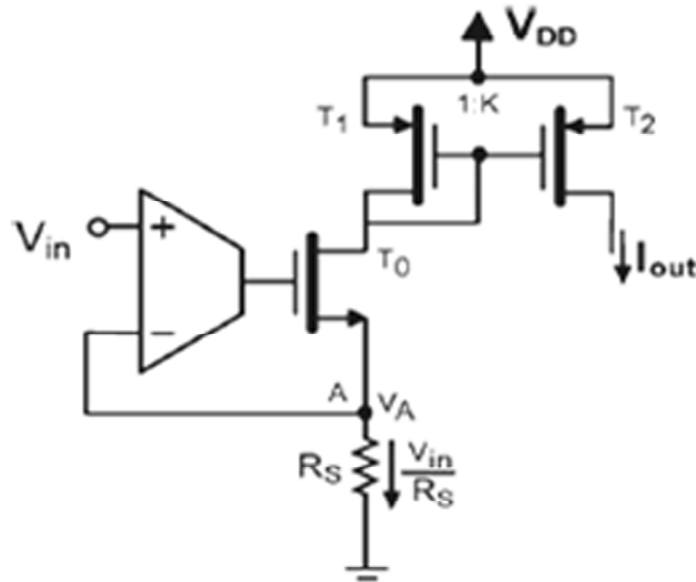


Figure 1: Schematic of the Conventional Voltage to Current Converter

signals in a parallel circuit may vary from one end to the other due to resistive wire losses. Additionally, current-sensing instruments typically have low impedances (whereas the voltage-sensing instruments have high impedances), that gives the current-sensing instruments large electrical noise immunity.

In turn to use current as an analog representation of a physical quantity, we need to have some way of generating a precise amount of current within the signal circuit. Still how do we generate a precise current signal when we might not know the resistance of the loop. [8] The way is to use an amplifier designed to clasp current to a agreed value, applying as much or as little voltage that is enough to the load circuit to keep up that value. Such an amplifier executes the function of a current source. Even though this approach provides a gain and a wide input signal range, the linearity of the circuit is typically low.

As the first choice for attaining rail-to-rail highly linear transconductors is the use of passive resistors for performing the V-I conversion. On the other hand, these V-I converters always show a rather small input impedance, as a compromise between area consumption and resistor value. As a result, an auxiliary rail-to-rail input buffer must be included for properly processing the signals, [9][10] thus incrementing the power consumption and the area.

On the other hand, the conventional V-I converter with an operational transconductance amplifier (OTA) driving an nMOS and a grounded linear resistor in a negative feedback loop is highly linear while offers a high impedance input node which affect the converter performance.

Therefore, this paper presents three CMOS rail-to-rail V-I converters based on the highly linear OTA/common source V-I converter approach, with rail-to-rail and high linearity over the complete input voltage swing and also have a reduced area and power consumption.

3. PROPOSED VOLTAGE TO CURRENT CONVERTERS

3.1. Feed Forward Voltage Attenuation Voltage to Current Converter

The FFVA V-I converter, shown in fig. 2, is the simplest design based on the above mentioned circuit principle. It primarily consists of a buffered voltage divider before the V-I converter. As a result, even though not a new theoretical topology, it will be considered as the starting point of the analysis of attenuated converters. In this design, to attenuate the input voltage, a rail-to-rail input voltage divider is kept before the main V-I converter. This input attenuator is made using an auxiliary OTA loaded with a resistive voltage

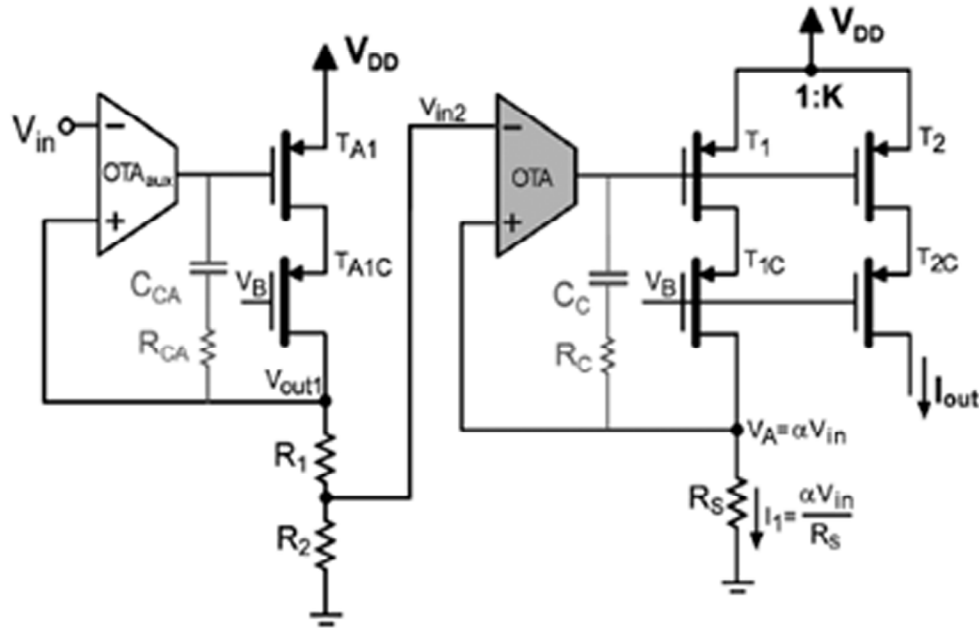


Figure 2: Schematic of Feedforward voltage attenuation V-I converter

divider formed by linear resistors R_1 and R_2 . Therefore, the FFVA converter on the whole have two cascaded improved V-I converters.

Foremost, the input voltage V_{in} is buffered to V_{out1} by the OTA aux – T_{A1} - T_{A1C} voltage follower with rail-to-rail input-output voltage operation. Cascode configuration is used to have a modular circuit, because cascode transistors will be used in the second stage to improve the current copy and to increase the output resistance. The buffered voltage V_{out1} is attenuated to $V_{in2} = \alpha V_{out1}$ through the voltage divider formed by resistors R_1 and R_2 , where $\alpha = R_2/(R_1+R_2)$. This attenuated voltage is given as input to the main V-I converter formed by OTA and transistors T_1 and T_{1C} . Thus, the voltage is buffered to $V_A = V_{in2} = \alpha V_{out1} = \alpha V_{in}$. Then, the generated current $I_1 = \alpha V_{in}/R_S$ is driven by $T_1 - T_{1C}$.

Therefore, the output current showing a linear transfer characteristic dependent on the attenuation factor K , the scaling factor and the resistor R_S .

3.2. Feedback Voltage Attenuation Voltage to Current Converter

The FBVA V-I converter approach is shown in Fig. 3. The voltage reduction across resistor R_S is carried out by keeping an attenuator between the OTA non-inverting input (at a voltage due to negative feedback) and node A. The attenuator is implemented with a non-inverting amplifier stage made by and feedback resistors R_1 and R_2 . The working of this circuit is as the non-inverting input of the main OTA is $V_{out1} = V_{in}$. Thereafter, by means of a straight forward analysis the voltage at the inverting input of the auxiliary OTA is $V_A = \alpha V_{in}$. This attenuated voltage V_A is then converted into a current which is driven by and given through output transistors with a mirror scaling factor, obtaining an output current.

The attenuators are kept inside the negative feedback loop, stability issues may happen if frequency compensation techniques are not used.

3.3. Feed forward Current Attenuation Voltage to Current Converter

The FFCA V-I converter approach in shown in Fig. 4, the reduction of the voltage across resistor is again attained by keeping an attenuator between the OTA non-inverting input (at a voltage due to negative feedback) and node A, it is implemented using a linear resistor R_1 driven by a current source proportional to V_{in} . To

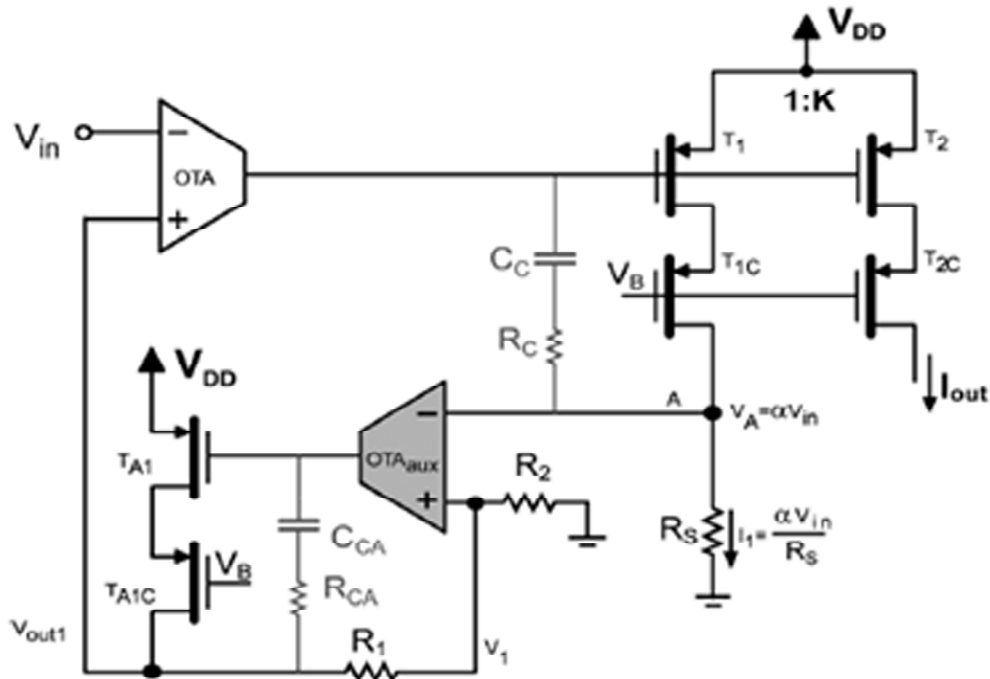


Figure 3: Schematic of Feedback Voltage Attenuation V-I Converter

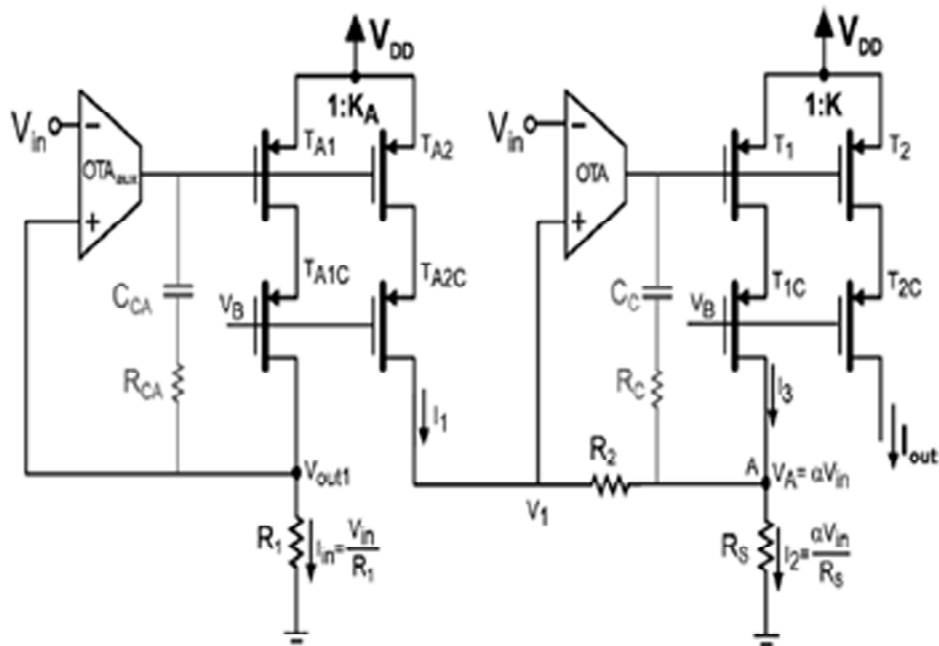


Figure 4: Schematic of Feed forward Current Attenuation V-I Converter

produce the required current, an auxiliary OTA V-I converter created by OTA aux, T1-T1A, and R1 is used. The voltage is buffered to and then it is converted into a current. This current drives resistor R_2 , so that the voltage across R_2 results V_{R2} and the voltage at node A is reduced to $V_a = \alpha V_{in}$. Therefore, current I_2 is given by $\alpha V_{in}/R_s$, while current through transistors T_1 and T_{1c} is given by $I_2 - I_1$. This current is then replicated with a mirror scaling factor to generate an output current I_{out} .

In this method, in spite of transistors T_{A1} and T_{A2} enter the triode region, the current copy in the auxiliary V-I converter is not seriously ruined, as the triode operation of T_{A1} is imitated in T_{A2} . This is achieved by forcing T_{A1} and T_{A2} not to have not only same gate and source voltages, but also same drain-voltage over the whole operating range.

4. OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

All V-I approaches are designed using the same core Operational Transconductance Amplifier. This main Operational Transconductance Amplifier consists of two complementary differential amplifier stages in parallel to achieve rail-to-rail input. It is biased with a current of $I_B = 0.5\mu\text{A}$, and provides 40 dB open loop gain, which is enough to give a linear $I_{\text{out}} - V_{\text{in}}$ relationship.

In the voltage attenuation approaches to achieve good resistance matching, and as a negotiation between area and power consumption, resistors R1 and R2 are set to 25k ohms. Consequently, the voltage attenuation factor is $\alpha = 0.5$. Hence, the input common mode voltage for the auxiliary OTAs ranges from 0 to $V_{\text{in}}/2$. Therefore not a rail-to-rail but a simple pMOS input stage OTA is used, that is obtained from the main OTA by removing some transistors.

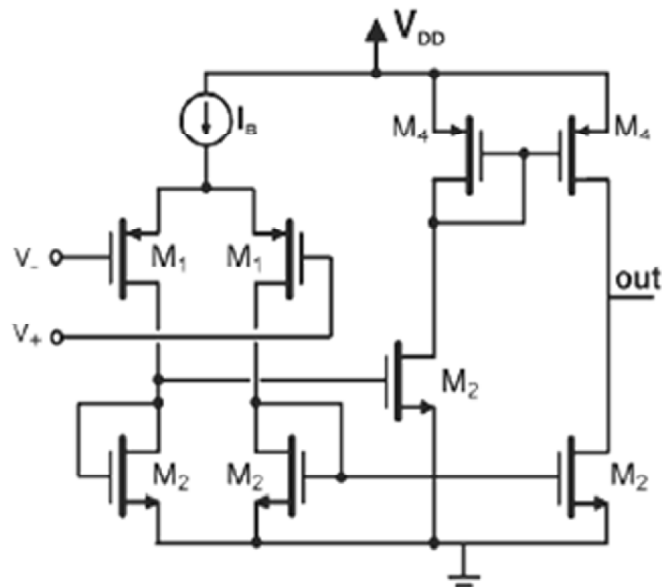


Figure 5: Schematic of simple pMOS input stage OTA

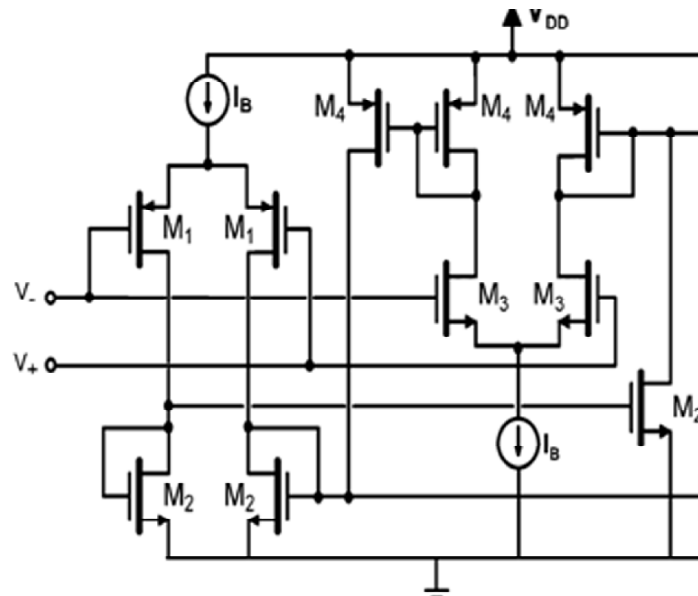


Figure 6: Schematic of OTA with two complementary differential amplifier stages in parallel

These two operational transconductance amplifiers work in the sub threshold region for the complete input range to decrease power consumption.

5. SIMULATION RESULTS

The proposed circuits and also the other circuits presented are simulated in 90nm technology in order to verify the performance of the proposed voltage to current converter. All circuits are optimally designed for $V_{dd} = 1.8V$ and an input voltage $V_{in} = 2.4mV$.

The transient response of the conventional V-I converter is shown in Fig. 6. It can be seen that the output is not linear for the entire input range. Fig 7, Fig 8, Fig 9 shows the transient response of FFVA, FBVA, FFCA voltage to current converters. . The graph shows that the proposed V-I converters give better

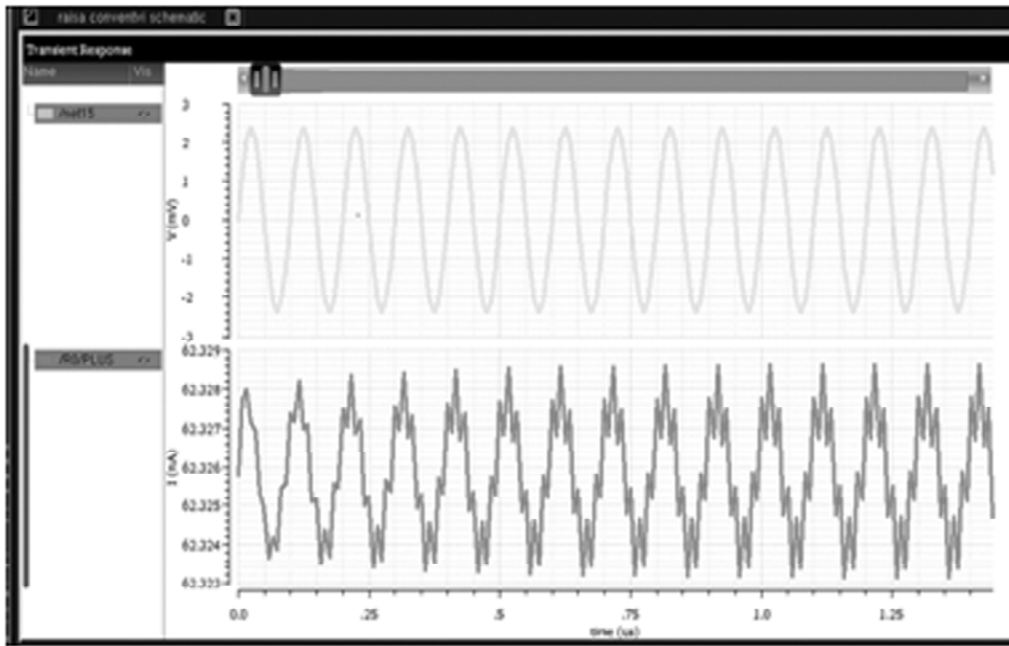


Figure 7: Transient Response of Conventional Voltage to current converter

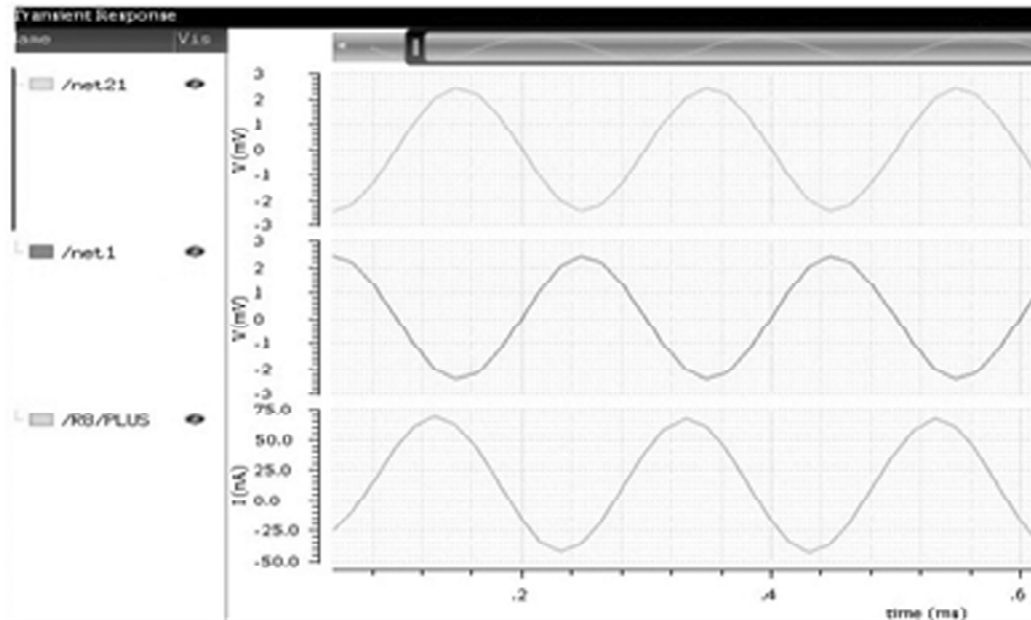


Figure 8: Transient Response of Feed forward voltage attenuation V-I converter

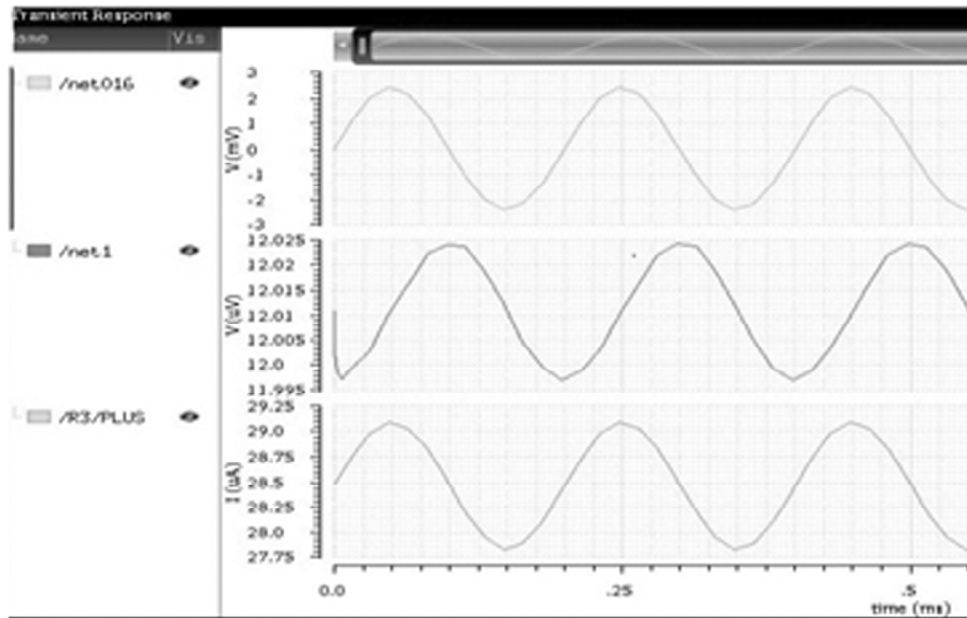


Figure 9: Transient Response of Feedback voltage attenuation V-I converter

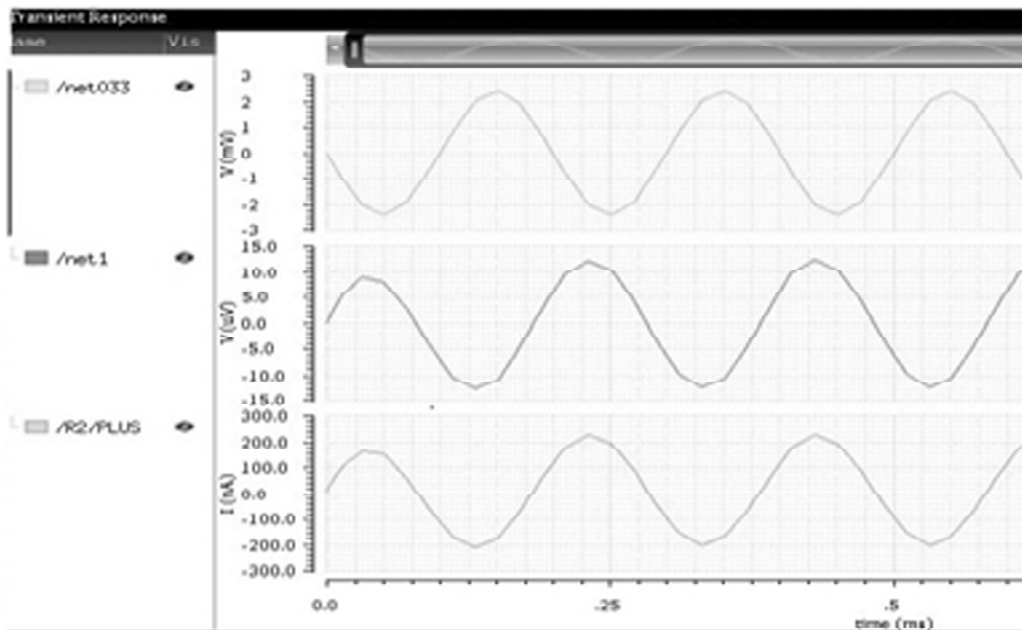


Figure 10: Transient Response of Feed forward Current Attenuation V-I Converter

rail to rail output compared to the conventional V-I converter. The Feedback voltage V-I converter is the one with better output current of $1\mu\text{A}$.

Fig 10, Fig 11, Fig 12 depicts the DC transfer response of FFVA, FBVA, FFCA voltage to current converters. In the DC response the transconductance G_m value is found at each point in the graph.

The Feed forward attenuation V-I converter is the one with better transconductance value of about 7.7mS .

The average input referred noise spectral density has been simulated and reported in Table I. This means that attenuation worsens noise. Regarding the three proposed converters, the FFCA and FFVA is the one with less noise.

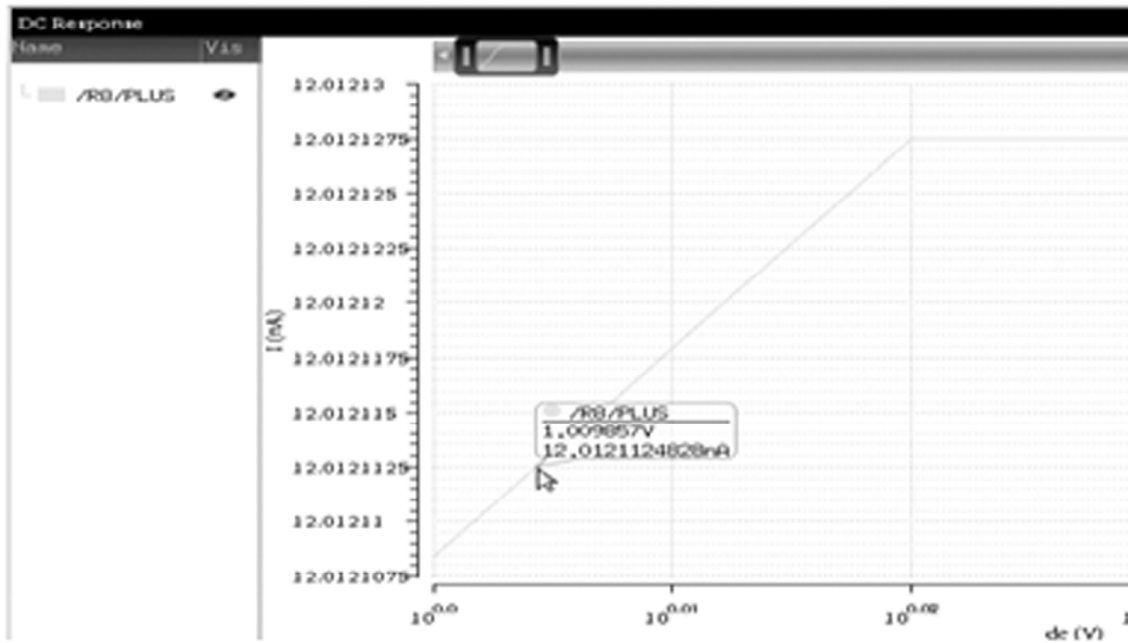


Figure 11: DC Response of Feed forward voltage attenuation V-I converter

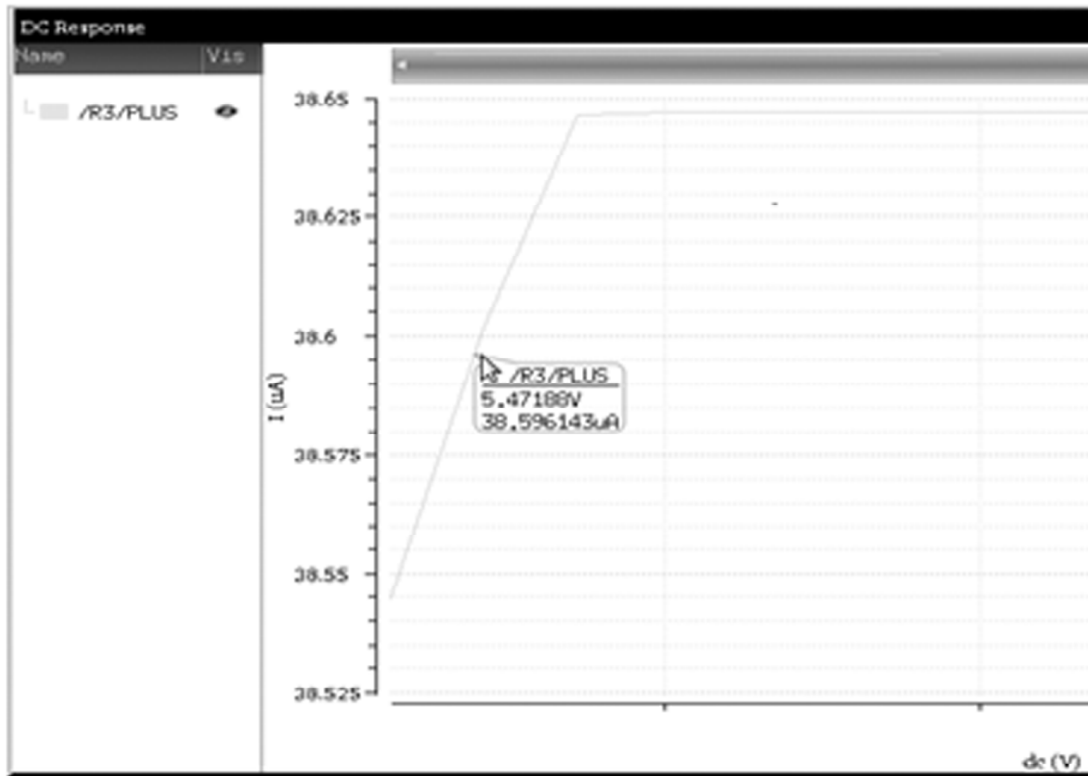


Figure 12: DC Response of Feedback voltage attenuation V-I converter

A comparison based on the given figure of merit, confirm that the FBVA and FFCA is the one with better performances. For the portable target application, the FBVA was chosen because of the overall performances, but mainly because of the Transconductance and the low power consumption. If noise or temperature stability becomes a priority, the FFCA is the suitable converter.

When compared with conventional V-I converter, the proposed V-I converters using operational transconductance amplifier shows remarkable the reduction on power consumption.

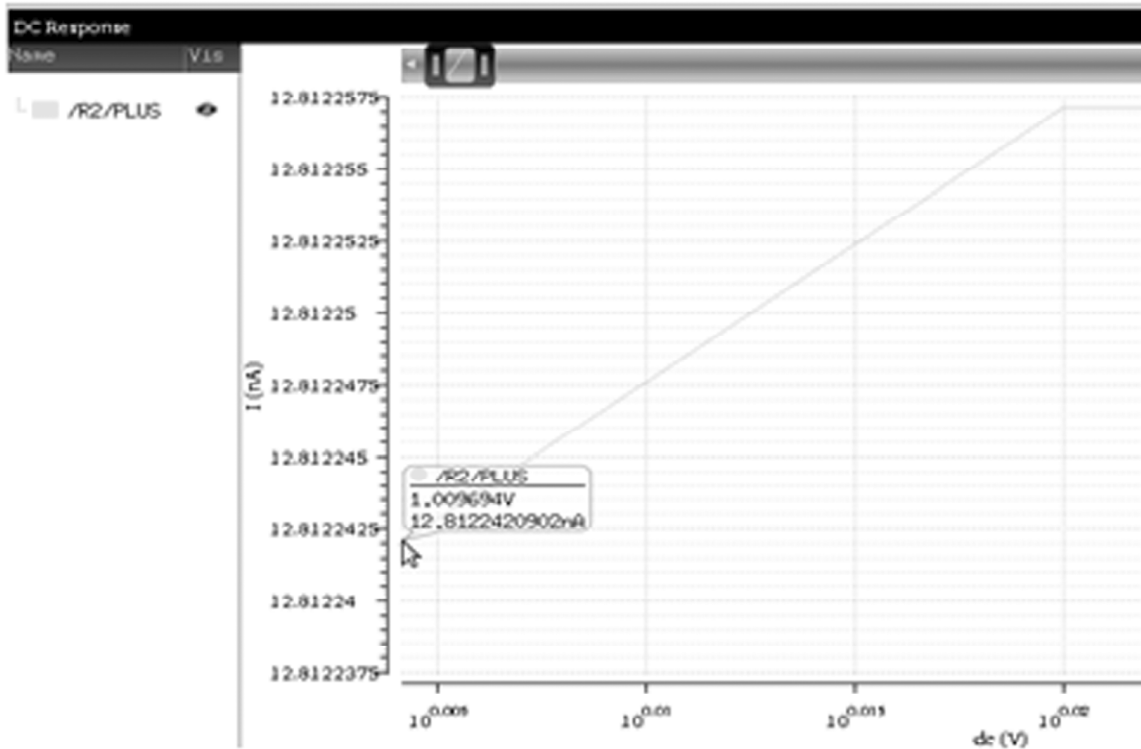


Figure 13: DC Response of Feed forward current attenuation V-I converter

Table 1
Comparison of V-I converters performances

Parameter	FFVA	FBVA	FCVA
Transconductance Gm	12.01 μ S	7.7mS	12.81 μ S
Power	596.8nW	557.2nw	557.2nw
Bandwidth	1.846MHz	2.113MHz	2.308MHz
Input referred noise	300pV \sqrt Hz	724.2pV \sqrt Hz	302pV \sqrt Hz
Figureofmerit	6.19GHz/W	7.5GHz/W	8.28GHz/W

6. CONCLUSION

Designed and analyzed the performances of three V-I converters using cadence virtuoso tool using 90nm technology. The converters shows a true rail to rail operating range. This improvement is of great importance in certain applications, such as low voltage portable application, voltage-to-frequency converters where rail-to-rail operation of the V-I converter at input stage affect the circuit performances.

ACKNOWLEDGEMENT

The authors would like to thank and acknowledge the Electronics and Communication Department of SRM University, Kattankulathur, for extending their support and also for providing the CADENCE Lab facility.

REFERENCES

- [1] A. Demosthenous and M. Panovic, "Low-voltage MOS linear transconductor/squarer and four-quadrant multiplier for analog VLSI," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 52, no. 9, pp. 1721–1731, Sep. 2005.
- [2] J. M. Algueta-Miguel, A. J. Lopez-Martin, L. Acosta, J. Ramirez Angulo, and R. Gonzalez-Carvajal, "Using floating gate and quasi-floating gate techniques for rail-to-rail tunable CMOS transconductor design," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 58, no. 7, pp. 1604–1614, Jul. 2011.

- [3] C. Azcona, "Design of CMOS voltage-to-frequency converters for low-power sensor interfacing," Ph. D. dissertation, University of Zaragoza, Zaragoza, Spain, May 2012.
- [4] A. J. López-Martín, J. Ramírez-Angulo, and R. G. Carvajal, "1.5 V 3 mW CMOS V-I converter with 75 dB SFDR for 6 input swings," *Electron. Lett.*, vol. 43, no. 6, pp. 31–32, Mar. 2007.
- [5] N. Hassen, H. B. Gabbouj, and K. Besbes, "Low-voltage, high-performance current mirrors: Application to linear voltage-to-current converters," *Int. J. Circ. Theor. Appl.*, vol. 39, pp. 47–60, Jan. 2011.
- [6] S.J. Chang, Y.Z. Lin, and Y.-T. Liu, "A digitally calibrated CMOS transconductor with a 100-MHz bandwidth and 75-dB SFDR," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 11, pp. 1089–1093, Nov. 2008.
- [7] C.C. Wang, T.J. Lee, C.C. Li, and R. Hu, "An all-MOS high-linearity voltage-to-frequency converter chip with 520-kHz/V sensitivity," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 8, pp. 744–747, Aug. 2006.
- [8] C. Azcona, B. Calvo, N. Medrano, A. Bayo, and S. Celma, "12-b enhanced input range on-chip quasi-digital converter with temperature compensation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 3, pp. 164–168, Mar. 2011.
- [9] C. Azcona, B. Calvo, S. Celma, and N. Medrano, "Highly-linear rail-to rail 1.2 V-0.18 CMOS V-I converter," *Electron. Lett.*, vol. 47, no. 18, pp. 1018–1019, Sep. 2011.
- [10] C. Azcona, B. Calvo, S. Celma, and N. Medrano, "Low-voltage lowpower CMOS rail-to-rail V-I converters," in *Proc. 2011 20th European Conf. Circuit Theory and Design (ECCTD)*, 2011, vol. 1, pp. 182–185.
- [11] B. R. Gregoire and U.K. Moon, "Process-independent resistor temperature-coefficients using series/parallel and parallel/series composite resistors," in *Proc. 2007 IEEE Int. Symp. Circuits and Systems (ISCAS'07)*, May 2007, vol. 1, pp. 2826–2829.
- [12] R. J. Baker, H. W. Li, and D. E. Boyce, "CMOS," in *Circuit Design, Layout and Simulation*. New York: IEEE Press, 1998.
- [13] P. P. Vervoort and R. F. Wassenarr, "A CMOS rail-to-rail linear VI-converter," in *Proc. 1995 IEEE Int. Symp. Circuits and Systems (ISCAS'95)*, May 1995, pp. 825–828.
- [14] C.C. Hung, M. Ismail, K. Halonen, and V. Porra, "A low-Voltage rail-to-rail CMOS V-I converter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 46, no. 6, pp. 816–820, Jun. 1999.