International Journal of Control Theory and Applications

ISSN : 0974-5572

Volume 10 • Number 36 • 2017

Baud Rate Generation at Fractional Multiples of Clock Frequency with a Single Electron Transistor Operating with Nano-Electronic Properties

Arul C[a] and Omkumar S[b]

[a]*Research Scholar, SCSVMV University, Kancheepuram, India.*

E-mail: arulvlsi123@gmail.com

[b]*Associate Professor, Department of Electronics and Communication Engineering, SCSVMV University, Kancheepuram, India.*

E-mail: omkumar1234@gmail.com

Abstract: 1. To study the Nano-electronic properties of a transistor 2. To analyze how Nano-electronic transistor differs from its CMOS and Bi-Polar counterparts 3. Model the transistor and utilize it in an application Methods/ Analysis: The quantum electronic behavior of an electron is studied. The analysis of different possible external conditions that can be utilized to confine an electron within an island is done. The transistor is modeled to show quantum mechanical properties at its terminals. The model is utilized to develop a frequency divider circuit. Findings: The Nano-Electronic transistor is able to control the motion of a single electron which is a major difference compared to the conventional MOS transistors as well as BJTs. Single electron control opens doors for opportunities like significant power reduction and area reduction. Novelty/Improvement: The power consumption is reduced compared to the power consumption of a typical transistor designed using CMOS or BJT.

Keywords: *Nano-electronics, Quantum-Theory, Coulomb-Island, Coulomb-Blockade.*

1. INTRODUCTION

The integration density of VLSI of CMOS circuits has been squaring for every one and a half year as of now. New Physical Design Techniques are evolving day by day and emphasis has been put on reducing the leakage current. However as the chip size is scaled below extremely low lengths leakage current which was not of paramount importance in micrometer scales becomes significant factor to be considered. The need for developing a device as a replacement for conventional CMOS and BJT is required. This leads to the motivation of research in nano-electronic properties of a transistor and that is the reason we choose to work in this area. The Reconfigurable Field Effect Transistor(RFET) is required to change the polarity of the transistor from *p*-type to *n*-type and vice versa [1].

This reconfiguration opens doors of opportunities to use the sametransistor to behave as a different gate thereby utilizing the same chip area to implement a different logic function. The RFETs were implemented using additional program gates. The simulation and experimental measurement results show that the DC characteristics of a Single Gate RFET(SGRFET) is the same as that of the complicated Dual Gate RFET(DGRFET).

Due to simple construction the channel length of the SGRFET is small which leads to faster operation. The infrared imaging provides high resolution capability and the microwave imaging provides high penetration capability. The THz electromagnetic spectrum which lies between infrared and microwave imaging combines the advantage of infrared imaging and the microwave imaging [2].

Physical Unclonable Functions(PUF) do exist for intrinsic CMOS circuits and considerable research is required to use the same with nano-electronic transistors [3]. Considerable attention needs to be paid to development of logic synthesis tools that can handle logic circuits made up of nano-electronic transistors [4]. The inkjet printing on flexible paper and additive manufacturing technologies is needed for design of nano-antennas and RF sensors [5]. GaN based Light Emitting Diodes are improved by photon management using nano-technology [6].

CMOS technology cannot be scaled indefinitely [7]. Charge-Based-Technologies for design of new nano-electronic components that can replace conventional CMOS is the subject of the work. Solar energy harvesting is done using photovoltaic cell as of now. Researchers are now exploring possibilities to develop nano-electronic transducers which can convert light to electricity or heat to light and then electricity [8]. The most efficient and versatile tools to create and process materials at nano scale are found to be plasmas with densities 10^{13} m^{-3} to 10^{23} m^{-3} [9]. CMOS transistor is a macro level component. However as the size is scaled to nano meter, the continuous nature of matter is no longer valid and a transistor in this scale can be considered to be made up of finite elementary particles [10].

2. THEORY OF NANO-ELECTRONICS

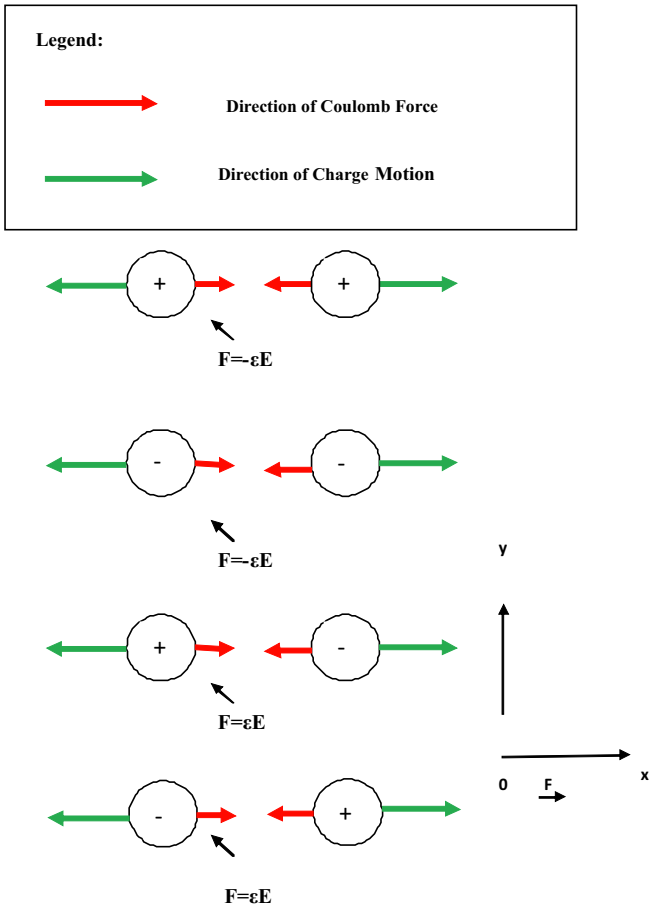

Figure 1: Basic Operation of Coulomb Blockade

The granularity of charge in terms of the finite number of charge or electrons need to be taken into consideration at nanometer lengths. The Coulomb Blockade forms the base of the nano-electronic transistor. The Coulomb Blockade is based on attraction and repulsion of fundamental charges which is shown in Figure 1.

Figure before an extra electron being injected from outside then this uncompensated single electron charge will create an electric field which repulses the addition of following electrons.

To ensure that the generated electric field is strong enough so that charge control is possible, the square of the island size has to be small enough.

This phenomenon is described more elaborately using the charging energy E_c, as:

$$E_c = \frac{e^2}{C} \quad (1)$$

3. MODEL OF NANO-ELECTRONIC TRANSISTOR

The model of the nano-electronic transistor should reflect the electrical properties required as that of CMOS or BJT at its ports. A similar property to those of CMOS or BJT will suffice to use the transistor in applications that are prevalent today. However to take advantage of new properties that are exhibited by nano-electronic materials the properties such as Coulomb Blockade have to be modelled.

Modeling at higher level of abstraction is required because we are interested in the electrical properties of the device. Verilog-A supports behavior level modeling which has higher level of abstraction. A transistor modelled at this level has properties of a CMOS or its BJT counterpart as well as that of a nano-electronic material. Verilog-A also supports conversion of non-electrical parameters to an equivalent electrical parameter. The conversion is facilitated by modelling the physical phenomena of a new technology under consideration using mathematical equations and deriving electrical equivalents of the same.

4. NANO ELECTRONIC DEVICES:

The Coulomb blockade, electron tunneling, Coulomb staircase and oscillations are the properties of nano-electronic transistor that has one of the biggest advantage of providing the ability to confine an electron within two tunnel junctions.

The tunnel junction is the basic building block of all family of nano-electronic devices and circuits. The tunnel junction is characterized by its cross section resistance R and capacitance C. The schematic representation of the Tunnel Junction is shown in Figure 2.

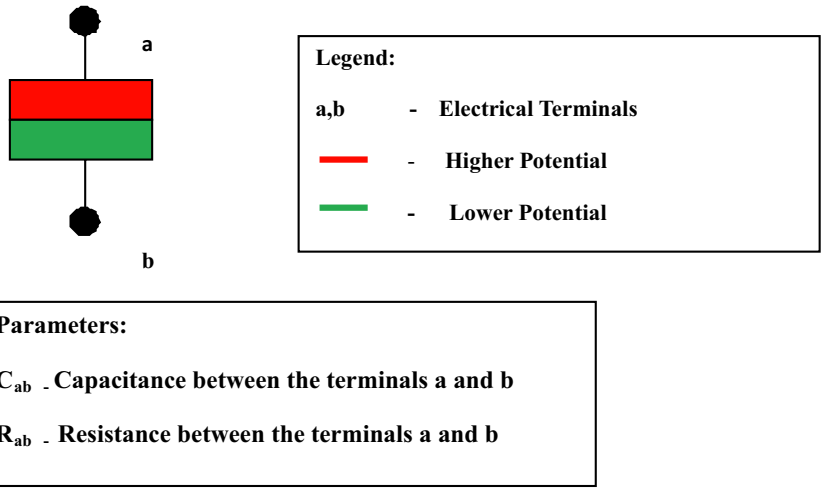

Figure 2: Schematic Representation of the Tunnel Junction

5. CRITERIA FOR MAKING THE SINGLE ELECTRON NANO-ELECTRONIC TRANSISTOR OPERATIVE

The nano-electronic transistor should be biased to make it operative under standard test conditions. The nano-electronic transistor has a drain, gate, and a channel in between for conduction and the conduction being controlled by the gate 1 and gate 2 electrodes. The voltage of gate 1 is usually varied keeping gate 2 potential constant. The gate 2 has control over the threshold voltage of the transistor. When a positive voltage is applied at the bias terminal electrons are pulled into the island from the bias terminal.

When steady state is reached, a small increase in gate 1 bias voltage pulls more number of electrons from the bias terminal into the central island and a consequent decrease of the same pushes electrons into the storage node. The number of electrons pulled or pushed depends on the applied gate bias voltage and the gate voltages. The storage node may be connected to a capacitor or optionally be connected to the ground. The criteria is illustrated graphically in Figure 3.

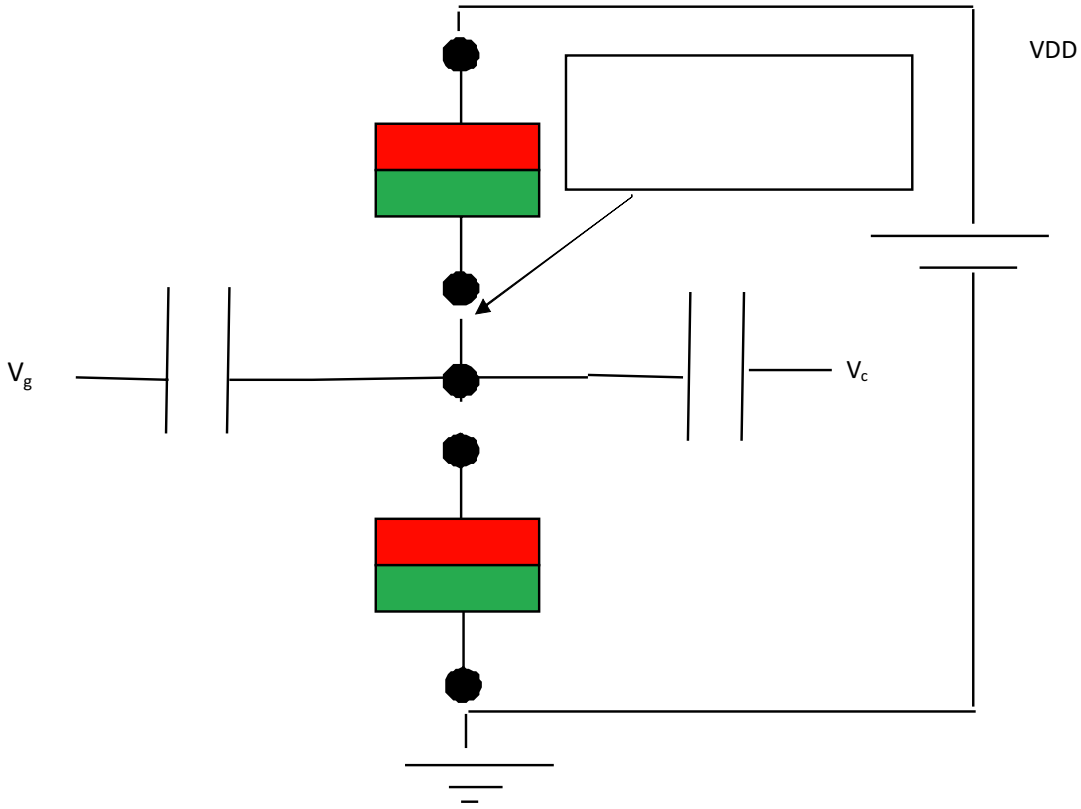

Figure 3: Criteria for Operation

6. HYPOTHESIS

The following assumptions are made with regard to the Single Electron Nano-Electronic transistor.

The voltages of all nodes are the same under steady state condition.

The interconnect capacitances are very much smaller than the device capacitances.

The first assumption is to make sure that the all the fabricated devices are alike and divide the potential equally when applied with a bias voltage. The second assumption prevents unnecessary complications in the analysis and makes the circuit relatively immune to parasitic effects.

7. ANALYSIS:

The charge accumulated on the capacitance existing between node a and node b is given by equation 2.

$$q_a = \sum_{b=1}^{N} C_{ab} V_b \quad (2)$$

q_a = The charge on the node a

C_{ab} = The capacitance between the node *a* and *b*

V_b = The potential of the node *b*

The orthodox theory finds the probability an electron tunnels through the junction using stochastic modeling of the tunneling events with probability per unit time. The result of this tunneling event is the reduction of free energy as given by 3.

$$\Gamma = \frac{\Delta E}{e^2 R_T [1 - \exp(-\Delta E / k_B T)]} \quad (3)$$

ΔE – Change in Energy of the System before and the tunnel even

e – *Ch arge e* of an electron

R_T – Re *sis* tan *ce* of the Tunnel Junction

kBT – The thermal energy

$$\Delta E = -e(|V_{ab}| - V_c) \quad (4)$$

V_{ab} = Voltage acros the tunnel junction

V_c = Control voltage of the tunnel junction

$$V_c = \frac{e}{2(C_{ext} + C_T)} \quad (5)$$

V_{ext} – The equivalent capacitance of the reminder of the circuit viewed from the tunnel junction.

C_T – Capacitance of the tunnel junction

When $V_{ab} > V_c$ an electron will tunnel from node b to node a. The node voltages and charges on those nodes will also change.

The operation of nano-electronic transistor is characterized by cycle of electron transfers. Electron tunnels from SN to N3 through two tunnel junctions when V_g increases from zero to a certain positive value (assume a positive value of V_b), after another). The electron starts tunneling from N3 to N1 when Vg returns to a smaller value and the transfer cycle is completed when V_g becomes equal to zero. The voltage on the storage node changes due to the electron charges that get accumulated at the SN.

8. VERILOG-A MODEL OF THE NANO-TRANSISTOR

The Verilog-A language is used to construct the model. The nano-electronic model of the transistor is developed and used in baud generator application, which is simulated with a SPICE simulator. The model is included in the SPICE netlist and simulated using SPICE simulator.

9. RESULTS AND DISCUSSION

The transient analysis and power analysis were done. The transient response of the input waveform in Figure 4 and output waveform is shown in Figure 5. From the waveform it is clear that the time period of the input waveform is 20 ns. The time period of the output waveform is 50 ns. This amounts to a frequency of 50 MHz and 20MHz respectively. Hence the input frequency is divided by a factor of 2.5. This is a divide by non integer, which leads to a complicated circuit if implemented using CMOS technology. The power consumption for the Nano Transistor is 10.8840 pW which is a huge advantage.

10. EXPERIMENTAL RESULTS:

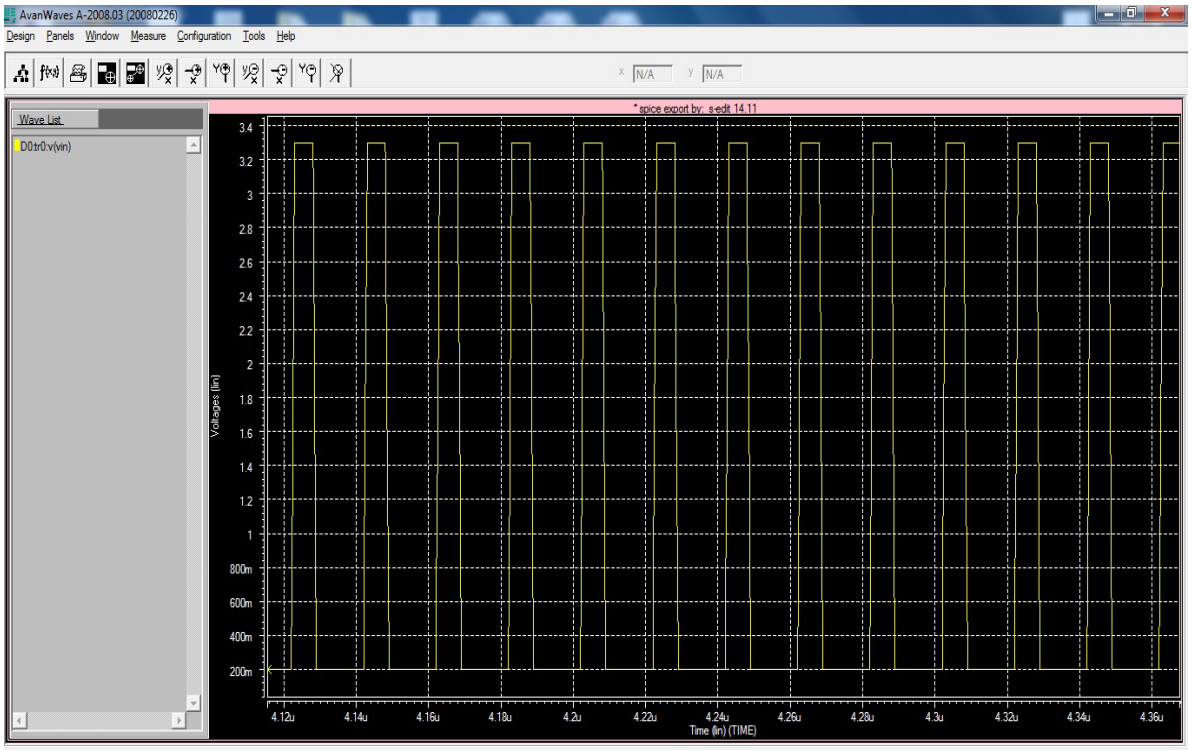

Figure 4: Input Waveform in the Scope with Time Period = 20 ns

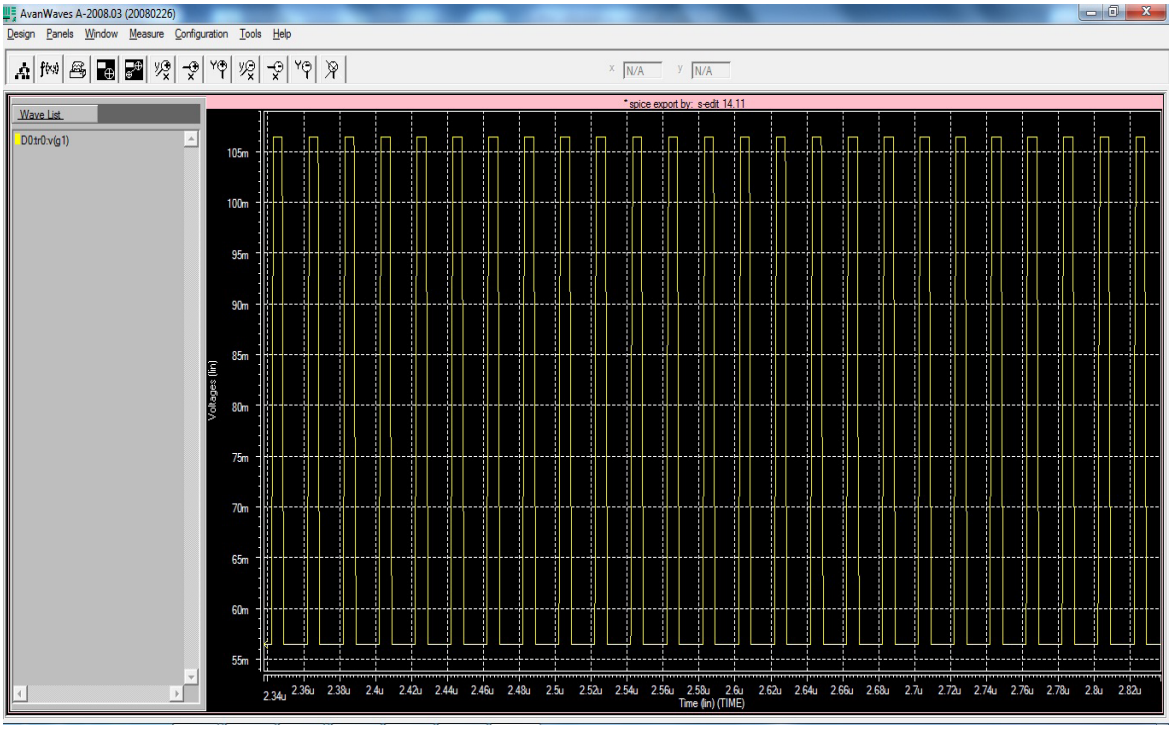

Figure 5 Output Waveform in the Scope with Time Period = 50 ns

REFERENCES

[1] Darbandy, Ghader, Martin Claus, and Michael Schröter. "High-Performance Reconfigurable Si Nanowire Field-Effect Transistor based on Simplified Device Design." IEEE Transactions on Nanotechnology, Vol. 15, No.2, PP-289-294,2016.

[2] Zhang, Mingyu, and John TW Yeow. "Nanotechnology-Based Terahertz Biological Sensing: A review of its current state and things to come." IEEE Nanotechnology Magazine", Vol. 10, No. 3,30-38, 2016.

[3] Gao, Yansong, et al. "Emerging physical unclonable functions with nanotechnology." IEEE access 4,61-80, 2016.

[4] Amarú, Luca, et al. "New logic synthesis as nanotechnology enabler." Proceedings of the IEEE, Vol. 103, 2168-2195, 2015.

[5] Hester, Jimmy G., et al. "Additively manufactured nanotechnology and origami-enabled flexible microwave electronics." Proceedings of the IEEE 103.4 ,583-606, 2015.

[6] Hsiao, Yu-Hsuan, Meng-Lin Tsai, and Jr-Hau He. "GaN-Based Multiple-Quantum-Well Light-Emitting Diodes Employing Nanotechnology for Photon Management." IEEE Transactions on Industry Applications 51.2, 1277-1283, 2015.

[7] Marshall, Andrew. "Thoughts on Possible Future Charge-Based Technologies for Nano-Electronics." IEEE Transactions on Circuits and Systems I: Regular Papers 61.11,3057-3065, 2014.

[8] Khoshaman, Amir H., et al. "Thermionics, thermoelectrics, and nanotechnology: New possibilities for old Ideas." IEEE Nanotechnology Magazine 8.2 ,4-15, 2014.

[9] Rawat, R. S. "High-energy-density pinch plasma: A unique nonconventional tool for plasma nanotechnology." IEEE Transactions on Plasma Science 41.4 (2013): 701-715.

[10] Bishop, David. "Nanotechnology and the end of Moore's Law?." Bell Labs Technical Journal 10.3, 23-28, 2005.

[11] Touati, F. and OMAN, S.O. "High-Performance CMOS and BiCMOS Transimpedance Preamplifiers for Optical Communications", Asian Journal of Information Technology, Vol. 3, No. 4, pp.287-292,2004.

[12] Sreedevi, M. and Paul, K., "Design and optimization of a high performance low-power cmos flex cell", International Journal of Signal System Control and Engineering Application, Vol.3, No.4, pp.65-69, 2010.

[13] Sedaghati, N., Mamun, M., Rahman, L.F. and Husain, H., "Design of 4-bit memory column dram cell in 0.18 µim CMOS process", Journal of Engineering and Applied Sciences, Vol. 8, No. 9, pp.269-272, 2013.

[14] Wan, Q. and Wang, C., "Design of 3.1–10.6 GHz ultra-wideband CMOS low noise amplifier with current reuse technique", AEU-International Journal of Electronics and Communications, Vol. 65, No. 12, pp.1006-1011, 2011.

[15] Eswaran, P. and Malarvizhi, S., "Design analysis of mems capacitive differential pressure sensor for aircraft altimeter", International Journal of Applied Physics and Mathematics, Vol. 2, No.1, p.14, 2012.