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Power Quality Regulations Using ANFIS–Synchronous Reference Frame Controller on Unified Power Quality Conditioner

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ABSTRACT

This paper is presents a control of power quality regulation using transformer less parallel injection of unified power quality conditioner systems (UPQC). An unbalanced and distorted utility power supply is taken in account in power quality disturbances and challenging task to overcome power quality disturbances in transformer less parallel injection. The Adaptive network based inference system (ANFIS) based synchronous reference frames controller is proposed in this topology. The natural merits of synchronous reference frame controller is used to extract harmonics content from unbalanced and distorted power lines and also reduces disturbances by synchronized reference frame controller is applied to both series and shunt converter. The presence of ANFIS controller on synchronous reference frame controller (ANFIS-SRF) is used to improve an accurate harmonics extraction and reduction by synchronization principles and draws better performances across shunt and series converter. The shunt and series voltage source converter operation is controlling of load harmonics, load unbalances, load reactive power control and power factor correction using proposed controller topology. The performance of entire topology is implemented and verified by MATLAB/Simulink results.

Keywords: Unified Power Quality Conditioner (UPQC), Synchronous Reference Frame (SRF) controller, Adaptive network based Fuzzy Inference System (ANFIS), Adaptive Network based Fuzzy Inference System- Synchronous Reference Frame Controller (ANFIS-SRF), Parallel Side Converter (PSC), Series Side Converter (SSC).

1. INTRODUCTION

The power quality problems are a great impact on AC transmission line system and distribution system in present era of AC networks. An essential power quality problems are voltage sag, swell, real power, reactive power, load harmonics, unbalances of utility power supply, distortion of utility power supply, power factor correction. So many Flexible AC Transmission System (FACTS) are used in literatures depends on power quality issues such as Static Var Compensator (SVC), Dynamic Voltage Restorer (DVR), Static synchronous Compensator (STATCOM), Thyristor Controlled Series Compensator (TCSC), Interline power Quality Conditioner or Improved Power Quality Conditioner (IPQC), Thyristor Protected Series Compensation (TPSC), Unified Power Flow Controller (UPFC) and Unified Power Quality Conditioner (UPQC). These are widely used for an effective transient and steady state voltage control on AC transmission and distribution lines. Static Var Compensator (SVC) is applied for damp power swings, reactive power control and fast response of transient voltage control .Static compensator (STATCOM) is required to reduce filter range and high voltage transient control. DVR is applied for voltage sag, swell and reactive power control. TCSC is applied in transmission line for stability of power flow control, oscillation control. IPQC is applied for current balances and improvements, power factor correction [1].

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TPSC is placed on transmission lines for fast over voltage protection during multiples faults conditions. UPFC is placed between middle of transmission lines for improving and controlling of power flow, real and reactive power control. UPQC is a combined application and process of STATCOM and DVR. The unified power quality conditioner is flexible solutions for power quality issues even at so many FACTS devices are presents. Series side converter act as DVR where as parallel side converter act as STATCOM and both are connected as back-to-back converter via DC-Link capacitor [2].

A common applications of UPQC are current harmonics minimization across load, real, reactive power control by absorption and injection principles, sag, swell compensation and displacement of unity power factor control [3].DC-Link voltage and its control is a main part of power balances and quality control so this is needed to control at peak value of voltage (phase to neutral voltage) in during power quality disturbances, sag and swell compensation [4]-[6]. So many literatures are explained and provided solutions for power quality during unbalances and distorted utility power supply conditions [7]-[11]. Injection of Parallel transformer is required for parallel side converter power transfer to inject with high power transmission networks but transformer design in UPQC causes bulky, cost effective and also involved in harmonics because of high frequency components which is constitute the problems concern impregnation of power. Transformer less unified power quality conditioner is presented to overcome above demerits and harmonics reductions by control law and digital mechanism in literatures [12], [13]. A Synchronous Reference Frame (SRF) controller is naturally used to extracting harmonics and distorted content in accurate form from input signals. So based on nature so many conventional methods are described in literatures [14]-[16]. But characteristics and performance of SRF controller is depends on phase lock loop design and its performances so SRF required a suitable phase lock loop system.

This paper is presented a transformer less parallel operation of four wire unified power quality conditioner system for power quality improvement. This paper analyses about harmonics and power factor correction in power quality issues and during distorted and unbalanced supply conditions. This topology of improvement is obtained by adaptive network based fuzzy inference system with synchronous reference controller to extract and control of harmonics, power factor corrections. Space vector pulse width modulation is applied to both active filters of series and parallel side converter using ANFIS-SRF controller. The proposed controller is used to maintain constant DC-link voltage during disturbances. Space vector scheme is applicable to decoupling of series and parallel converter process with utility line and also this is capable of replacing transformer in present unified power quality conditioner system. Simulation results are obtained and proved using MATLAB/Simulink environment. Design of active and passive filter on UPQC is explained in details in chapter II. The working principle of proposed controller and structures details is given in chapter III. The stepwise performance of topology, parameters details is presented in chapter IV during unbalancing and distributed power supply conditions.

2. DESIGN OF PASSIVE AND ACTIVE SERIES AND PARALLEL CONVERTER

The filter design aspects enable a little change to the rotating frame as well as the controller design. Y connected LCL filters and delta connected LCL filters design schemes are applied for series and parallel respectively shown in fig. 1. The 5.6KW UPQC is presented with 800V voltage (line to line, 50Hz). The parameters are listed in the Appendix. The fundamental components of output current for both converter (SSC and PSC) derived in low frequency. Capacitor branch has been neglected while determine control parameters because it has low pass and high frequency components.

A). The equivalent circuit for LCL Shown in fig. 1 and the filters are inserted between UPQC rotor and PSC as well as SSC and grid. U_0 Is terminal voltage, U_S is grid voltage, L_1, L_2 and are the converter and grid side inductors respectively. R_1, R_2 are the equivalent resistance of L_1, L_2 respectively. R_3 Is the damping resistor with C_3 capacitor the transfer function between input voltage U_0 and output current I_0 is

$$\frac{R_3 + C_3 s + 1}{L_1 + L_2 + C_3 s^3 \left(L_1 + L_2\right) R3C3s^2 + \left(L_1 + L_2\right) s} \tag{1}$$

Equation (1) is a third order transfer function which is offer high attention in high order harmonics with high frequency operations. The inductance value should limit the current ripples of I_1 in the range of 15%-25% of rated current [17]. The current I_1 is mainly depends on impedance X_{L1} (impedance of L_1), X_{L2C3} (impedance of L_2 and C_3) and X_{c3} (impedance of C_3). Ripple current is derived by PWM frequency is given by

$$irip\_\max = \frac{UDC}{8fPWM_{L1}} \tag{2}$$

Where U_{DC} dc-link voltage and is converter switching frequency. Based on desired current ripple i_{rip} obtained by

$$L_1 \geq \frac{UDC}{8iripp f_{PWM}} \tag{3}$$

In order to avoid voltage drop inductor L is limited and it's given by [18].

$$L_1 \leq \frac{\sqrt{U_{DC}^2/3 - U_m^2}}{wBIm} \tag{4}$$

U_m Is a peak grid voltage, I_m is a peak grid current and w_B is an angular frequency of grid voltage. High range of capacitor C_3 denotes a low impedance of X_{c3}. C_3 Is designed by following

$$C_3 \leq 5\% \times \frac{Prated}{3 \times 2\pi fB U_{rated}^2} \tag{5}$$

Where P_{rated} rated power of converter is, f_B is grid frequency and U_{rated} is RMS value of converter phase voltage.

B). The current ripple reduction (σ) is minimizing through reducing the rate of L_2, C_2 are reduces the current ripple in grid at low level.

$$\sigma = \frac{ig\left(f_{PWM}\right)}{ic\left(f_{PWM}\right)} = \frac{1}{\left|L2C3w_{PWM}^2 - 1\right|} = 10\% \tag{6}$$

Where $i_g(f_{PWM})$ and $i_c(f_{PWM})$ are the grid current ripple and converter current ripple in the switching frequency limit.

C). Resonance frequency w_{res} fixed between the range of ten times of switching frequency and half of the times of switching frequency are given by

$$10wB < wres < 1/2\, wPWM \tag{7}$$

Resonance frequency w_{res} for Y connected LCL filters is obtained by

$$w_{res} = \sqrt{\frac{L1 + L2}{L1L2C3}} \tag{8}$$

Resonance frequency for connected LCL filters is obtained by

$$w_{res} = \sqrt{\frac{L_1 + L_2}{3L_1L_2C_3}} \tag{9}$$

D). the damping resistor is implemented to reduce the complexity and improve the reliability of system. Without damping resistor (R_3) in equation (1) becomes

$$R_3 = \frac{1}{3w_{res}c_s} \tag{10}$$

Damping resistor (R_3) fixed at one third of impedance C_3 and also in resonance frequency limit.

3. WORKING PRINCIPLES OF PROPOSED TOPOLOGY

The enhancement of proposed circuit configuration is undergone an unbalancing and distorted power level for verifying the performance of proposed circuit system and its control topology. The details regarding about circuit of systems and controller is explained in clear in section A and B.

3.1. Principles of proposed structures

The circuit is consisting of series and parallel converter injection for supply and load side respectively as shown in Fig.1. Series and parallel converters are injected to main line through LRCL (L_1, R_1, C_1 & L_2, R_2, C_2) filters in the form star-delta arrangement. A three wire combination is presented in this topology so adequate range of DC-Link Capacitor is placed to control of both parallel and series combination of converter. PCC (Point of Common Coupling) is a measuring of both series and parallel circuit performance (Real power, reactive power, Total Harmonics Distortion (THD) and Power Factor Correction (PFC)) in near load. Presented filters circuit is used to overcome stress across DC-link capacitor voltage and four wire

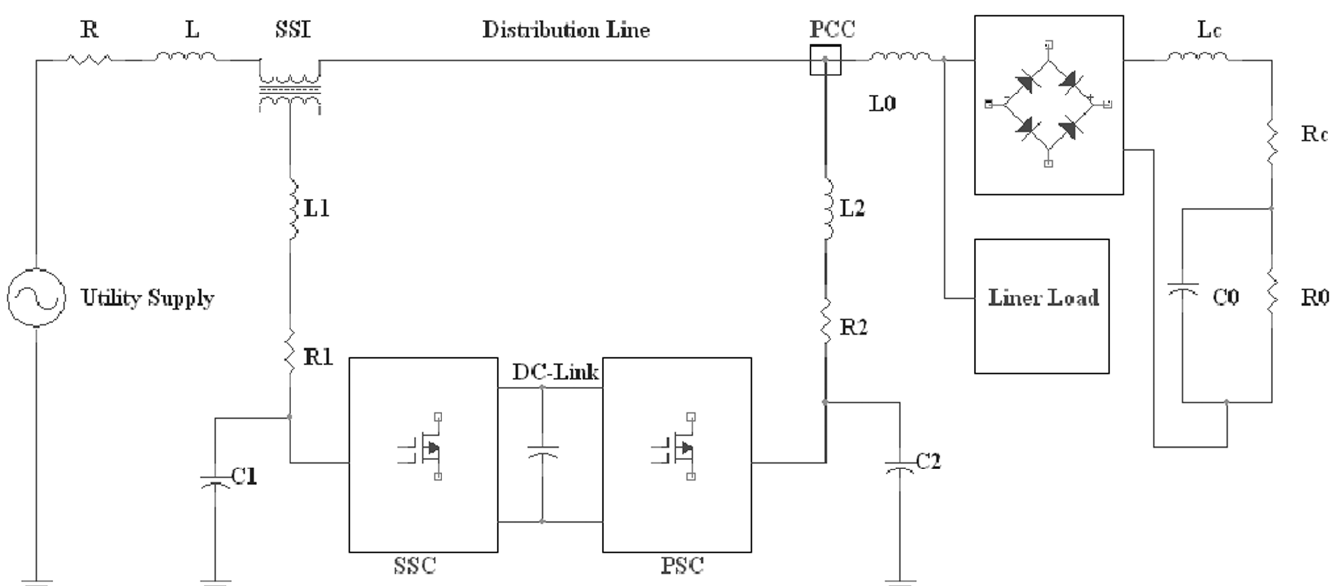


Figure 1: Proposed circuit configuration

system. A utility power supply is tested under various magnitude of voltages is called unbalancing; inductance injection across utility power supply is called distorted conditions. Even though circuit is suitable of distortion and unbalancing control, performance completion is obtained by applying a suitable control topology. The circuit of controller and working principles are given in section below B.

3.2. Adaptive Networks Fuzzy Inference System

The inference system is a non-linear system which is able to estimate Real system empirical data, least-squares combination and back propagation of gradient descent methods are used for training FIS membership function parameters to model a given set of input/output data. The fuzzy logic rules having the limitation while executing the human knowledge based on non-linearity and data among the limitation and complexity. Adaptive neuro fuzzy system having decoupling merits of fuzzy logic and artificial neural network such as complicated system, learning reading of instruction [19], [20]. Neural networks performance in two methods reading and processing output, transferring information among in between the nodes. This operation of feed forward neural networks is performed in present adaptive inference system with sugeno-fuzzy logic controller. The encoding of speed is applied and compared with reference speed and finally given proposed adaptive fuzzy inference system and its architecture is shown in fig. 2.

This control loop is easily obtained an automated bandwidth change for torque control by controlling the phase current. The proposed automated bandwidth control loop is combination of ANFIS control and filter with respect to both input and output scaling factors which is like self tuning methods [21]-[23]. Distorted and unbalancing fault signals is applied to ANFIS which belongs to PLL .The combined performance of low pass and high pass filter performance is achieved using proposed ANFIS control law and its structure. The present control loops performed as good scaling factors and noise suppression across signals and provided accurate torque references in desired frequency range and it’s provided better

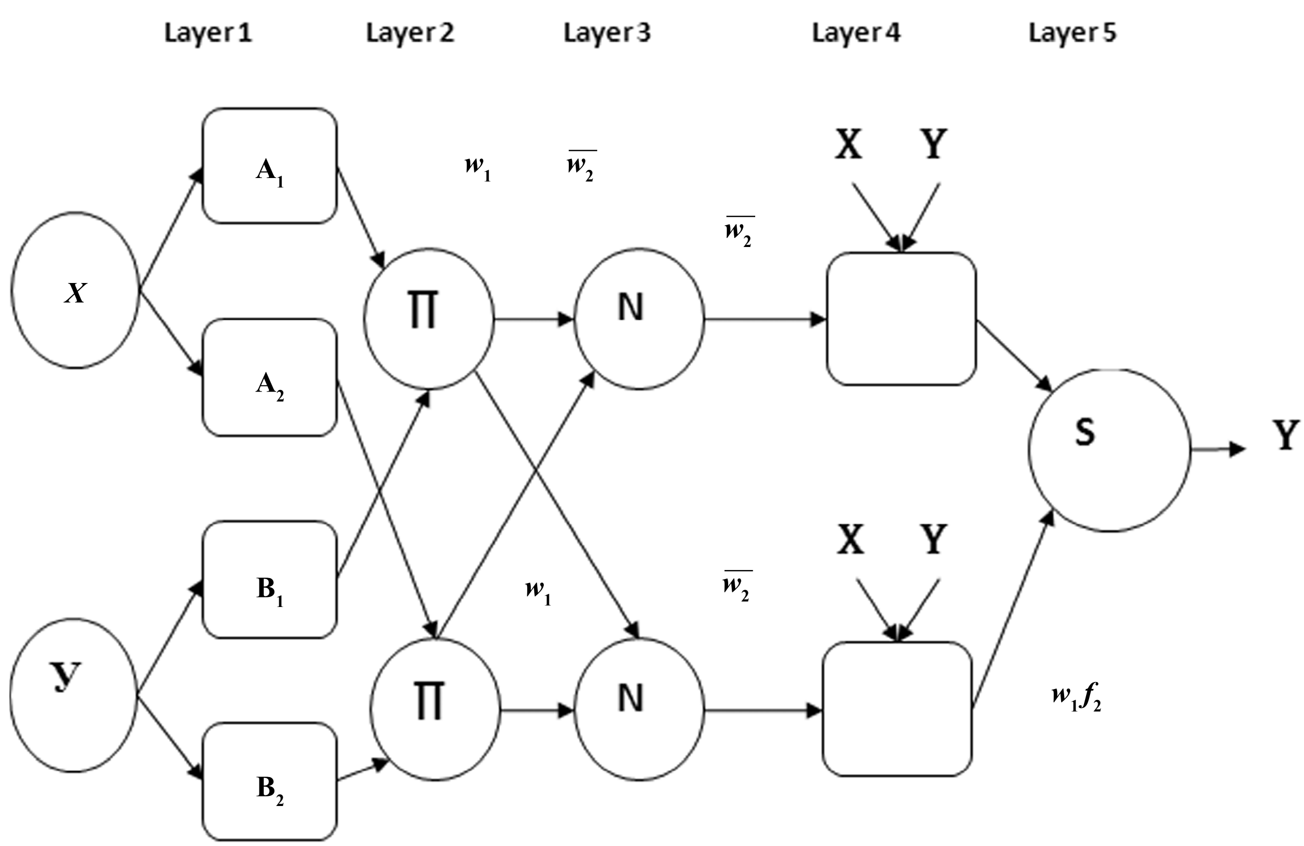


Figure 2: ANFIS architecture

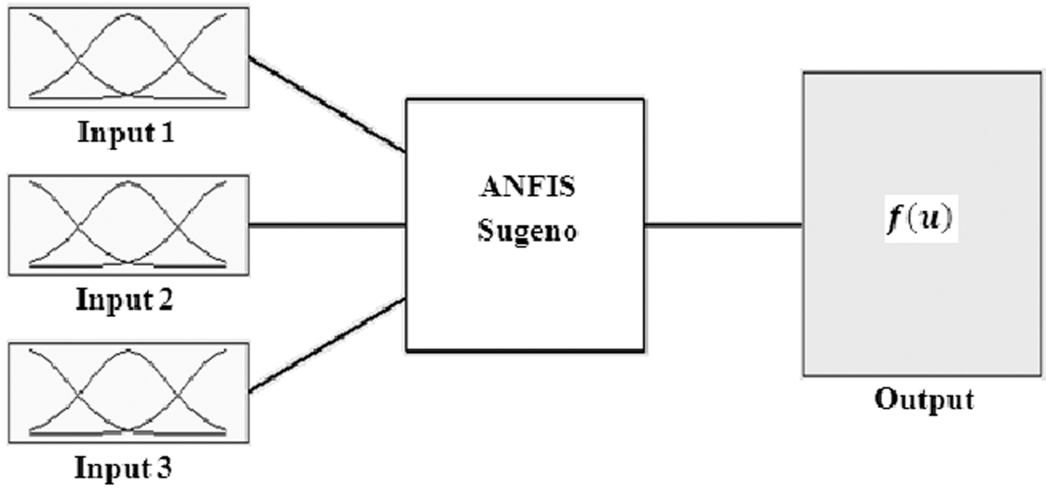


Figure 3: Adaptive Fuzzy Inference System (ANFIS) scheme

performance while it enrolled in proposed space vector approach and reducing complexity of space vector based switching selection and its loops. Adaptive neuro-fuzzy inference system is described in bellow which three set of rules for each three input selection i.e the totally a nine set of rules is described using Sugeno method in proposed ANFIS topology shown in Fig. 3.

The simulation implementation of nine set of if-then rules is implemented as

- If (input1 is input1mfn1) and (input2 is input2mfn1) and (input3 is input3mf1) then (output1mfn1 is p1input1+q1input2+h1input3.
- If (input1 is input1mfn2) and (input2 is input2mfn2) and (input3 is input3mfn2) then (output1mfn2 is p2input1+q2input2+h2input3.
- If (input1 is input1mfn3) and (input2 is input2mfn3) and (input3 is input3mfn3) then (output1mfn3 is p3input1+q3input2+h3input3.

The present proposal of ANFIS system is given bellow with respect to layers is shown in fig.8 and this implemented is shown in Fig. 9.

Layer 1

The adaptive node of this layer is used to creating a languishing label of membership function and given input variables is performed by membership function of Gaussian (*mfn*):

$$O_{2,j} = w_j = \mu_1^{i1} \mu_1^{i2} \mu_1^{i3} \mu_1^{i4} \mu_1^{i5}$$

$$(j = 1,..,ci),(i1 = 1,..,c1),..,(i5 = 1,..,c5) \tag{11}$$

Here $c1 = ... = c2 = 3$

Layer 2

Performed as it is performance details given in Layer 2

Layer3

This layer gives regularized results of firing strength from input of this layer and this layer (j^{th}) node is calculating the ratio between firing strength across the node to total firing strength of entire node.

$$O_{3,j} = \overline{w_j} = wb_j = \frac{w_j}{\Sigma i\, w_i}, (i = 1,..,3) \tag{12}$$

Layer 4

The node value of this layer is square node and its correlation between inputs to output function of this layer is expressed by

$$O_{4j} = \overline{w_j} f_i = \overline{w_j}\left(p_j t_{ox} + q_j t_{si} + h_j T + g_j V_{gs} + k_j V_{ds} + r_j\right), \tag{13}$$

$j = 1, \ldots 3$. Here $\overline{w}_j$ Is the third layer output and parameter set $\{p, q, h, g, k, r\}$. The resultant parameters is calculated from previous layer

Layer 5

The particular node of this layer output is calculating the summation of all incoming signals

$$Os = \Sigma j\, \overline{wj} f_i = \frac{\Sigma j\, wj f_i}{\Sigma j\, wj} \tag{14}$$

Here, O_s is denoted as output layer for layer 5.

4. PRINCIPLES OF SYNCHRONOUS REFERENCE FRAME

The presented a modified circuit structure of synchronous reference frame controller is designed by adequate design of phase lock loop design which is shown in Fig.4. Phase lock loop design is designed using adaptive network fuzzy inference system. This ANFIS topology is extracting an accurate reference angle from distorted power supply signals and it's implemented in easy procedure on phase lock loop circuit. The implementation procedures and details regarding about proposed ANFIS topology is described below. Proposed phase lock loop circuit is capable of converting a sum of power in auxiliary form using applied continuous supply voltage (V_{sab}, V_{scb}). i.e $V_{sab} = V_{sa} – V_{sb}$ & $V_{scb} = V_{sc} – V_{sb}$. In order to calculate ω, the continuous power supply (V_{sab}, V_{scb}) is multiplied with continuous variations of line current (I_{ax1}, I_{ax2}) in unity form to calculate sum of auxiliary power ($P3ax$).

Calculated Auxiliary power applied to ANFIS controller to reach desired magnitude and angle by sum function of ω0 = 2π*f*. calculation of ω′t is obtained by integrating of functions but ω′t is lead 90° phase difference to base frequency of system. So angle 90° is needed to subtract from calculated ω′t. The calculated form of phase lock loop reference signals unmovable form when both low frequency level of applying faulty (distorted and unbalancing) signals and auxiliary form of power is turns to zero.

The calculated signals ωt is a positive sequence form of line voltage or faulty voltages, like wise sin (ωt) is a positive sequence component with base frequency of system also cos (ωt) is similar form of frequency with sequence components. The overall synchronous reference frame controller is obtained using proposed ANFIS topology with respect to faulty conditions of measured line current. Unique merit of presented control method is not required maximum of measured current over classical schemes. This reference signals generation is capable of controlling unbalancing and distorted line conditions by extracting and eliminating harmonics and improving other power qualities.

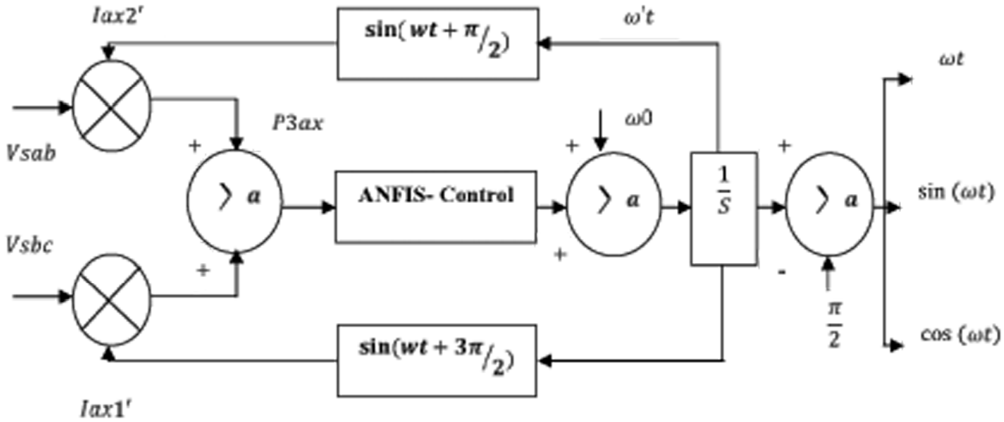


Figure 4: Phase Lock Loop (PLL) Circuit using ANFIS Controller

4.1. Proposed reference signals generation for series and parallel converter

Series side converter controller is generating reference signals by comparing with positive sequence of supply voltage with load voltages is shown in Fig. 5. Supply voltage (V_{ia}, V_{ib}, V_{ic}) is transformed as ($d - q - 0$) using transformation method as given by equation (15) and (16).

$$Trans = \sqrt{2/3}\begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ \sin(\omega t) & \sin(\omega t - 2\pi/3) & \sin(\omega t + 2\pi/3) \\ \cos(\omega t) & \cos(\omega t - 2\pi/3) & \cos(\omega t + 2\pi/3) \end{bmatrix} \tag{15}$$

$$Trans = \sqrt{2/3}\begin{bmatrix} 1/\sqrt{2} & \sin(\omega t) & \cos(\omega t) \\ 1/\sqrt{2} & \sin(\omega t - 2\pi/3) & \cos(\omega t - 2\pi/3) \\ 1/\sqrt{2} & \sin(\omega t - 2\pi/3) & \cos(\omega t + 2\pi/3) \end{bmatrix} \tag{16}$$

$$\begin{bmatrix} V_{i0} \\ V_{id} \\ V_{iq} \end{bmatrix} = Trans \begin{bmatrix} V_{ia} \\ V_{ib} \\ V_{ic} \end{bmatrix} \tag{17}$$

A rapid voltage V_{id}, V_{iq} is having both oscillation elements $\widehat{V}_{id}, \widehat{V}_{iq}$ and mean elements $\overline{V}_{id}, \overline{V}_{iq}$ with respect to unbalancing utility grid supply and harmonics conditions. The same rapid voltage V_{id}, V_{iq} is having negative sequence components and harmonics occurrences on distorted supply voltage conditions. Positive sequence is occurs on mean value of elements and zero sequence is occur on unbalancing voltage conditions. One of rapid voltages V_{id} is consist of mean value and oscillation components is given by

$$V_{id} = \overline{V}_{id} + \overline{V}_{id} \tag{18}$$

The reference voltages on load side are calculated is given by

$$\begin{bmatrix} V'_{La1} \\ V'_{Lb1} \\ V'_{Lc1} \end{bmatrix} = Trans^{-} \begin{bmatrix} 0 \\ \overline{V}_{id} \\ 0 \end{bmatrix} \tag{19}$$

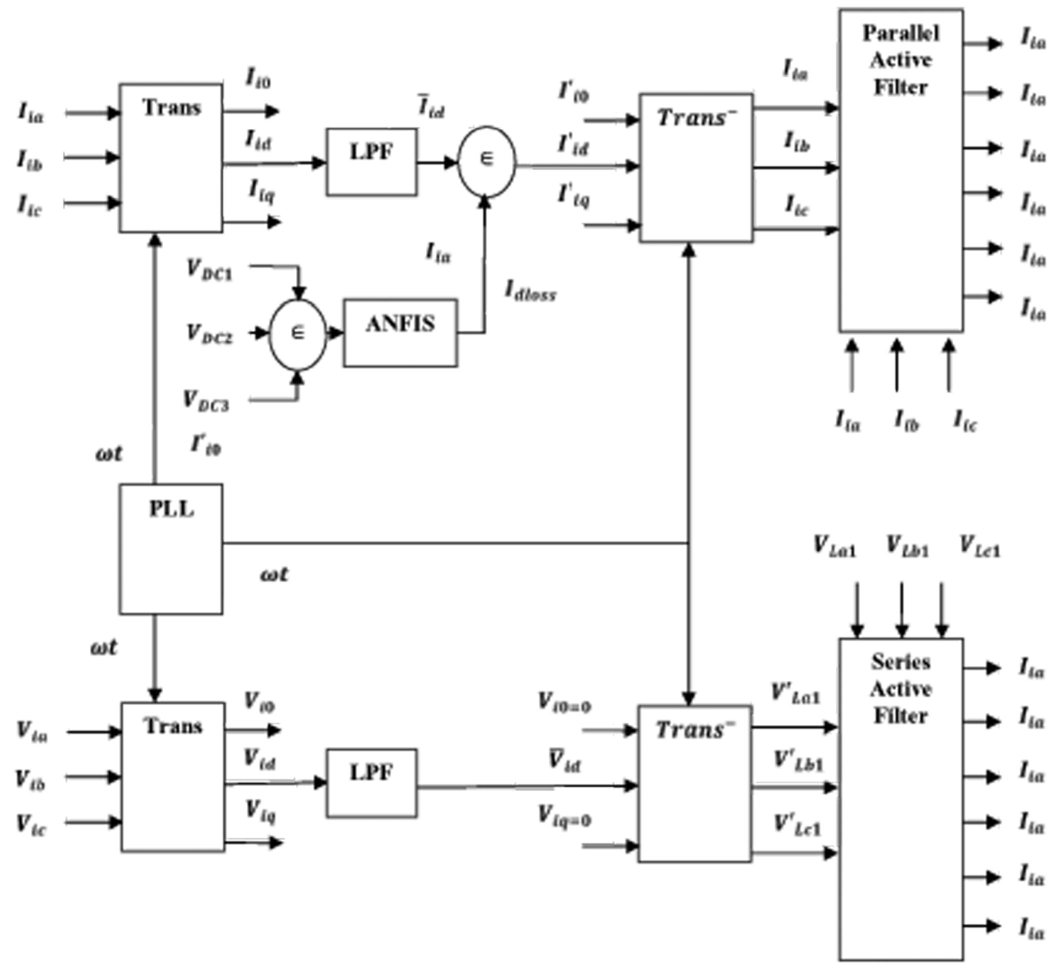


Figure 5: Proposed controller circuit diagram using ANFIS based synchronous reference frame controller

Inverse transform calculation is described on (16) is applying by mean components across supply voltage and in proposed ANFIS based SRF algorithm. Direct axis of positive sequence components voltages is calculated by low pass filters which is presented on controller circuit is shown in Fig. 5. In equation (17), zero sequence components and negative sequence components becomes zero for control and overcoming an unbalancing, distorted and harmonics on system. A sinusoidal pulse width modulation is generated by comparing generated reference signals $V'_{La1,Lb1,Lc1}$ with load voltage $V_{La1,Lb1,Lc1}$. The entire controller performance of series side converter is verified across point of common coupling (PCC).

Similarly parallel side converter controller is designed by transform and inverse transform equation is described bellow in details. Direct I_{id} and quadrature I_{iq} axis current is calculated by comparing oscillation elements $\tilde{I}_{id}, \tilde{I}_{iq}$ and mean elements $\overline{I}_{id}, \overline{I}_{iq}$ is given by

$$\begin{bmatrix} I_{i0} \\ I_{id} \\ I_{iq} \end{bmatrix} = Trans \begin{bmatrix} I_{ia} \\ I_{ib} \\ I_{ic} \end{bmatrix} \tag{20}$$

The ANFIS based synchronous reference frame controller for parallel side converter current elements of positive sequence is on direct axis elements, negative sequence components is placed on zero and quadrature axis elements for compensating unbalancing and harmonics conditions in accurate manner. Active power control is usually obtained by DC-Link capacitor control so reference voltage V'_{DC} is compared with actual DC-Link Voltage V'_{DC}. Here controlled DC-link current (*Idloss*) is obtained using ANFIS control topology. Base current components is calculated by summations of active current and controlled DC-Link Current is given as

$$I'_{id} = I_{dloss} + \overline{I}_{id} \tag{21}$$

Presented series converter control of zero and negative sequence components are set to zero as 0 and quadrature axis elements for compensating harmonics, unbalances and distorted supply utility supply conditions.

$$\begin{bmatrix} I'_{ia} \\ I'_{ib} \\ I'_{ic} \end{bmatrix} = Trans^{-} \begin{bmatrix} 0 \\ I'_{id} \\ 0 \end{bmatrix} \tag{22}$$

The calculated reference current of utility supply $I'_{ia1,b1,c1}$ is compared with $I_{ia1,b1,c1}$ for generating pulse width modulation for performing series converter operations and injection to compensating harmonics, real power and reactive power control, distorted and unbalancing utility power supply condition.

5. SIMULATION IMPLEMENTATION

In this study, 380 V_{rms} is applied as utility power supply in 5.3 *KW* capacity of series injection transformer. Parallel side injection is implemented without transformer help to tolerate power supply faults and maintain

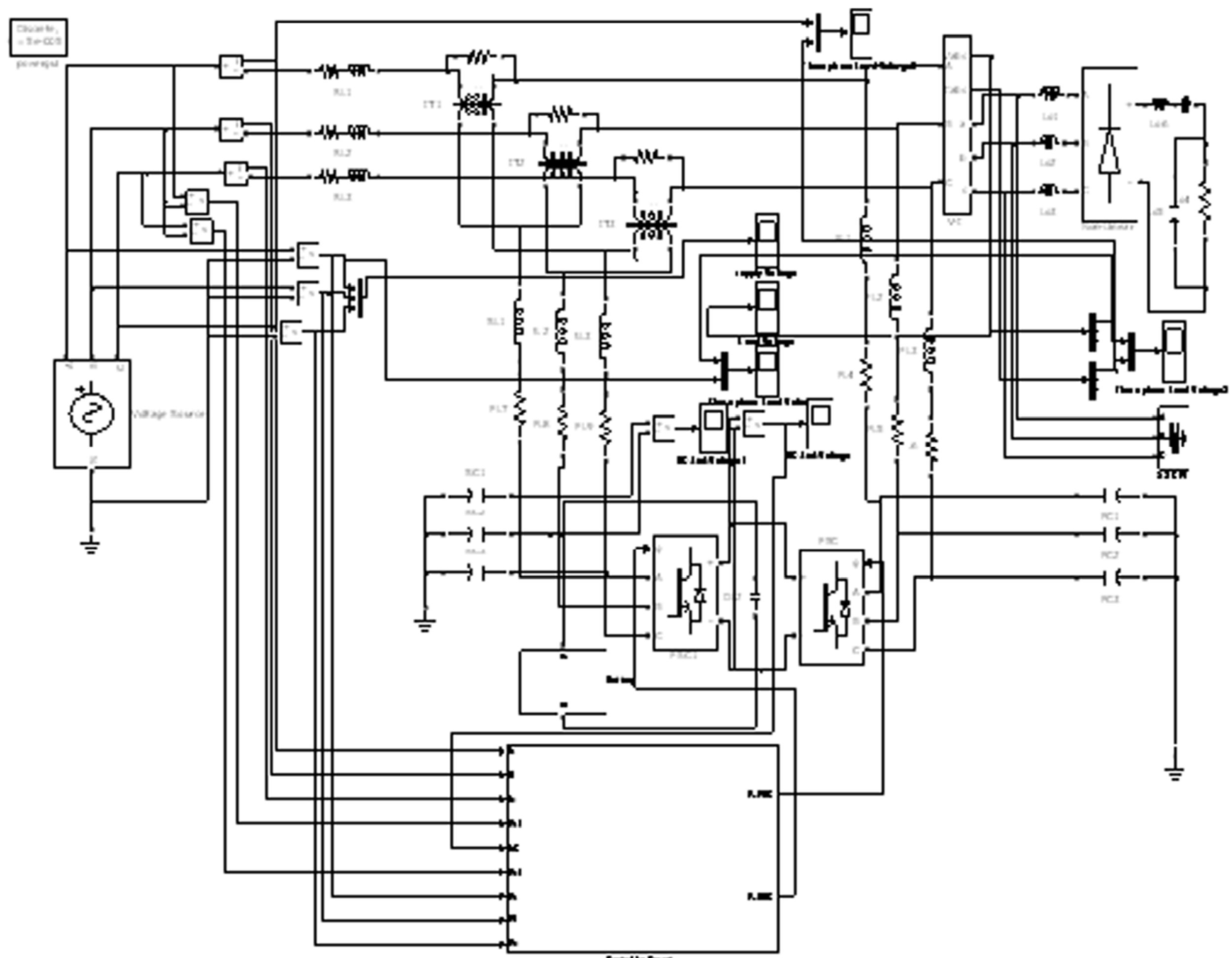
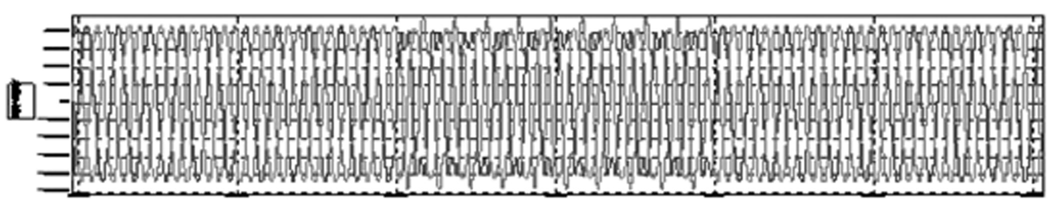


Figure 6: simulation implementation circuit

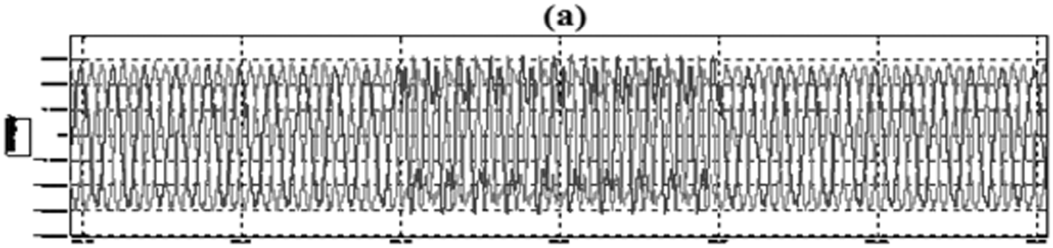
power quality across PCC (point of common coupling). Series side converter is injected using RLC filter as well as parallel side converter. Split type capacitor is used in DC-Link area to reduce range and bulky in size and controlled by adaptive fuzzy inference system controller by comparing reference DC-Link voltage V_{DC} * with actual DC-Link voltage V_{DC}. Series side converter is controller is designed by simple space vector pulse width modulation using adaptive neuro-fuzzy inference system based synchronous reference frame controller because space vector technique is most suitable method to overcome transformer-less operation of proposed UPQC system.

Table I
Parameters

	Parameters		Value
Source	Voltage	V_{iabc}	380
	Frequency	f	50Hz
Load	Three phase Line Inductance	L_{iabc}	1.47mH
	Three phase load Inductance	L_{Labc}	1.47mH
	DC Line Inductance	L_L	3.5mH
	DC Line Capacitance	C_L	10000uF
	DC resistance	R_L	500
DC Link	Voltage	V_{DC}	210
	capacitance	C_1, C_2	4700uF
Parallel Side Converter	AC Line Inductance	$L2_{abc}$	3mH
	Filter resistance	$R2_{abc}$	5Ω
	Filter capacitance	$C2_{abc}$	4.7uF
	Switching Frequency	f_{PSC}	20 kHz
Series Side Converter	AC Line Inductance	$L1_{abc}$	1.5mH
	Filter resistance	$R1_{abc}$	5Ω
	Filter capacitance	$C1_{abc}$	26uF
	Switching Frequency	f_{SSC}	12 kHz



(a)



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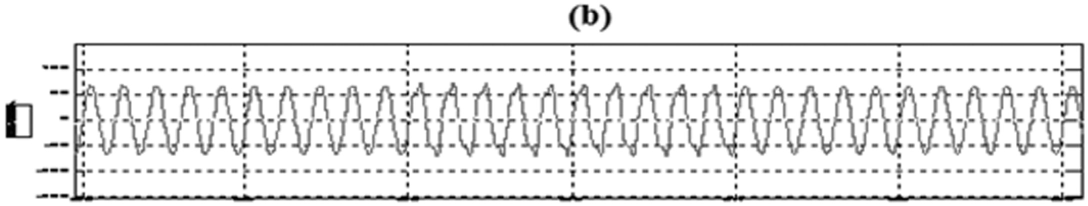

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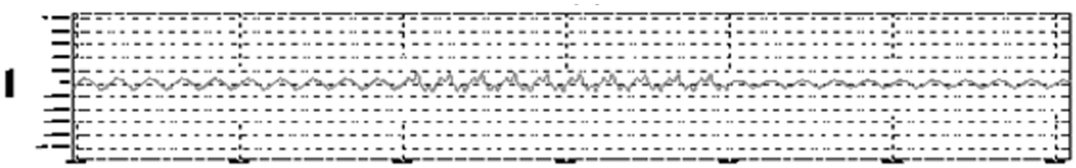
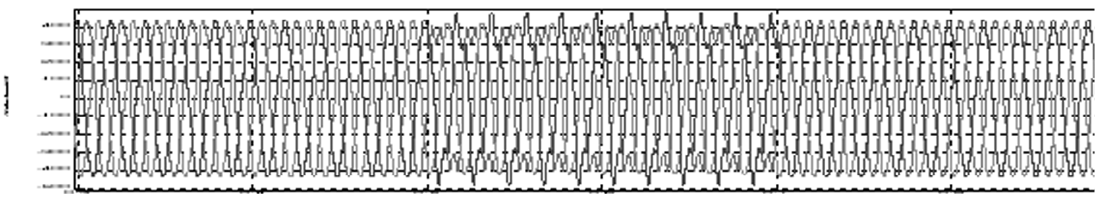


(d)

Figure 7: performance of distorted control using PI (a) distorted supply voltage (b) compensated load voltage (c) distorted supply current (d) compensated load current



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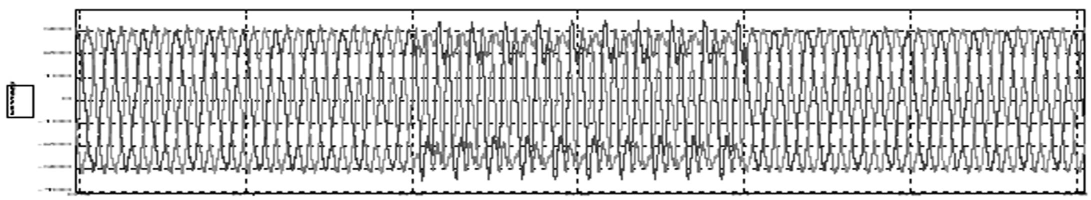

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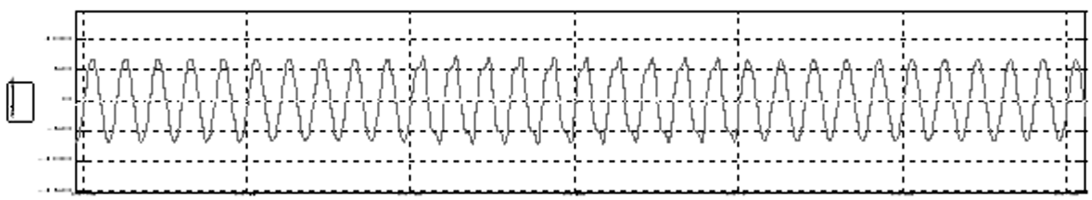

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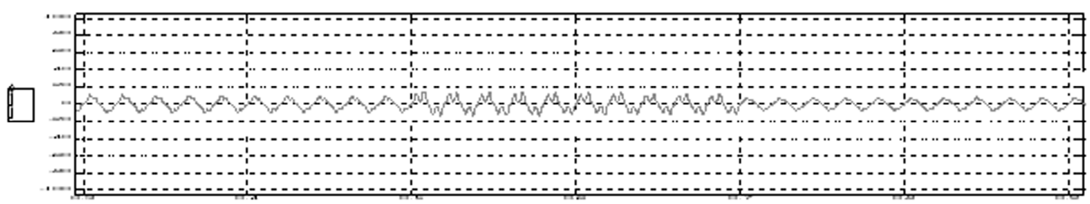
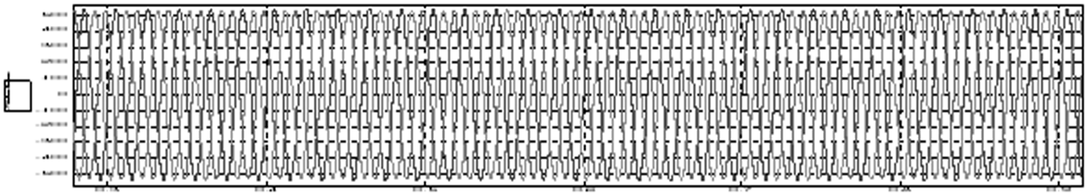


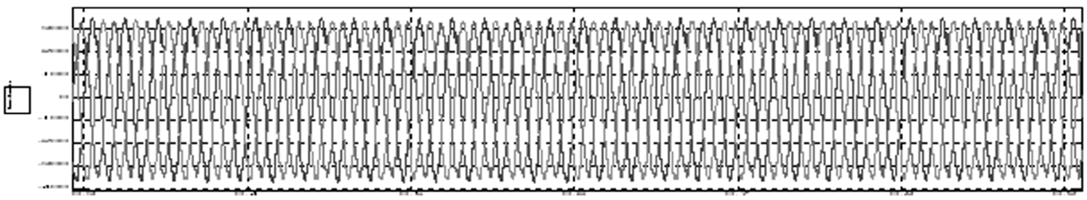
(d)

Figure 8: power performance using ANFIS (a) distorted supply voltage (b) compensated load voltage (c) distorted supply current (d) compensated load current

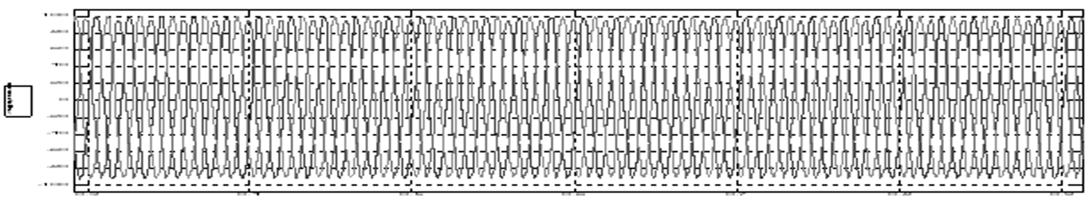
Parallel side converter is controller is designed by hysteresis band controller using adaptive neuro-fuzzy inference system based synchronous reference frame controller. The performance is analyzed under non-linear load condition in the capacity of 5.3 *KW*. Shunt side transformer-less unified power quality conditioner is developed using MATLAB/Simulink is shown in Fig. 6. The existing topology of PI controller is achieved the load performance is shown in Fig. 7. Power quality performance is greatly improved using ANFIS based synchronous reference frame controller is shown in Fig. 8 and Fig. 9. Power factor correction performance is shown in Fig.10.Total Harmonics Distortion analyses using FFT is reached in load current from 14.28% to 14.25% for existing system to proposed system respectively. Total Harmonics Distortion analysis using FFT is reached in load voltage from 10.31% to 10.20% for existing system to proposed system respectively.



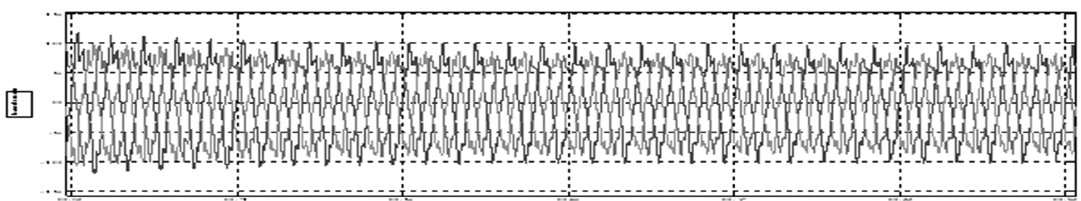
(a)



(b)

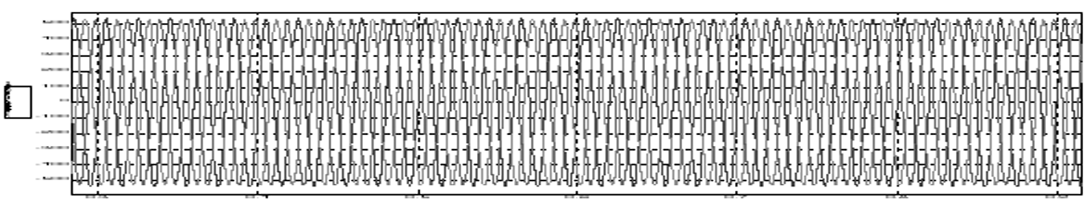


(c)

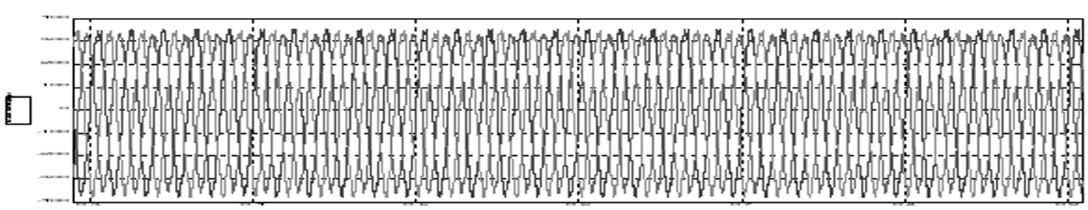


(d)

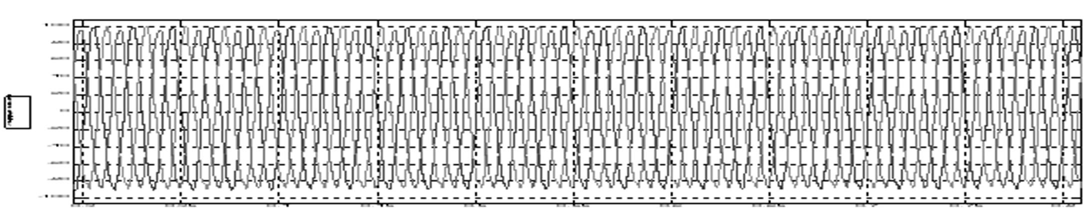
Figure 9: performance of unbalancing control using PI (a) unbalanced supply voltage (b) compensated load voltage (c) unbalanced supply current (d) compensated load current



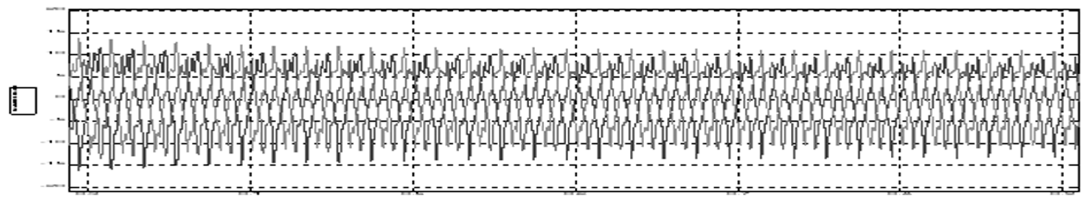
(a)



(b)

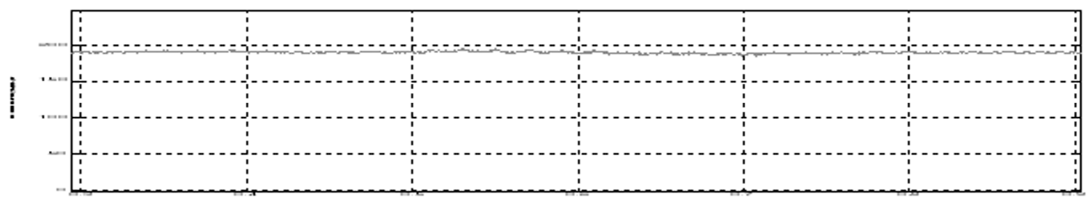


(c)

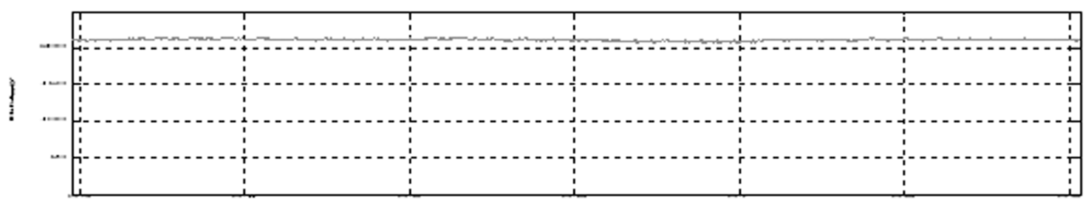


(d)

Figure 10: performance of unbalancing control using ANFIS (a) unbalanced supply voltage (b) compensated load voltage (c) unbalanced supply current (d) compensated load current

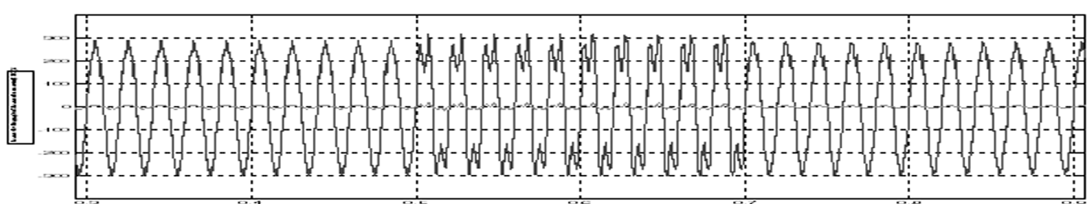


(a)

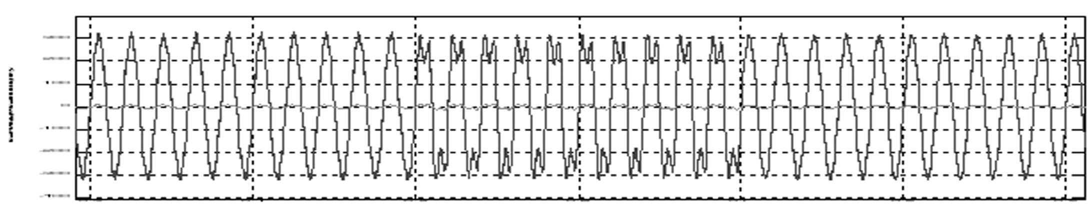


(b)

Figure 11: DC link voltage performance analysis: (a) using PI (b) using ANFIS



(a)



(b)

Figure 12: power factor correction (PFC) performance analysis: (a) using PI (b) using ANFIS

6. CONCLUSION

The present approach of transformer-less unified power quality conditioner is applied on unbalancing and distorted power supply conditions. The performed better as fault free control and power quality improvement using adequate control of parallel-series converter region. Presented adaptive fuzzy inference system based synchronous reference frame control for both series side converter and parallel side converter and also DC link voltage control is used to conserve the constant by adaptive fuzzy inference system. Presented system is compared with existing topology using PI controller and verified performance using MATLAB simulation results. Even system is having capability of low to medium power load demand but it can able to control of fault utility power supply using transformer less parallel side converter injections. The performance of power factor correction, harmonics reduction, tolerant of unbalancing and distorted supply is performed well enough to examine the presented system performance.

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