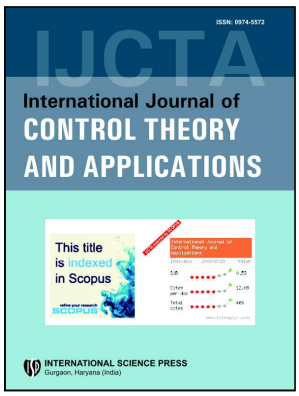

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Design of Low Power CMOS VCO with Wide Tuning Range

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Abstract: This paper presents a new design of CMOS differential voltage controlled ring oscillator (VCO) with low power and wide tuning range. A novel differential delay cell has been proposed based on dual delay path architecture. The results have been obtained in TSMC 0.18µm CMOS technology with supply voltage 1.8V. The proposed VCO achieves a controllable frequency range from 1.803 GHz to 4.231 GHz with a tuning range of 80.4%. The control voltage (V_c) has been varied from 0.1V to 1V for obtaining the different output frequencies. The power dissipation of proposed VCO is 4mW at a control voltage of 1V. Power dissipation and output oscillation frequency range of proposed VCO has been compared with earlier reported circuits and proposed VCO shows improved performance.

Keywords: Differential Delay Cell, Dual Delay Path Technique, Low Power, Phase Locked Loop, Tuning Range, VCO

1. INTRODUCTION

In recent years, the high speed and low power consumption are the major design issues in portable electronic devices (PEDs). Complementary metal oxide semiconductor (CMOS) based integrated circuits (ICs) are widely used for various battery operated applications such as portable communication devices, mobile phones, sensor networks etc. Voltage controlled oscillators are widely used in phase locked loop (PLL) for, clock generation, frequency synthesizer, and recovery circuits for the microprocessor and wireless communication systems [1-4]. A PLL is a closed loop control system consisting of a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage controlled oscillator (VCO) and a frequency divider (FD). The block diagram of a PLL system is shown in figure 1.

VCO consumes the majority of power in the PLL system. The design of low power VCO circuit is very critical for low power PLL system. The output frequency of a VCO is the linear function of its input control voltage [5].

$$f_{out} = f_o + K_{vco} V_c \tag{1}$$

where f_0 represents the output frequency corresponding to $V_c = 0$ and K_{vco} is the gain of VCO. There is a tradeoff between the phase noise of the VCO and its frequency range [1], [6]. With the increase in its gain, the output

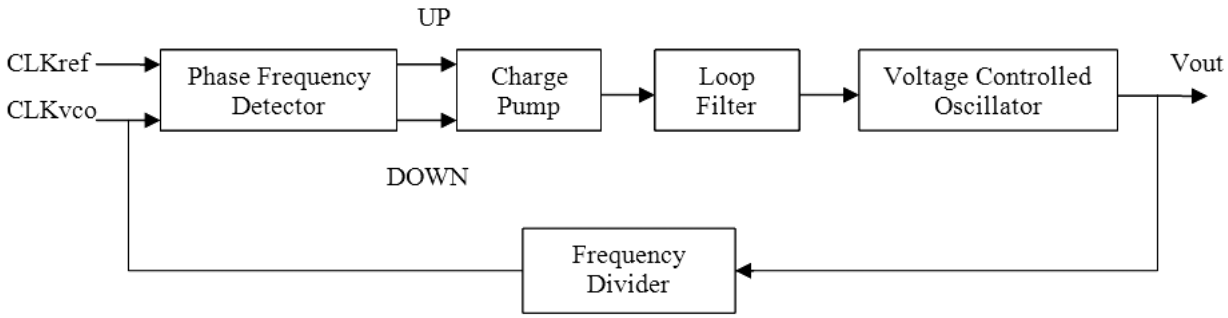

Figure 1: Block diagram of a PLL system

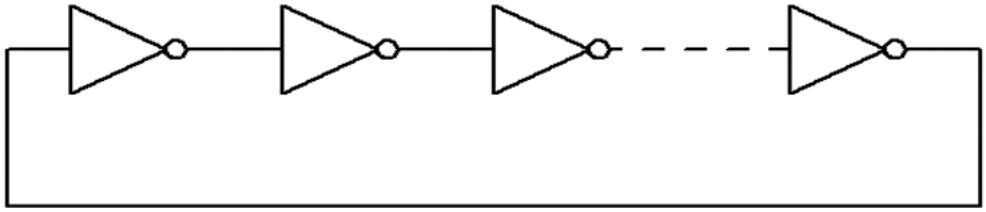

Figure 2: Block diagram of single ended N-stage ring VCO

frequency increases as per equation (1) and consequently, the phase noise performance of VCO degrades. Two types of oscillators are widely used in the majority of the PLL designs, i.e. ring oscillator and LC oscillator [7]. In a ring oscillator, the delay cell can be single-ended or differential. A number of delay cells must be odd in a single ended ring oscillator which is composed of a chain of inverters of PMOS and NMOS transistors. In the differential ring oscillator, the number of delay cells can be odd or even. Differential delay cells can be constructed by using either an active load or with a passive load having a pair of NMOS differential input or push-pull inverter [8]. The propagation time of delay cells is set by the charge present at every node and the current passing through the load. The block diagram of a single ended N delay stage ring VCO is shown in figure 2. For generating the oscillations, ring oscillator must provide unity voltage gain and a phase shift of 2π [5].

Voltage controlled ring oscillator has wide frequency range and compatible with digital CMOS technology and occupies significantly less area than LC oscillators [9-10].

Figure 3 shows the basic model of an LC oscillator. LC VCOs have superior phase noise performance but normally need on-chip inductors, which occupy large silicon area and ability to operate at higher frequencies [11-13]. Its resonant frequency is given as follows

$$\omega_o = \frac{1}{2\pi\sqrt{LC}} \tag{2}$$

The quality factor, Q of an LC tank circuit is given by

$$Q = 2\pi \frac{Energy\ \ Stored}{Energy\ \ Dissipated\ \ Cycle} = \frac{R}{\omega L} \tag{3}$$

The higher quality factor Q means lower VCO phase noise. A good phase noise model is the main key to minimize the phase noise in VCO design.

The major challenge in the design of VCO is to obtain high-output oscillation frequency, lower phase noise along with minimum power dissipation. Overall power consumption of PLL can be reduced mainly by minimizing

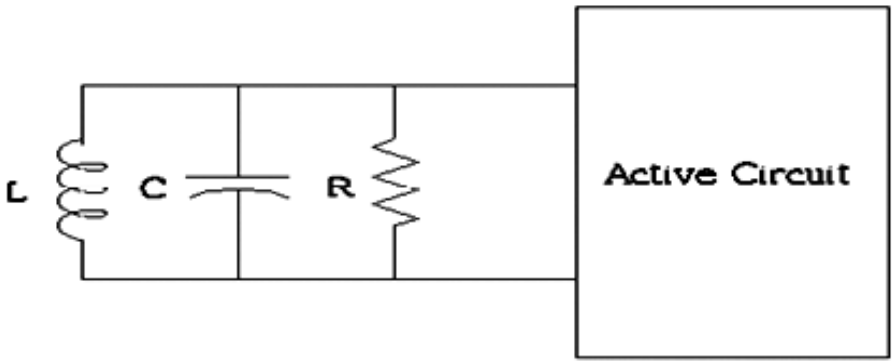

Figure 3: Model of LC oscillator

the power consumption in VCO circuit. The delay cell is the key component in any VCO design and improvement in its design will automatically enhance the overall performance of the VCO. In this paper, a differential delay cell is reported and a four stage differential VCO with reduced the power dissipation and wide output oscillation frequency has been proposed.

2. PROPOSED VCO DIRCUIT DESIGN DESCRIPTION

2.1. Architecture of High Speed Ring Oscillator with Dual delay Paths

In a ring oscillator, only a supply voltage is required to operate. The oscillation initiates when the supply voltage is greater than a certain threshold level. For the fixed supply voltage, the output frequency of ring oscillator is determined by the propagation delay of each delay cell and number of delay cells connected in the closed loop. If the number of delay cells connected in the closed loop is fixed, the propagation delay of each cell is varied by applying the different control voltage, V_c at the control input of VCO as shown in figure 4. In a ring oscillator, the output oscillation frequency can be derived as [9]:

$$f_{osc} = \frac{1}{t_d N} \tag{4}$$

Here, f_{osc} is the oscillator frequency, t_d is the propagation delay of the each delay cell and N is the number of stages of the delay element. In this paper, VCO having four stages have been used to attain full signal delay and signal delay has been feedback to VCO input. The delay time constant, t_d of each cell is

$$t_d = RC_{load} \tag{5}$$

where R is the equivalent load resistance and C_{load} is the total load capacitance at the output node. The equation (4) can be written as

$$f_{osc} = \frac{1}{2RC_{load} N} \tag{6}$$

When I_d is the load current and V_{dd} is the supply voltage then the above expression can be written as

$$f_{osc} = \frac{I_d}{2NV_{dd}C_{load}} = \frac{2\mu C_{ox}\left(\frac{W}{L}\right)_{3,4}\left(V_{gs} - |V_{THp}|\right)}{2NV_{dd}C_{load}} \tag{7}$$

Therefore, the frequency of the oscillator depends on the delay time of each delay element. The delay time cannot be lesser than that of a single inverter which gives rise to frequency limitation problem [14]. Hence, the maximum oscillation frequency of the VCO is controlled by the delay time of the simple inverter delay cell. Skewed delay design is used to eliminate this frequency limitation problem. Figure 4 shows the architecture of VCO with dual delay path technique. The VCO structure uses the even stage skewed dual delay path design which facilitates higher operating frequency and wider frequency tuning range [15-17]. The skewed signal is taken from outputs of two stages before the existing delay cell. This skewed signal is used to turn ON the PMOS prematurely during output transition. This compensates the performance of PMOS transistor which is generally slower than NMOS transistor. PMOS transistor M_5 or M_6 (figure 5) will pre-charge the output node of the delay cell. As a result, the output node of the delay cell can charge to high voltage faster and can attain higher oscillation frequency. The rise time of the output signal shows reduction with the use of this technique. When the skewed signal increases, the power dissipation and speed also raise. Further, the increment in skewed signal decreases the speed of the VCO due to direct path formation between the power supply and ground**.** To acquire higher oscillation frequency with acceptable power consumption the skewed delay should be small compared with the total period [18]. In figure 4, the normal delay paths are shown by thick lines and skewed path are represented as dotted lines.

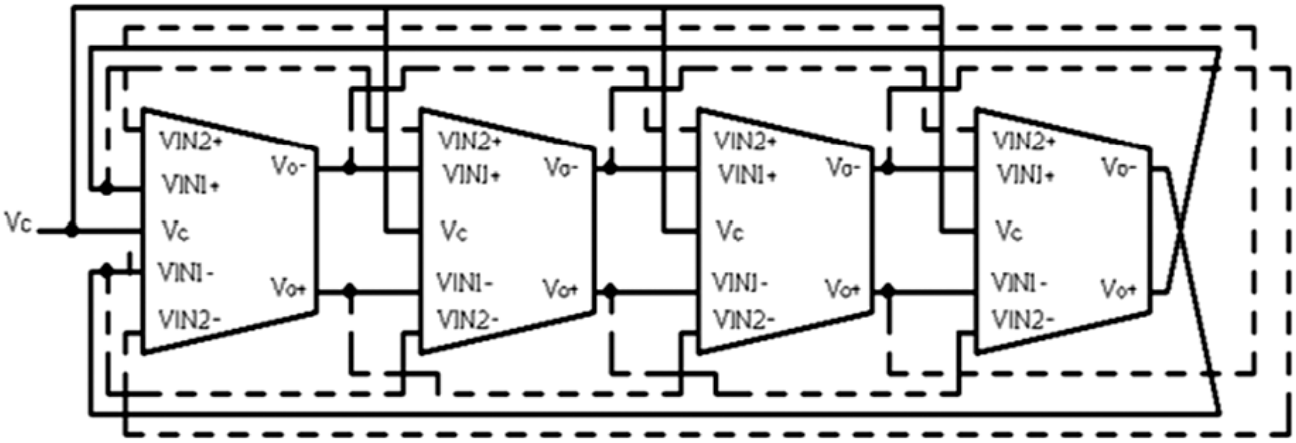

Figure 4: Four stage VCO ring oscillator structure with dual delay path

Total power consumption for a differential ring oscillator is given by

$$P = NI_d V_{dd} \tag{8}$$

The voltage controlled ring oscillator consists of N stages delay cells which are changed by the control voltage V_c. For satisfy both power consumption and finest performances of oscillation frequency N can be chosen [8]. The number of delay cells N increases, for a fixed supply voltage V_{dd}, the current I_d to all delay cell must decrease to convince the power requirements. However, the higher oscillation frequency can be obtained by minimizing gate area, which can be attained by reducing the number of delay stages, leading to less gate capacitance.

2.2. Proposed Delay Cell

The schematic of the proposed four input differential delay cell is shown in figure 5. In this delay cell, differential input block consists of two NMOS transistors M_1 and M_2 acting as primary input pair. A pair of PMOS transistors M_5 and M_6 has been added to the PMOS loads of delay cell. These additional transistors serve as secondary input pair to take negatively skewed signal. The output frequency can be controlled by the

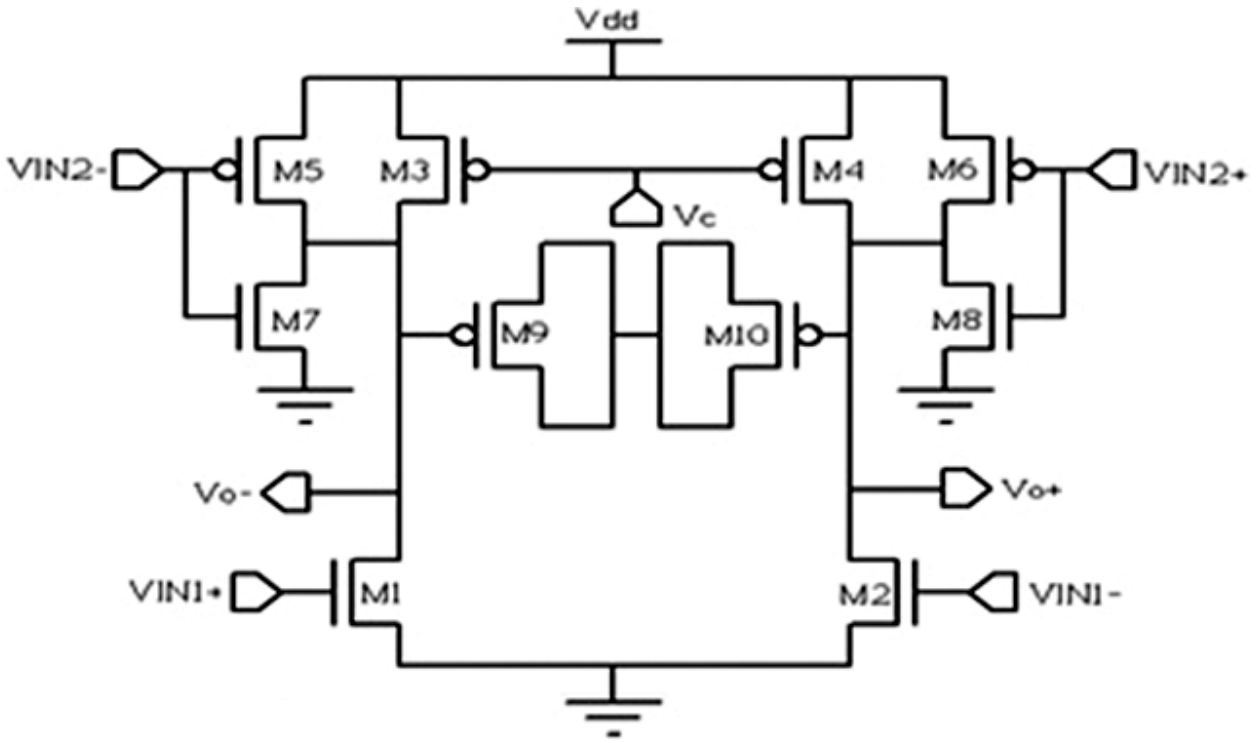

Figure 5: Proposed differential delay cell

variation of the control voltage at the gate of the PMOS load transistor M_3 and M_4. With the decrease in control voltage (V_c), the value of resistance decreases which decreases the time constant of the delay cell. As a result, the frequency at the output node increases. Moreover, with an increase in the control voltage (V_c), the value of the resistance increases resulting in the lower output frequency. When V_{IN+} is lower than V_{THn}, M_1 transistor turns off. Since the input voltage at M_5 arrives earlier than M_1, therefore transistor M_5 start conducting. As a result, the output node charge lower to higher voltage and this operation reduces the rise time at the output node. A pair of NMOS transistor M_7 and M_8 are added to the secondary input. These are used to pre-discharge the output nodes which reduces the rise time as well as fall time of the output node. The output frequency of the proposed VCO is higher due to pre-discharge operation. A pair of PMOS transistor M_9 and M_{10} are used as the capacitive load at the output node of the delay cell which increases the tuning range of the VCO.

3. RESULTS AND DISCUSSION

The ring VCO with a four stage proposed delay cell has been simulated in TSMC 0.18µm CMOS technology with control voltage variation from 0.1V to 1V. Figure 6 shows the output waveform of proposed VCO at control voltage 0.1V and supply voltage 1.8V. Table 1 shows the impact of the control voltage on the output frequency and power dissipation. The variation in the frequency range with the change in control voltage (V_c) and supply voltage (V_{dd}) is shown in figure 7. As supply voltage decreases, the output frequency and power consumption decrease. The frequency range varies from 1.803 GHz to 4.231 GHz with a tuning range of 80.4% at a supply voltage of 1.8 V. The proposed VCO consumes power in the range of 4 mW to 10.8 mW with the corresponding variation of the control voltage from 0.1V to 1V. Figure 8 shows the relationship between control voltage and power dissipation. It has been observed from the results that with a decrease in control voltage, the output frequency, and power dissipation are increased. Table 2 shows the comparison of proposed VCO results with existing VCOs which are reported in literature earlier.

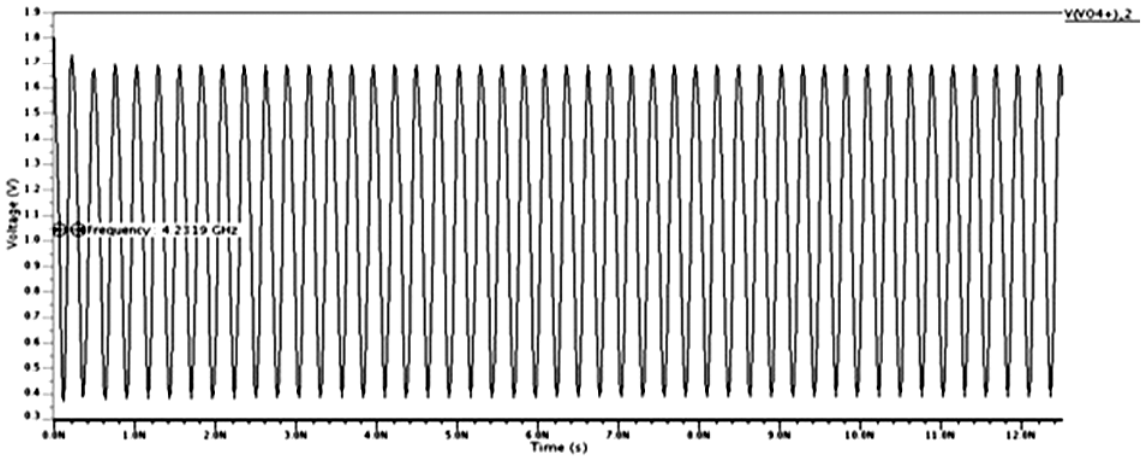

Figure 6: Output waveform of VCO

Table 1
Simulation results of VCO

	Vdd = 1.8V		*Vdd = 1.7V*		*Vdd = 1.6V*		*Vdd = 1.5V*		*Vdd = 1.4V*	
Control Voltage (Vc)	*Output Frequency (GHz)*	*Power Dissipation (mW)*	*Output Frequency (GHz))*	*Power Dissipation (mW)*	*Output Frequency (GHz)*	*Power Dissipation (mW)*	*Output Frequency (GHz))*	*Power Dissipation (mW)*	*Output Frequency (GHz)*	*Power Dissipation (mW)*
0.1V	4.231	10.856	3.650	8.805	3.487	7.098	3.358	5.600	2.971	4.301
0.2V	3.784	10.130	3.255	8.097	3.025	6.395	2.926	4.914	2.493	3.649
0.3V	3.399	9.306	2.856	7.292	2.660	5.611	2.552	4.165	2.103	2.953
0.4V	3.021	8.417	2.555	6.453	2.337	4.830	2.216	3.449	1.785	2.311
0.5V	2.706	7.521	2.260	5.646	2.075	4.104	1.947	2.809	1.523	1.759
0.6V	2.427	6.669	2.034	4.897	1.843	3.451	1.737	2.255	1.324	1.310
0.7V	2.264	5.882	1.839	4.221	1.675	2.880	1.545	1.795	1.187	0.980
0.8V	2.044	5.170	1.700	3.626	1.544	2.401	1.427	1.448	1.081	0.795
0.9V	1.910	4.544	1.597	3.123	1.4453	2.033	1.325	1.248	1.046	0.739
1.0V	1.803	4.011	1.493	2.734	1.361	1.817	1.279	1.185	1.014	0.730

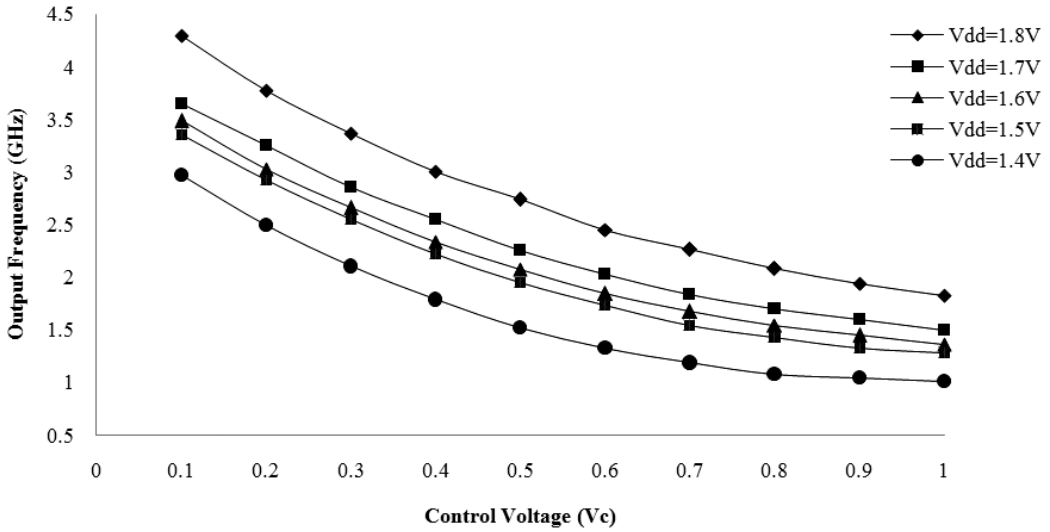

Figure 7: Measured frequency verses control voltage

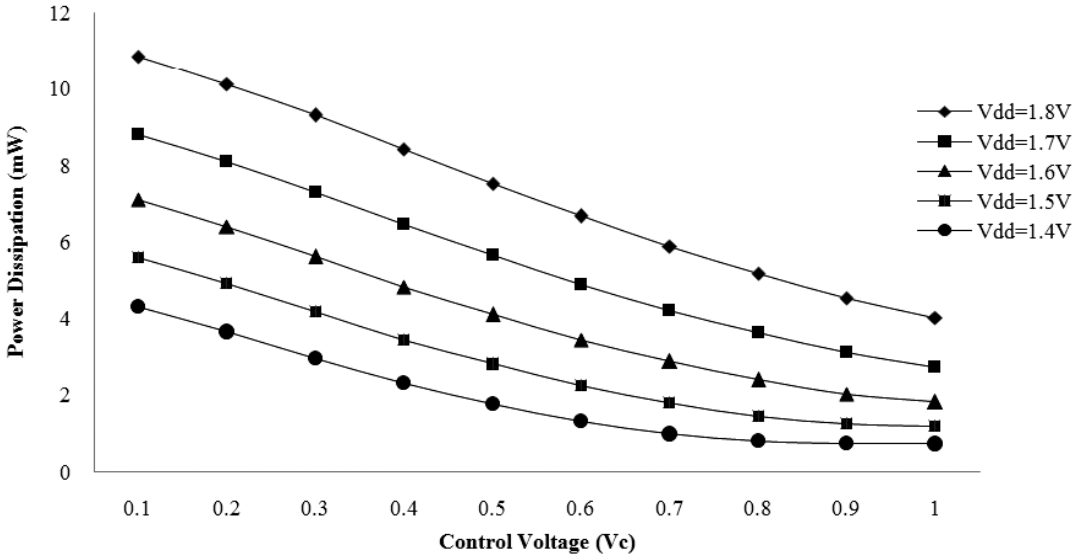

Figure 8: Measured power dissipation verses control voltage

Table 2
Comparison of ring VCO performance

References	*CMOS Process (μm)*	*Supply Voltage (V)*	*Oscillation Frequency (GHz)*	*Tuning Range in % (GHz)*	*Control Voltage (V)*	*Power Dissipation (mW)*
[1]	65 nm	1.2	0.48–1.1	78	0.2–1.2	3.84
[2]	0.18 μm	2	0.523 – 2.11	49.4	0–3	14.8
[4]	0.5 μm	3	1.3–1.8	32.25	——	23
[9]	0.18 μm	1.8	3.03 –5.36	43.39	0–1.8	100
[10]	0.18 μm	1.8	——	18	- 0.8–0.2	12.6
[12]	0.18 μm	1.8	2.5–5.2	74	- 0.4–0.4	17
[13]	0.18 μm	1	0.479– 4.09	88.29	0–1	13
[14]	0.6 μm	3	0.75–1.2	50	1–2.6	30
[16]	65 nm	1	0.4 –1.01	115	0–0.8	10
[17]	0.18 μm	1.8	1.77 –1.92	8.13	0–2	13
Proposed work	0.18 μm	1.8	1.8–4.2	80.4	0.1–1	4–10.8

4. CONCLUSION

The CMOS ring VCO with a four stage proposed delay cell has been simulated in TSMC 0.18mm CMOS technology. In proposed differential delay cell, a pair of NMOS transistors M_7 and M_8 is added to secondary inputs and a pair of PMOS transistor M_9 and M_{10} are used to as capacitive load at the output node to increase the frequency and tuning range of VCO. The structure of the VCO utilizes dual delay path techniques to achieve high oscillation frequency and a wide tuning range. VCO achieves a controllable frequency range from 1.803 GHz to 4.231 GHz with a tuning range 80.4%, with the variation in control voltage from 0.1V to 1V keeping supply voltage at 1.8V. The proposed VCO dissipates a power of 4 mW at a control voltage of 1V. The proposed VCO design has been compared with previously reported design and the present approach shows significant power saving with high oscillation frequency.

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