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DC Link Capacitor Voltage Balance and Neutral Point Stabilization in Diode Clamped Multi Level Inverter

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Abstract : Diode clamped multi level inverters are widely used topology of multilevel inverters in medium voltage and high power applications. Diode clamped multilevel inverters has an inherent problem which is neutral point voltage fluctuation caused by DC link capacitor voltage unbalance. Using sine PWM phase shift technique neutral point voltage is stabilized for three level diode clamped multilevel inverter but for higher level inverter individual capacitor voltage balance is needed. This paper presents a new control circuit which balance capacitor voltages, unlike other control method this control circuit works effectively under different load and fault conditions. The proposed controlled system is implemented in MATLAB and simulations results are conducted for various loads.

Keywords : Diode-Clamped Multilevel Inverter (DCMLI)/Neutral Point Clamped (NPC) Inverter, Equalizing Circuit, Bias Value (B), Sinusoidal Pulse Width Modulation (SPWM), Total Harmonic Distortion (THD).

1. INTRODUCTION

Multilevel inverters continue to receive more and more attention because of their high power operation capability, high efficiency, low switching losses and low output of Electro Magnetic Interference (EMI). Nowadays, multilevel inverters are becoming increasingly popular in power applications, as multilevel inverters have the ability to meet the increasing demand of power rating and power quality associated with reduced harmonic distortion and lower electromagnetic interference. A multilevel inverter has several advantages over a conventional two-level inverter that uses high switching frequency pulse width modulation (PWM). The most attractive features of a multilevel inverter are as follows:

1. They can generate output voltages with extremely low distortion and lower dv/dt.
2. They draw input current with very low distortion.
3. They generate smaller common-mode (CM) voltage.
4. They can operate with a lower switching frequency.

There are three types of multi level inverters: Diode clamped multilevel inverter, Flying capacitor multilevel inverter, Cascaded inverter with separate DC sources. Out of these three multilevel inverters diode clamped multilevel inverter is best suited for voltage stabilization. Whereas flying capacitor type inverter can be more effective Also, pre charging all of the capacitors to the same voltage level and startup are complex compared to diode clamped multilevel inverter. Compared to cascaded multilevel inverter diode clamped is simple and easy to operate. In cascaded multilevel inverter many voltage sources are required of same dc value. Even though diode clamped multi level inverter (DCMLI) is best suited for

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voltage stabilization it has its disadvantages [2]. DCMLI is also called neutral point clamped (NPC) inverter because of an added neutral point level. For more than three level NPC inverter, by SPWM scheme neutral point voltage is balanced. But the DC link capacitor voltage is not balanced effectively. This is due to non-uniform power drawn from the capacitors resulting in fall of some and raise of other capacitor voltages. Another control circuit is proposed in this paper for controlling and balancing individual capacitor voltages and also balancing neutral point voltage. This control circuit is most effective for different loads and fault conditions.

2. DIODE CLAMPED MULTILEVEL INVERTER

DCMLI can convert a single DC source to AC output of any number level, with increase in level the AC output is nearly sinusoidal and also THD decreases.

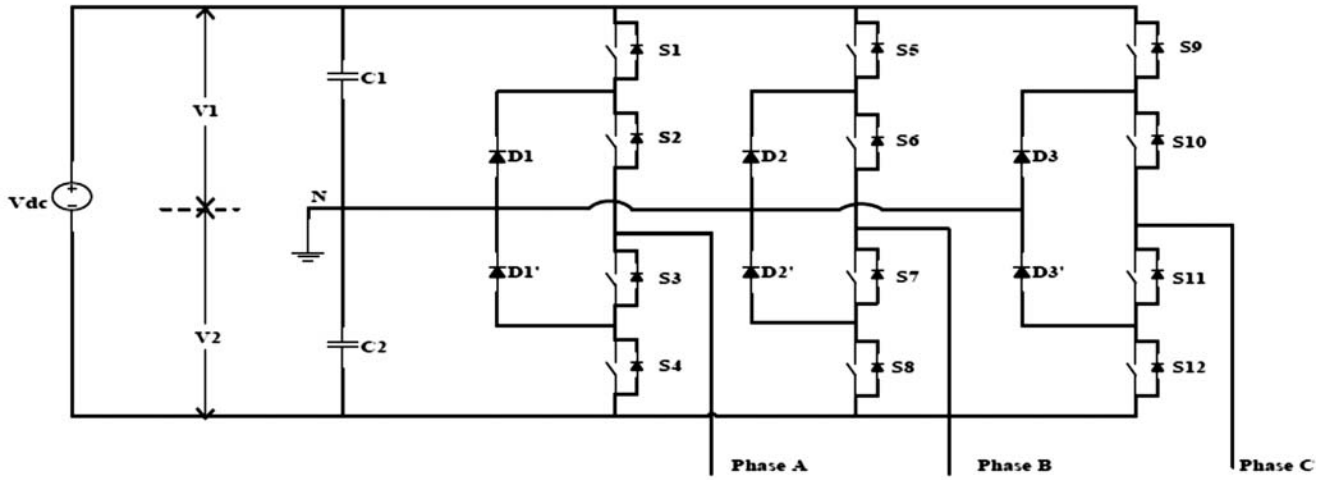

Fig. 1. NPC three-level inverter.

In the SPWM scheme for two-level inverters, each reference phase voltage is compared with the triangular carrier and the individual pole voltages are generated, independent of each other. The SPWM technique, for multilevel inverters, involves comparing the reference phase voltage signals with a number of symmetrical level-shifted carrier waves for PWM generation. In an '*m*' level inverter (*m*-1) number of DC link capacitors and carrier wave forms. 2(*m*-1) switching devices and (*m*-1)*(*m*-2) diodes are required in each arm of the inverter. The schematic diagram of NPC three-level inverter is shown in the figure 1. Each arm in three level inverter creates three voltage levels $\frac{+v_{dc}}{2}, 0, \frac{-v_{dc}}{2}$. The diodes used are called clamping diodes connected to midpoint of capacitors, each capacitor will block the voltage rated where *m* is the level of the inverter.

Table 1. Switching States of Three-Level Inverter for Phase A.

S.No.	*Arm switches*				*Output Voltage*
	S1	*S2*	*S3*	*S4*	
1.	1	1	0	0	$\frac{+v_{dc}}{2}$
2.	0	1	1	0	0
3.	0	0	1	1	$\frac{-v_{dc}}{2}$

The possible pole voltages for each arm of three-level inverter are :

$$V_{AN} = \frac{\pm v_{dc}}{2}, 0 : V_{BN} = \frac{\pm v_{dc}}{2}, V_{CN} = \frac{\pm v_{dc}}{2}, 0$$

For five-level NPC inverter:

$$V_{AN} = \frac{\pm v_{dc}}{4}, \frac{\pm v_{dc}}{2}, 0 : V_{BN} = \frac{\pm v_{dc}}{4}, \frac{\pm v_{dc}}{2}, 0 : V_{CN} = \frac{\pm v_{dc}}{4}, \frac{\pm v_{dc}}{2}, 0$$

Line voltages are:

$$V_{AB} = V_{AN} - V_{BN} : V_{BC} = V_{CN} : V_{CA} = V_{CN} - V_{AN} \quad (1)$$

SPWM modulation scheme is most widely used method to generate gating signals. It is very simple and easy to implement by using digital technique. In SPWM switching pulses are generated by comparing a sinusoidal reference wave with vertically shifted triangular carrier waveforms. For '*m*' level inverter (*m*-1) triangular carrier waveforms are required to generate (*m*-1) level output voltage. All the carrier triangular waves have same frequency and amplitude. The carrier wave frequency is very high compared to reference wave frequency.

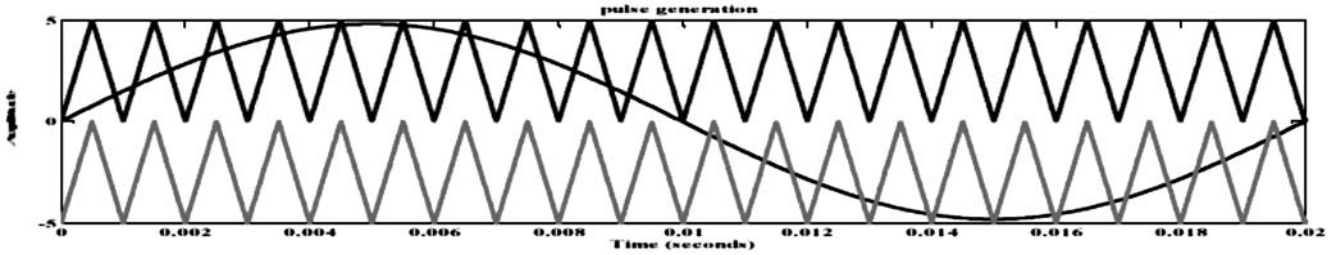

Fig. 2. SPWM scheme for NPC Three level inverter.

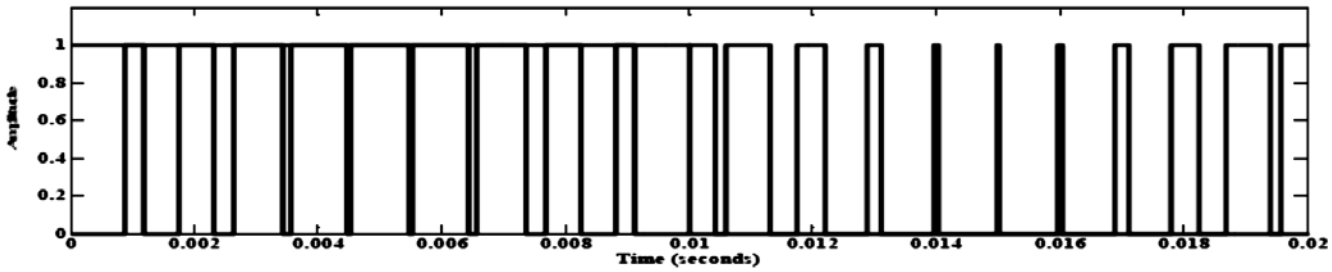

Fig 3. Pulses generated in the SPWM scheme.

When reference wave is greater than carrier wave the corresponding switch is ON. Here, when reference wave is greater than upper carrier wave S1 switch is ON and S3 is OFF. In contrast if reference wave is greater than lower carrier wave S2 is ON and S4 is OFF. In this scheme three reference sinusoidal waves each shifted with $_{120^0}$ are used to compare level shifted carrier waves to generate gating signals. Modulation index used in this paper is less than 0.98.

$$\text{Modulation index (MI)} = \frac{A_r}{A_c}[3] \quad (2)$$

Where,

A_r – Reference signal amplitude, A_c – carrier signal amplitude.

The voltage difference of upper half (positive part) and lower half (negative part) of a arm (leg) should be zero *i.e*. neutral point voltage should always remains zero (From Fig. 1, V1 and V2 are upper half and lower half voltages with respect to neutral point) for stabilization. Control technique proposed in [3] is modified in this paper. When neutral point voltage is positive means the upper half voltage is greater than lower half voltage in a DC link. To balance the ON time period of switches in lower leg should be less than

the ON time period of upper switches in a leg so that upper capacitor discharges. Hence, whenever neutral point voltage becomes unbalance it needs to shift reference wave in the same direction. If neutral point voltage is positive then reference wave is shifted in positive direction. If neutral point voltage is negative then reference wave is shifted in negative direction. This is done by adding bias value to the reference wave. Table III gives selection of bias value with respect to neutral point voltage, here when neutral point voltage is zero then no bias value is added.

Table 2. Selection of the bias value

V1-V2	***Bias Value***
Positive	Positive
Negative	Negative
0	0

3. DC LINK CAPACITOR BALANCE CONTROL CIRCUIT

For higher level (more than three level) NPC inverter SPWM scheme is effective for controlling neutral point voltage. *i.e*. upper and lower half arm voltage balance can be done but the individual capacitor balance is not possible. For '*m*' level inverter each capacitor needs to block $\frac{v_{dc}}{m-1}$ voltage in general. The NPC inverter with more than three level the individual capacitor voltage is unbalanced, as the time progress in a arm complete upper half voltage $\frac{v_{dc}}{2}$ is blocked by top capacitor which is connected to positive terminal of DC source voltage and complete lower half voltage is blocked by lower capacitor connected to negative terminal of Dc voltage source. Schematic diagram of five level NPC inverter is shown in fig 4.

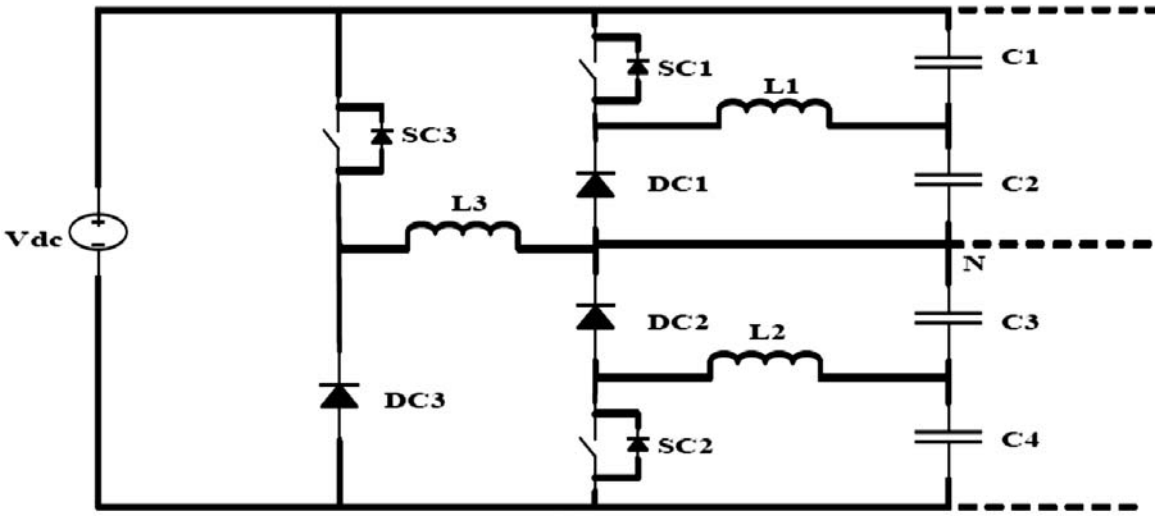

Fig. 4. Capacitor voltage balance control circuit diagram.

As shown in Fig. 4, the four capacitors should block $\frac{v_{dc}}{4}$ each but the capacitor C1 blocks $\frac{+v_{dc}}{2}$ and lower most capacitor C4 blocks $\frac{-v_{dc}}{2}$.The middle capacitors C2 and C3 blocks almost zero voltage. This results in bad quality voltage outputs. The switches are over rated hence damage of equipment occurs results in collapse of NPC inverter. This problem can be solved by balancing each capacitor with its

respective voltage. A control circuit is proposed in this paper to balance individual capacitor voltage. Fig 5 shows control circuit diagram for DC link capacitor balance, in this consider the positive half of an arm, whenever the upper capacitor C1 blocks more than $\frac{v_{dc}}{4}$ voltage then the controller switches on the switch SC1 to transfer the extra energy to L1. When the capacitor C1 is balanced this inductor discharges its energy to C2 through a diode D1 and balances both the capacitors to $\frac{v_{dc}}{4}$. Same control circuit operation is applied to negative half of the arm. Here whenever lower capacitor C4 blocks less than $\frac{-v_{dc}}{4}$ voltage, control circuit comes into action and charges inductor L2. Now the whole upper half of the arm and lower half of the arm of five-level NPC inverter can be controlled through the application of same control circuit. Therefore neutral point voltage is balanced. Here, whenever upper arm capacitors voltage is greater than $\frac{v_{dc}}{2}$ Voltage the extra energy deviates through the switch SC3 and charges inductor L3. After balancing upper arm voltage the stored energy in L3 discharges to lower arm capacitors.

In this way both upper and lower half capacitor voltages are balanced and the difference between them is always zero i.e. neutral point voltage is balanced.

4. RESULTS AND DISCUSSION:

The control strategy of DC link capacitors voltage balance of DCMLI is implemented using MATLAB Simulink toolbox. The DC source voltage of 400 V and DC link capacitors of 4940μF is used.

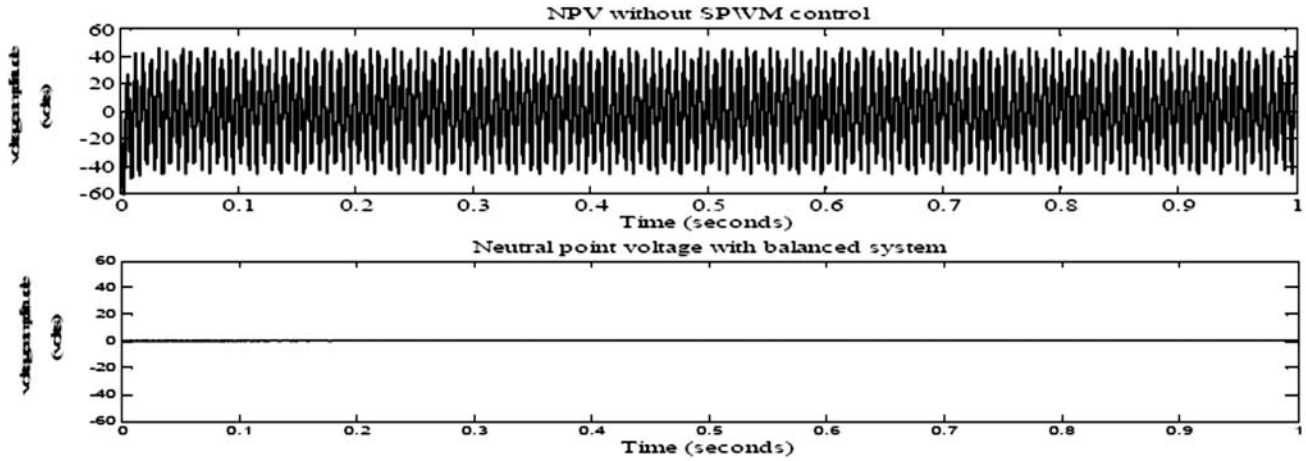

Fig. 5. Neutral point voltage without and with SPWM control scheme.

From fig 6., It has seen that without sine PWM control scheme neutral point voltage varies with wide range of –40 to + 40. With sine PWM scheme it has improved to -0.5 to 0.5

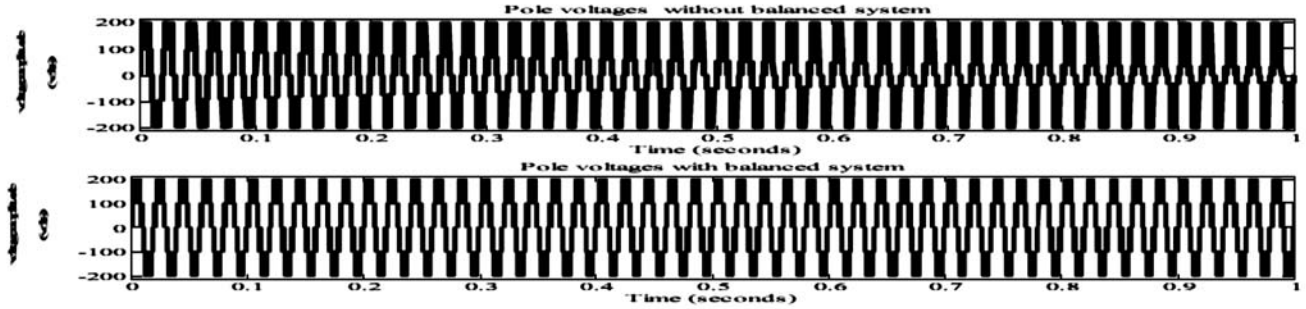

Fig. 6. Pole voltages of five level inverter without and with DC link capacitors control circuit

Fig 7 shows pole voltages of five level inverter, without capacitor control circuit voltage level deviates and devices needs to block more voltage which results in equipment damage. With capacitor control circuit the levels are balanced as capacitors are balanced.

Table 3. Neutral point voltage differences in three level DCMLI without and with sine PWM scheme

S.NO	*LOAD*	*NPV without sine PWM scheme*	*NPV with sine PWM scheme*
1.	R = 10Ω, L = 2*e*-3H	12.22	-0.84
2.	R = 5Ω, L = 10*10e-12H	25.12	0.0122
3.	R = 8Ω, L = 10*10e-9H	17.23	-0.029
4.	R = 10Ω, L = 0.003H	28.02	-0.08

Fault Analysis

Fault time applied in this paper is 0.1 seconds

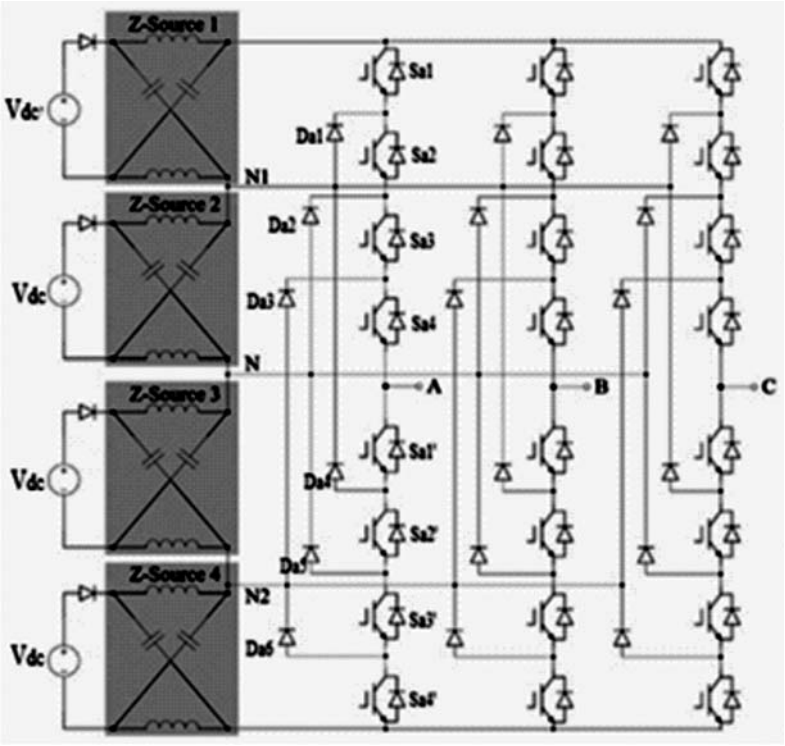

Fig. 7. Three level pole voltages without and with DC link capacitor balance having fault in system.

The fault time applied in this paper is 0.1 seconds. In fig t. It is shown that the fault applied from time 0.1 to 0.2 (sec). without DC link capacitor balance, pole voltages take more time to settle even after fault is cleared.

Table 4. Three level DCMLI voltages settling time after fault.

Fault	*Settling time (seconds) after fault without capacitor balancing system*	*Settling time after fault (seconds) with capacitor balancing system*
Line to ground	0.7	0.001
Line to line to ground	0.8	0.008
Line to line	0.7	0.008
Line to line to line	0.8	0.006

Table 5. Five level DCMLI voltages settling time after fault.

Fault	*Settling time (seconds) after fault without capacitor balancing system*	*Settling time after fault (seconds) with capacitor balancing system*
Line to ground	1.2	0.0001
Line to line to ground	2.6	0.0035
Line to line	2.8	0.003
Line to line to line	1.4	0.005

From table IV and table V it is seen that without capacitor voltage balancing circuit even after fault is cleared the settling time of voltages taking more than 0.5 seconds and it is also crossed 2 seconds for line to line and line to line to ground faults in five level inverter, This leads to uneven voltage distribution and inverter may damage. With DC link capacitor voltage balancing circuit the settling time after fault is decreased to very little.

5. CONCLUSION

Compared to SPWM modulation scheme capacitor voltage balance control scheme is better for individual voltage balance *i.e*. effective for NPCI more than three-level, and for faulty conditions. Without fault at load case for neutral point voltage balance SPWM scheme is best for any level DCMLI. When both control circuits used the DCMLI is most effective. In spite of having some complexity for having more switches the neutral point voltage balance is most effective compared to both individually and effective capacitor voltage balance is achieved.

6. REFERENCES

1. Jose Rodriguez, Steffen Bernet, Peter K. Steimer, Ignacio E. Lizama, “A Survey on Neutral Point Clamped Inverters”, IEEE Trans. on Industrial Electronics, Vol.57, No.7, sept 2010, pp. 2219 – 2230.
2. Anshuman Shukla, Arindam Ghosh, Avinash Joshi, “Control Schemes for DC Capacitor Voltages Equalization in Diode-Clamped Multilevel Inverter-Based DSTATCOM”, IEEE Trans. on Power Delivery, Vol.23, No.2, April 2008, pp. 1139-1149.
3. Zhiguo Pan, Fang Zheng Peng, K. A. Corzine, V. R. Stefanovic, J. M. Leuthen, S. Gataric, “Voltage balancing control of diode-clamped multilevel rectifier/invertersystems”, IEEE Trans. on Industry applications, Vol.41, No.6, Nov/Dec 2005, pp. 1698 - 1706.
4. Manthri Swamy, K. Anuradha, B. Ganesh Babu, “DC level stabilization in Neutral Point Clamped multilevel inverters”, IEEE Conference on Power, Control, Communication and Computational Technologies for Sustainable Growth (PCCCTSG), 11-12 Dec. 2015, pp. 211 – 216.
5. J.-H. Kim, S.-K. Sul, and P. N. Enjeti, “A carrier-based PWM method with optimal switching sequence for a multilevel four-leg voltage source inverter,” IEEE Trans. Ind. Appl., vol. 44, no. 4, pp. 1239–1248, Jul./Aug. 2008.
6. S. Ebanezar Pravin, R. Narciss Starbell, “Induction motor drive using seven level multilevel inverter for energy saving in variable torque load application”, International Conference on Computer, Communication and Electrical Technology (ICCCET), March 2011, pp. 352-357.
7. U. V. Patil, H. M. Suryawanshi, M. M. Renge, “Direct torque control of induction motor: Simulation results using two-level and diode clamped multilevel inverter”, Joint International Conference on Power Electronics, Drives and Energy Systems (PEDES) and Power India, Dec 2010, pp. 1-5.
8. J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, “Multilevel voltage-source-converter topologies for industrial medium-voltage drives,” IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2930–2945, Dec. 2007.