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VLSI Circuit of Cortical Neuron Applied with Bias Adaptation

Anirudha Singha[a] and Jyotirmoy Pathak[b]

[a-b]*Department of Electronics and Communication systems, Lovely Professional University. Email: [a]anirudhasingha2@gmail.com, [b]jyotirmoy.16082@lpu.co.in*

Abstract: Spiking and bursting patterns are produced by silicon neuron circuitry. It mimcs spiking pattern same as biologically. The neuron circuitry reproduces the intrinsic bursting, chattering, regular spiking and fast spiking. In real time, bias voltage is not fixed in the circuitry of neuron. It changes for all neuron. In paper circuit of cortex neuron is adaptive with bias voltage that is performed in VLSI circuitry which is analogues. The proposed circuit produced time depending bias voltage that applies to main input. The paper introduces how bias modulation is accomplished along with execution of the circuit. To perform bias adaption of the circuitry produces several spiking. The analysis of power is also determined for every spike patterns and it consumes low power. It is a simulation process, using the technology of 180nm which produces results of the circuit.

Keywords: Neuron Circuit, Membrane potential, Slow variable, Bias Adaptation, Spiking and Bursting.

1. INTRODUCTION

Spiking neural system is utilizing accesses propelled by bioscience, so that it gives to promise the answer for an assortment of critical issues. These issues may be advanced the ability to perform many capable PCs. Henceforth the fabrication and manufacture of VLSI neural circuits, which is having interest in expanding attention of research[13]. Among these applications, integrate and fire (I&F) neuron is broadly utilized because of its effortlessness and small size of the neuron circuit block[16]. Be that as it may, normally utilize I&F neuron cells expend roughly twenty transistors. It actualize power which is very low for versatile neuron circuit[1][2]. Moreover, I&F neurons display straightforward spiking conduct just; this may not to be satisfied due to the advancement of genuinely large number scale, conveyed, hugely collateral systems between VLSI hardware which is to be equipped for mirroring the handling of mortal sensory process, as the cortex is made of 90% non-direct oscillatory as opposed to basic spiking neurons[14]. In this way consideration of a few scientists has concentrated on executing basic neuron blocks that are equipped for giving various sorts of cortical spiking conduct through using as couple of transistors as conceivable to active integration of expansive number of cells in a one chip.

Circuitries actualizing neuron conductance-based models (Hodgkin-Huxley model)[3] have been accounted for the describing. So those circuits devour huge number of mosfets. This circuit usage of oscillatory models of neuron, for example, the model of FitzHugh-Nagumo neuron[4], the model of Morris-Lecar neuron[5], the Volterra model[6] in view of neuron model of the Resonate-and-Fire, the Hindmarsh-Rose neuron display and Oregonator Hardware model[7] have devoured around twenty transistors. Be that as it may, every one of these models don't imitate exact states of the spikes created by neurons which are biological and those are not equipped for delivering diverse sorts of cortical bursting and spiking practices in one circuit with parameters which are tunable.

In this paper we show a simple CMOS circuit by computational model[8] proposed by Izhikevich. While that model uses as basic as conceivable arrangement of scientific conditions, our model adventures underlying nonlinear attributes of MOS transistors to actualize the neuron with as few circuit components as could be expected under the circumstances. The input current is depending on the synapses circuit. The parameters depending on the STDP synapses implementations [15]. The spiking shape given by the circuit takes after that of genuine neurons (in spite of the fact that it works on an alternate timescale - the VLSI neuron is more than 105 times quicker than the biological one). Here proposed circuit has 19 transistors. Bias voltage of this circuit is changing according to the membrane potential. Instead of fixed bias voltage, it is now adaptive in nature.

2. CORTICAL NEURON MODEL

The circuit is to be seen in Figure (1). The implemented circuit consists of two state variables illustrates by voltage. The voltages produce across the capacitors Cv and Cu. These are called as membrane potential (V) and slow variable (U)[10]. Different types of spiking and bursting is generated by controlling two parameters Vc and Vd. From the analysis of the circuit we defined the following equations:

$$V = \begin{cases} I1V^2 - I2V - I3U^2 + I4U + I5 & \text{If } V \geq U - UT \\ m_1V^2 - m_2V - m_3UV + m_4 & \text{otherwise} \end{cases} \quad (1)$$

$$U = k1V^2 - k2V - k3U^2 + k4U + k5 \quad (2)$$

if $V \geq V^{th}$ then, $V < -C$, $U < -\Delta Q + U$

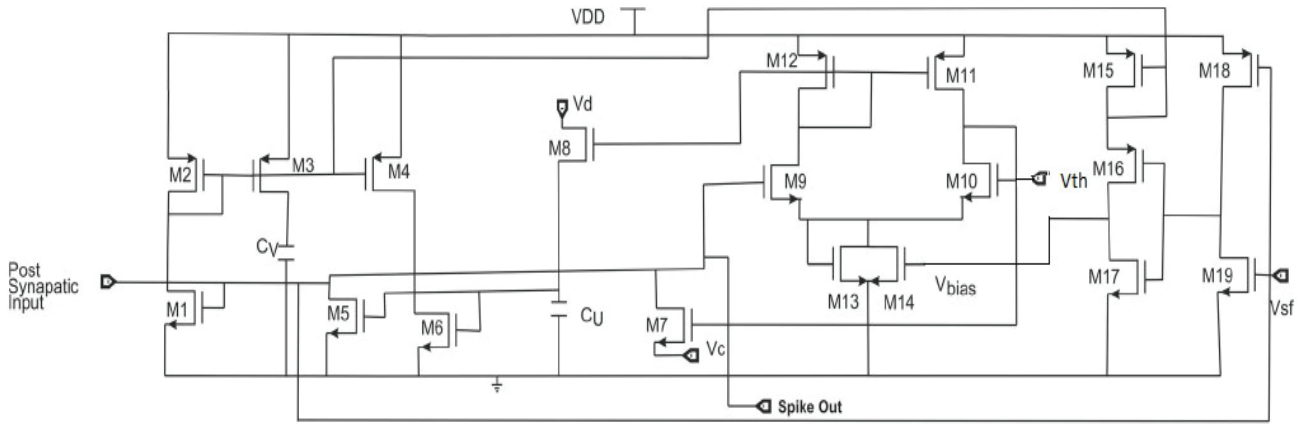


Figure 1: Proposed circuit with bias adaption

It is very basic model and it generates bursting, spiking and bursting, low threshold spiking and mixed spiking patterns etc. Izhikevich model is most simple and adjustable model so that it generates spiking patterns

almost close to cortex. The synapses current is a basically step current which is generally introduced by external synapses circuit [12][17][18].

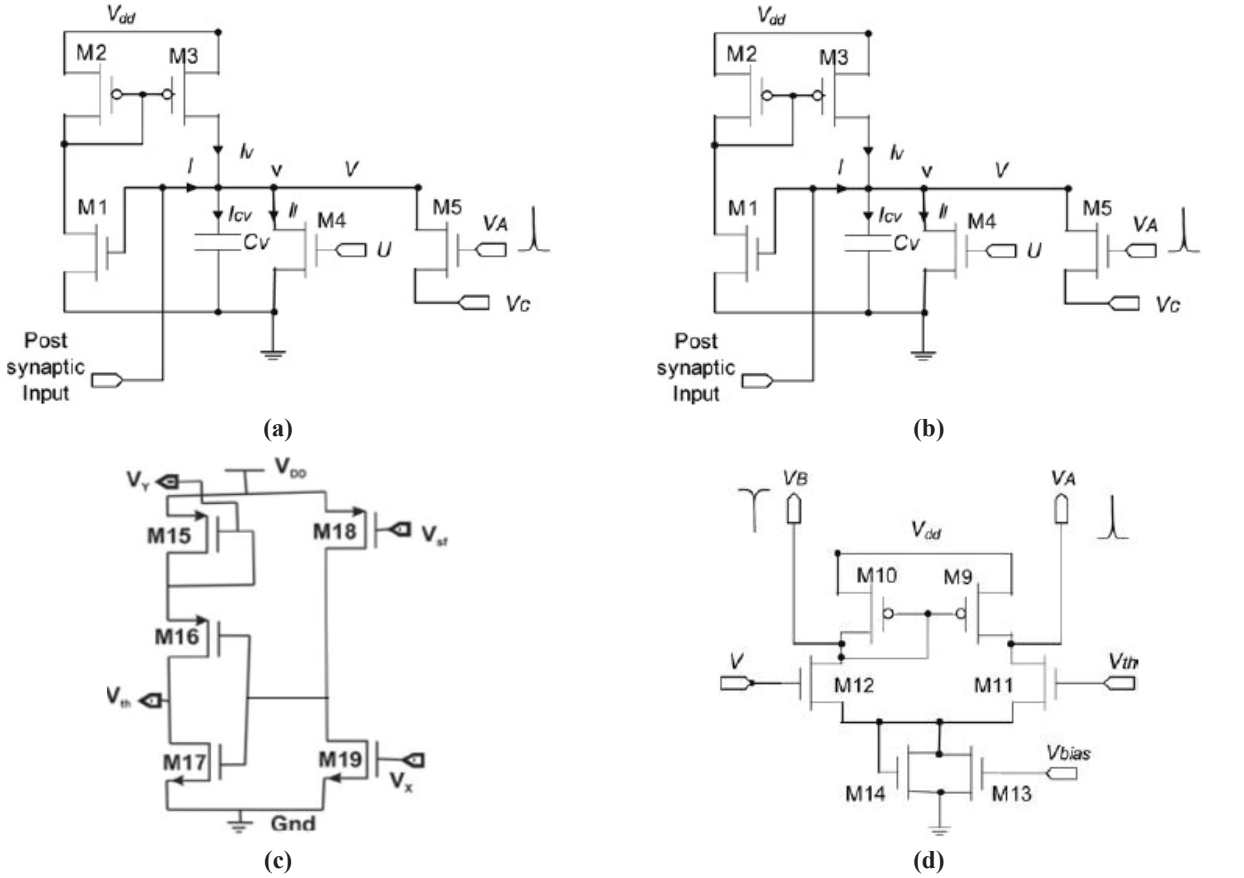


Figure 2: Sub-circuits of the cortical neuron: (a) Membrane potential circuit, (b) Slow variable circuit, (c) Comparator circuit, (d) Bias adaptation

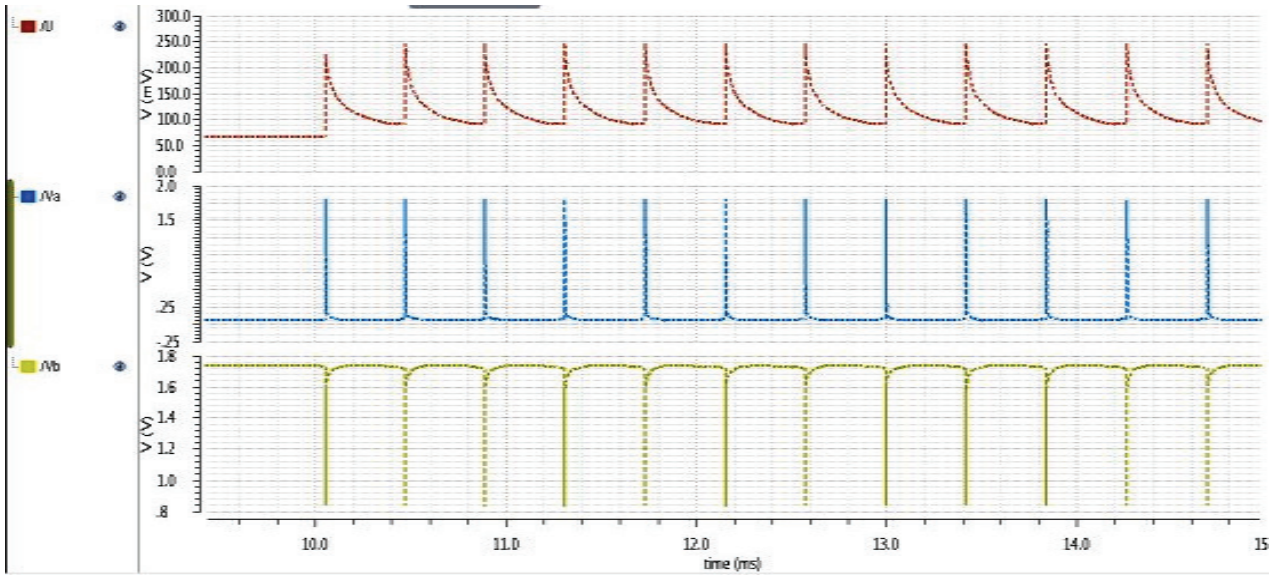


Figure 3: Waveforms of slow variable (U) and Comparator (VA and VB)

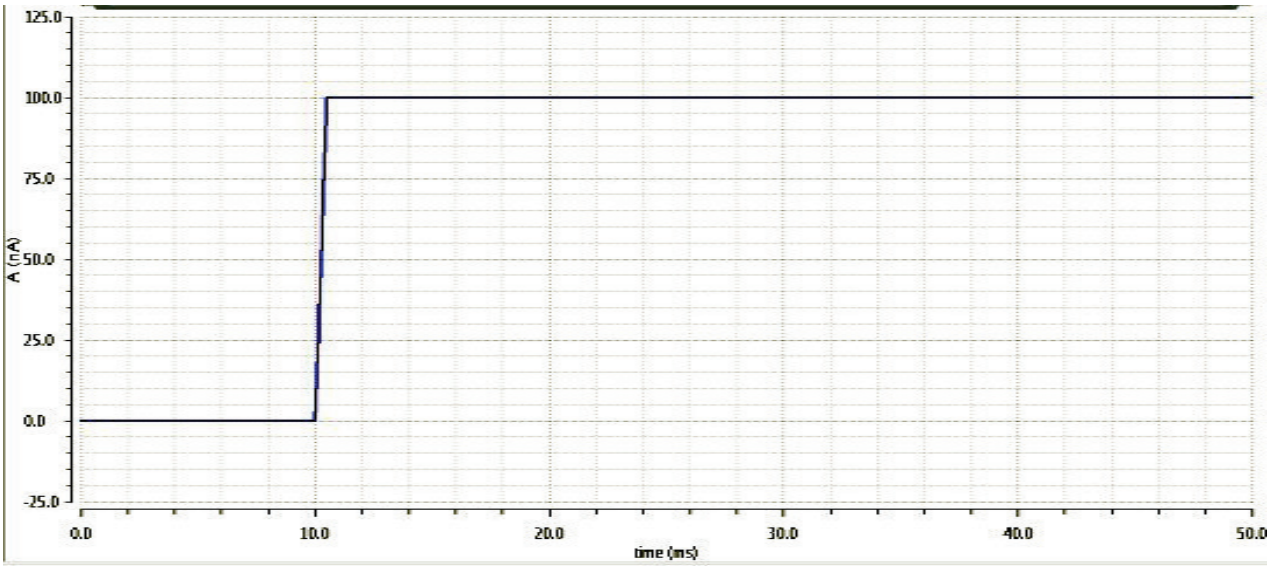


Figure 4: Input Step Current (0.1µA)

3. IMPLEMENTATION

The proposed circuit consists of four functional blocks such as:

(a) Membrane Potential Circuitry

The circuitry is illustrated in Figure: (2.a). As shown in Figure (4) the input step current is led at M1 transistor. The Iv is produced by the circuit (M1-M3) which is (M1 to M3) current mirror. That feedback current (Iv) is applied across capacitor Cv. Transistor (M4) generates the leakage current (Il). The leakage current is maintained through the slow variable (U). summation of the currents are implemented across the capacitor (Cv) of membrane. The equation of the capacitor (Cv) is followed as[9]:

(3)

The comparator generates a pulse when the membrane potential attain a threshold voltage (Vth). The generated pulse resets the membrane circuit through transistor (M5).

(b) Slow Variable Circuitry

The slow variable circuitry is illustrated in Figure: (2.b). Voltage of that circuitry, U is generated through integrate through the current gives by the transistor (M7)., minus that current observed by the transistor (M6). The sum current across the slow variable capacitor (Cu) is followed as:

(4)

A charge through the transistor (M7) provides incremental the slow variable voltage during the comparator output generates a pulse.

(c) Comparator Circuitry

The comparator circuitry is illustrated in Figure: (2.c). The circuit produces two pulses VA and VB as illustrared in Figure (2). VA is applied across the transistor (M5) and VB is applied across the transistor (M8) to discharge the capacitor and reset the parameters to Vd and Vc values[11].

(d) Bias Adaptation Circuitry

Bias adaption circuitry is illustrated in Figure (2.d). It is followed by the transistor (M15-M19). In real time, bias voltage is not constant. It changes according to membrane potential. To get that membrane potential is connected with some source follower. To get that membrane potential is connected through source follower in inverter and feedback loop circuitry. The follower equation is followed as:

(5)

where, Vmem = membrane voltage and Vsf = constant voltage for source follower. This voltage is going to be inverted and it generates the bias voltage as illustrated in Figure (5).

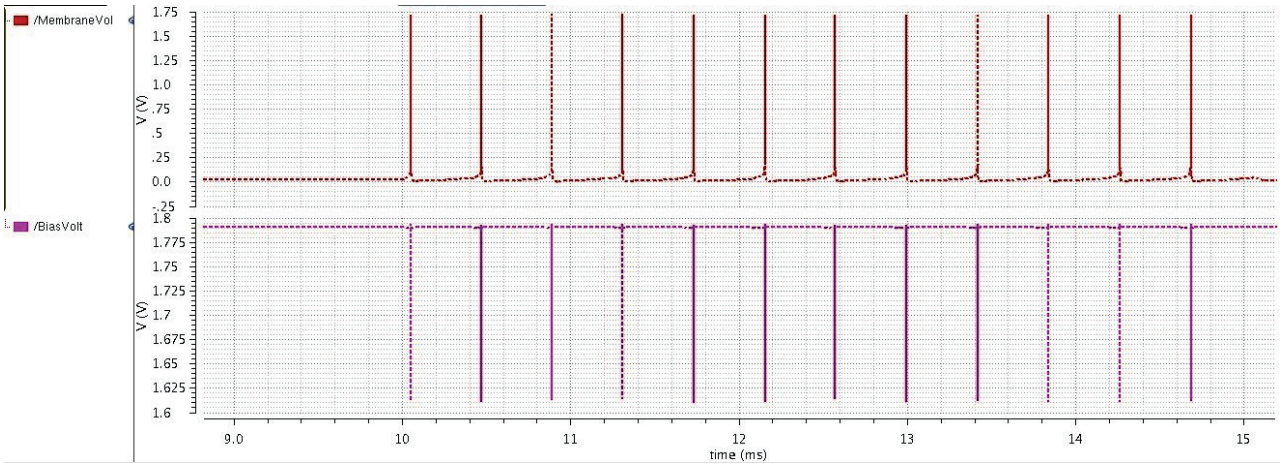


Figure 5: Changing in membrane potential and bias modulation voltage

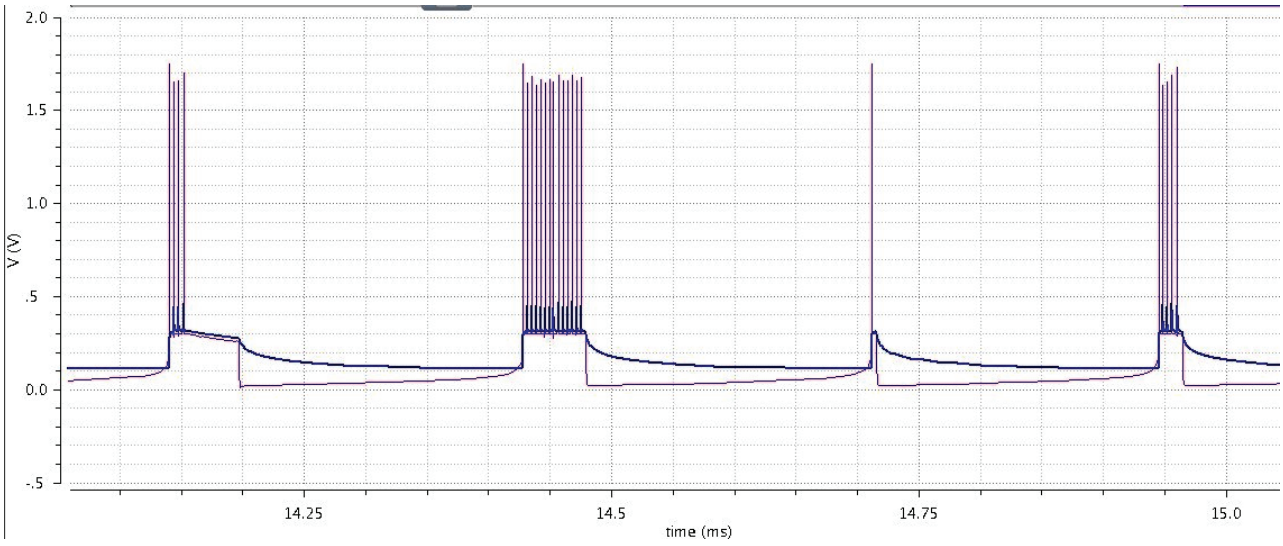


Figure 6: Reaction of the chattering cell to a step post synaptic current 0.1μA infusion demonstrating starting and consequent spike groups with respect to the membrane potential (Vmem) and slow variable potential (U)

4. EXPERIMENTAL RESULTS AND DISCUSSION

The proposed circuit made of 19 transistors that have four sub blocks. The step input current is defined as post synaptic current which is applied as 0.1μA. The neuron circuit produces different types of bursting and spiking

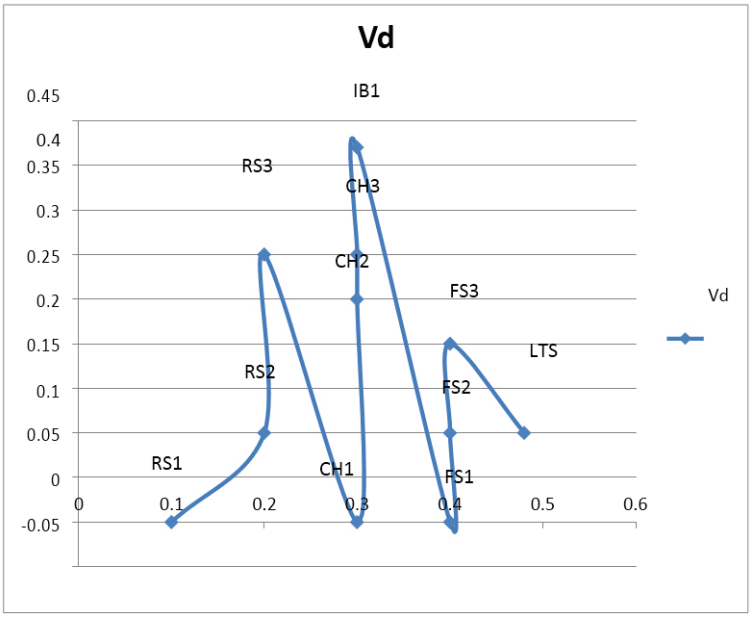
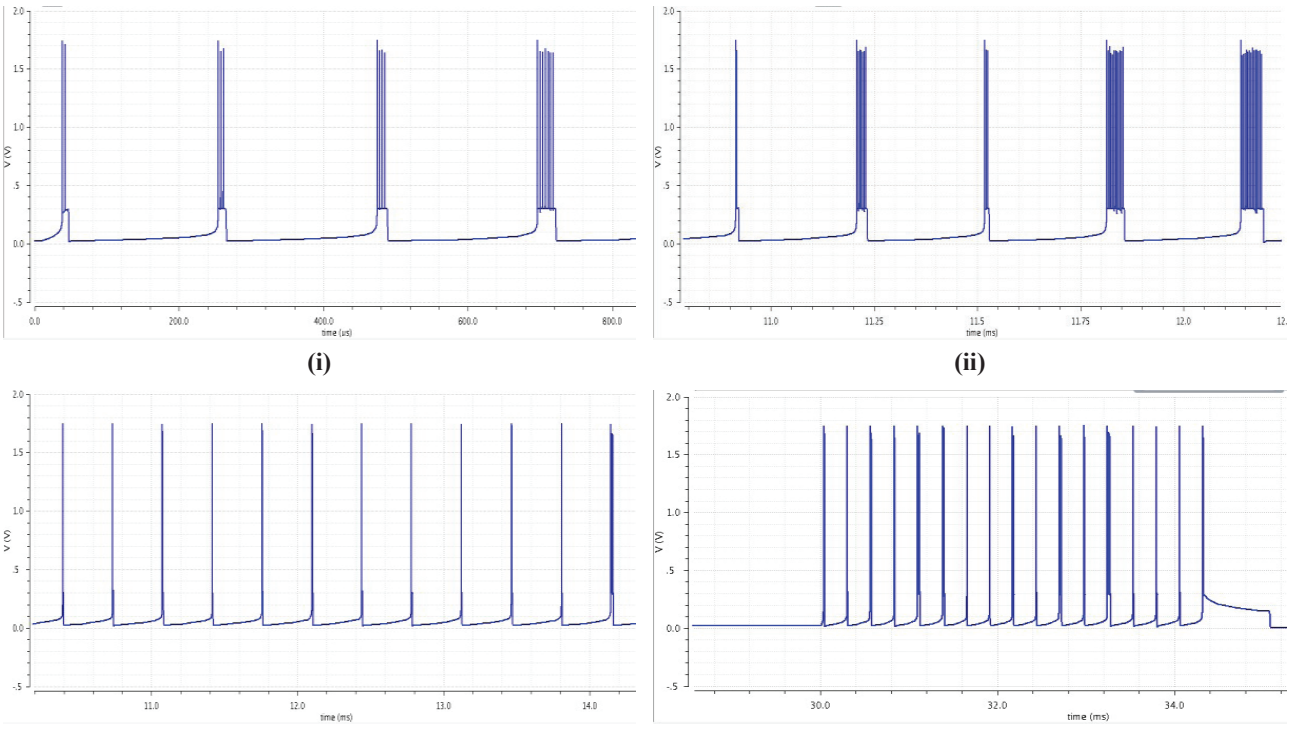


Figure 7: Vd and Vc plot for various types of spiking pattern

by changing the two voltage parameters suvh as Vc and Vd. for regular spiking (RS) is illustrated as Figure (4).In Figure (5) the progressive behaviour among the spiking is explained state trajectories across two variables such as slow variable and membrane potential. It also determines the membrane voltage is increased by applied step input current to fixed value. For feedback path, it increases quickly because of action potential of depolarization after the spiking is generated. The comparator circuit observes the output and resets the potential of the membrane circuit signal by discharging the respective two capacitor, Cv and Cu.



(i) **(ii)**

(iii) **(iv)**

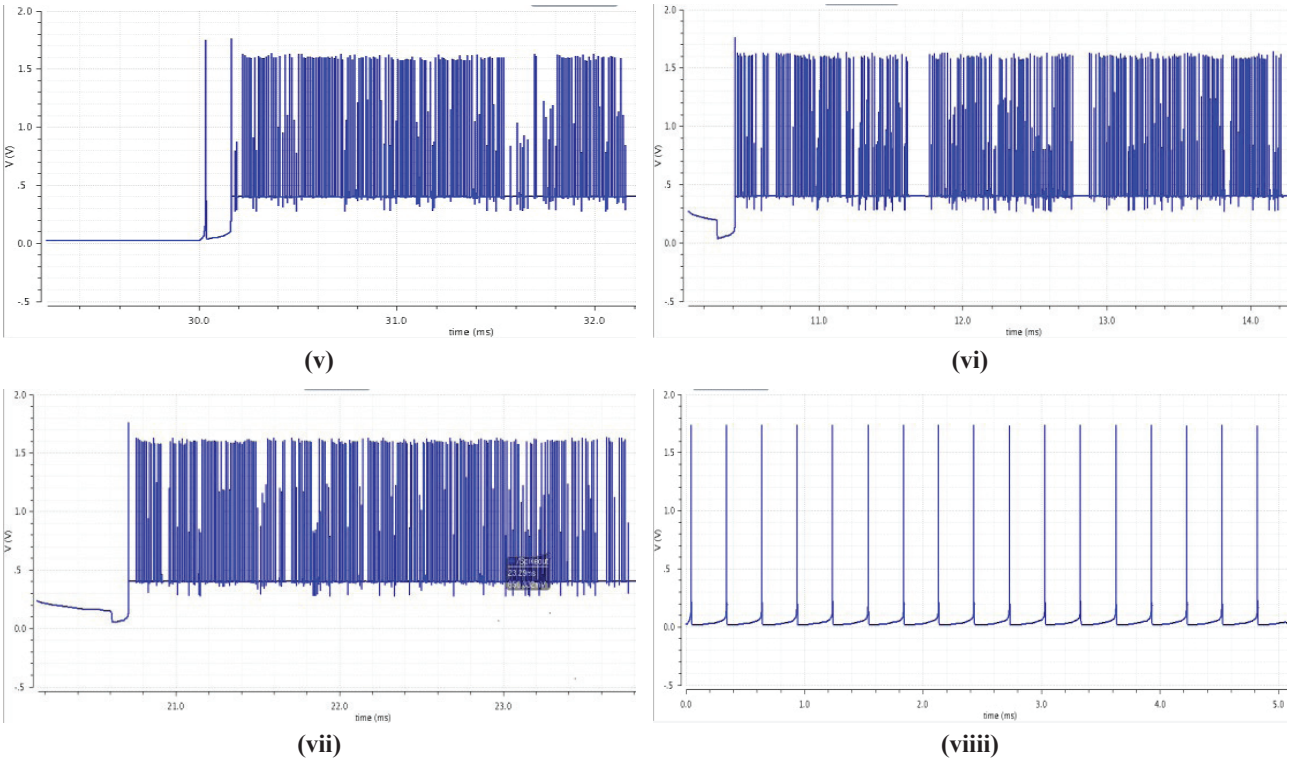


Figure 8: Output waveforms of (i & ii) CH, (iii & iv) IB, (v, vi & vii) FS and (viii) RS

Table 1
Comparison between different neuron models with respect to proposed neuron model

Neuron Model	*Types of Spiking (RS, CH, IB, FS, LTS)*	*Number of Transistors*	*Shape of Spikes*	*Power (μW)*	*Adaptation*	*References*
Conductance-based	Normal Spiking	18 - 20	Fair	0.3 – 1.5	Yes	Mahowald and Douglas (1991)
Integrate and fire	Normal Spiking	27 – 30 +	Good	60	_	Indiveri (2003)
Morris-Lecar	Oscillatory	22	Envelope	_	_	Patel and De Weerth (1997)
Fitz Hugh-Nagomo	Oscillatory	21	Envelope	_	_	Linares Barranco et. al., (1997)
Hindmarsh- Rose	Bursting (CH)	90	Fair	163.4	_	Lee et. al., (2004)
Resonate and Fire	Oscillatory	20	Pulse	_	_	Nakada et. al., (2005)
Compact Silicon Neuron	All types	14	Good	8 - 40	_	Wijekoon and Dudek (2008)
Proposed Circuit	All types	19	Good	13.63 – 14.96	Yes	Proposed Circuit

Comparison between different neuron models and proposed model give an idea to evaluate the best model. We can determine the different characteristics, output patterns and no of components used. It gives also the power consumption value to determine which one is best for low power design. In above table we are comparing of the execution of various neuron models and proposed neuron model. The proposed model is capable to produce all types of spiking and all outputs spike patterns are also good as compare to others. The Figure 8 illustrates all type of spiking of the proposed cortical neuron circuit.

The Figure 9 shows the power analysis at different currents for each bursting and spiking. It illustrates increasing power for different spiking. Here we can see FS consumes the higher power but in other patterns consume very less. This occurrence happens for quick rising and declining rates of membrane voltage in fast spiking. Regular spiking consumes less power while CH and IB consume comparatively high power.

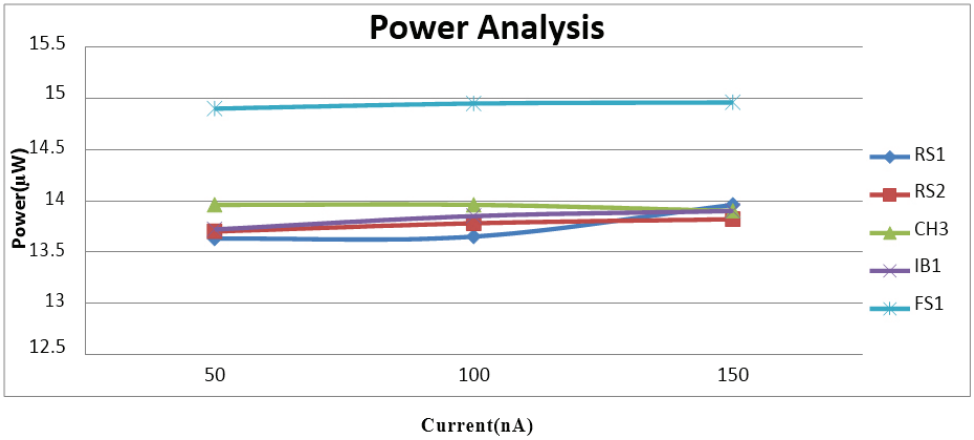


Figure 9: Power analysis for different spiking at different current

5. CONCLUSION

The CMOS neuron circuit is generating bursting and spiking firing characteristics with a biological spike shapes. The behaviour of that circuit is verified through cadence simulation. The proposed circuit is capable of mimics to generate various types of spiking which is resembles of the real neuron cells. The characteristics of cortical cells should be adjusted by threshold voltage and biasing voltage. Here biasing voltage is modulated by membrane potential. The circuit is implemented using 19 transistors. Because of the low number of MOSFETs is used so that it could be inserted in huge blocks of cortical micro circuits and take a small silicon area. To generate parallel analo neuromorphic networks, we are using compact, simple, and easily configurable circuit of cortical neuron. It is as similar as neocortex characteristics by changing (W/L) ratios of the MOSFETs M4, M6, M7. This circuit is designed using 180nm technology. The spiking output is mainly vary when two voltages Vc and Vd is changing respectively. The circuit is consumed very less power than other neuron circuits. So it helps to build very less power microcircuits in cortical neuron.

REFERENCES

[1] S. R. Schultz and M. A. Jabri, "Analogue VLSI 'integrateand-fire' neuron with frequency adaptation," Electronic Letters, Vol. 31, No. 16, pp. 1357–1358, Aug 1995.

[2] G. Indiveri. "A low-power adaptive integrate-and-fire neuron circuit." IEEE Int. Symp. Circuits and Systems, ISCAS, pp IV820-823, 2003.

[3] B. Linares-Barranco, E. Sanchez-Sinencio, A. Rodriguez-Vazquez, J. L. Huertas. "A CMOS implementation of FitzHugh-Nagumo neuron model", IEEE Journ. Solid-St. Circ., Vol. 26, No. 7, pp 956-965, 1991.

[4] G.N. Patel, S.P. DeWeerth "Analogue VLSl Morris-Lecar neuron" Electronics Letters, Vol. 33, No. 12, pp 997- 998, 1997.

[5] K. Nakada, T. Asai and H. Hayashi. "A silicon Resonate-and-fire neuron based on the volterra system", Int. Symp. on Nonlinear Theory and its Applications, pp 82-85, 2005.

[6] Young Jun Lee et.al. "Low power real time electronic neuron VLSI design using subthreshold technique", IEEE Int. Symp. Circuits and Systems, Vol. 4, pp IV-744-747, 2004.

[7] K. Nakada, T. Asai, and Y. Amemiya "Analog CMOS implementation of a bursting oscillator with depressing synapse" in Proc. Intelligent Sensors, Sensor Networks and Information Processing Conference, ISSNIP '04, pp 503-506, 2004.

[8] E.M. Izhikevich, "Simple model of spiking neurons" IEEE Trans. Neural Netw, Vol. 14, No. 6, pp. 1569 - 1572, Nov. 2003.

[9] Ethoti Radhika, Sanjeev Kumar, Anita Kumari. "Low Power Analog VLSI Implementation of Cortical Neuron with Threshold Modulation". 978-1-4799-8792-4-4/15/$31.00,2015 IEEE.

[10] Jayawan H B Wijekoon and Piotr Dudek, "Simple Analogue VLSI Circuit of a Cortical Neuron" 2006

[11] Jayawan H B Wijekoon and Piotr Dudek "A CMOS circuit implementation of a spiking neuron with bursting and adaptation on a biological timescale" 2007

[12] R. J. Vogelstein, U. Mallik, and G. Cauwenberghs, "Silicon spikebased synaptic array and address-event transceiver," in Proc. IEEE Int. Symp. Circuits and Systems, pp. 385–388, 2004.

[13] P. Merolla and K. Boahen, "A recurrent model of orientation maps with simple and complex cells," in Advances in Neural Information Processing Systems. Cambridge, Vol. 16, pp. 995–1002, 2004.

[14] F. Tenore, R. Etienne-Cummings, and M. Lewis, "A programmable array of silicon neurons for the control of legged locomotion," in Proc. IEEE Int. Symp. Circuits and Systems, pp. 349-352, 2004.

[15] A. Bofill-i Petit and A. F. Murray, "Synchrony detection and amplification by silicon neurons with STDP synapses*,"* IEEE Trans. Neural Netw., Vol. 15, No. 5, pp. 1296–1304, Sep. 2004.

[16] [S. C. Liu and R. Douglas, "Temporal coding in a silicon network of integrate-and-fire neurons," IEEE Trans. Neural Netw., Vol. 15, No. 5, pp. 1305–1314, Sep. 2004.

[17] E. Chicca, D. Badoni, V. Dante, M. D'Andreagiovanni, G. Salina, S. Fusi, and P.D. Giudice, "A VLSI recurrent network of integrate-andfire neurons connected by plastic synapses with long term memory," IEEE Trans. Neural Netw., Vol. 14, No. 5, pp. 1297–1307, Sep. 2003.

[18] Giacomo Indiveri, Elisabetta Chicca, and Rodney Douglas, "A VLSI array of low-power spiking neurons and bistable synapses With Spike-Timing Dependent Plasticity" IEEE Trans. on Neural Netw., Vol. 17, No. 1, pp. 211-221, January 2006.