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# Comparative analysis of Level-2 battery chargers for Plug-in Automotive Applications

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**ABSTRACT**

This paper deals with a comparative analysis of three different topologies of AC/DC Power Factor Corrected (PFC) boost converter being used in plug-in automotive applications. Three topologies namely, interleaved, semi-bridgeless and bridgeless interleaved are considered. Digital Proportional Integral (PI) control is implemented to validate the performance of each topology. The experimental and simulation results are presented for a universal input voltage of 230V, with power factor correction and the output voltage is regulated to 400V. The digital platform used is TMS320CF28335 DSP processor. The performance of the converters is compared in terms of input power factor, output voltage regulation and its efficiency. It is concluded from the performance analysis, that the bridgeless interleaved converter is suitable for level-II charging plug-in automotive applications.

***Keywords:*** conduction losses, EMI filter, front end AC/DC PFC boost converter, Plug-in automotive applications, PI controller.

## 1. INTRODUCTION

The conversion of conventional Hybrid Electric Vehicles (HEV) to plug-in Hybrid Electric Vehicle (PHEV) is to reduce the fuel consumption, lower emission and higher performance. PHEV constitutes a storage system that would be recharged by plugging an external electric power source [1]-[3]. Basically, the chargers are classified based on the power level that they can provide to the battery. They are termed as Level-I, Level-2 and Level-3 chargers. Level-1 battery chargers for a rated to 120V and 15A are used for the common household circuit. Level-2 and Level-3 chargers are used for permanently wired electric vehicle equipment for charging. Level-2 chargers are rated up to 240V, 60A with a load power of 14.4kW. Level-3 battery chargers are rated above14.4 kW. Fig. 1 illustrates the simplified block diagram of a level-2 battery charger. The front-end AC/DC power factor correction (PFC) converter is the main component of the charger system. The charger unit [4], [5] was categorically divided into two: single stage approach and two-stage approach. The single stage modeled is suitable for low power applications where only lead acid batteries can be charged.

Two-stage approach shown in Fig. 1 is suitable for high power applications and is used for charging PHEV batteries. The first-stage is the rectification and amplification of the input AC voltage ($V_{in}$). Also

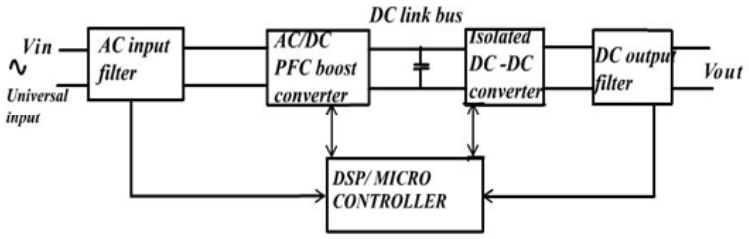


**Figure 1: Block illustration of the universal two-stage battery charger.**

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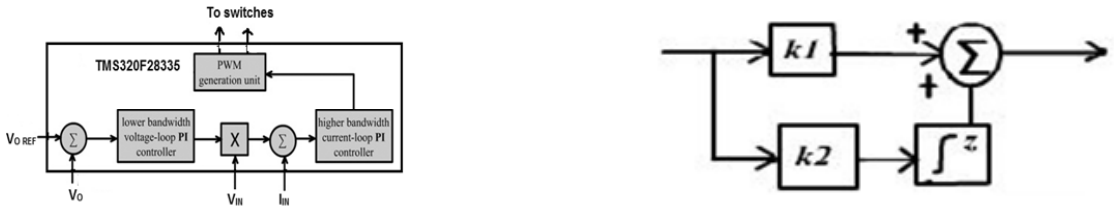
transferring it into a regulated intermediate DC bus link. At the same time, power factor correction on the input is also achieved significantly. The second stage is DC-DC converter stage, which provides isolation between mains and the battery bank.

This paper focuses on three different front-end AC/DC converters with digital implementation of PI control for improving the input power factor and regulating the output voltage. Topologies considered are interleaved, semi-bridgeless and bridgeless interleaved boost converters. Here, Section-II describes the implementation of digital control technique and section-III deal about AC/DC boost converter topologies. Section-IV and V analyze the simulation and hardware results for three topologies. Converter performance is compared in Section-VI, followed by conclusion in Section-VII.

## 2. DIGITAL PI CONTROL TECHNIQUE

To meet the regulatory standards on the power quality of the front end converter [6-9], different control methods such as average current mode control [10]-[11], peak current mode control [12], one cycle control [13] and hysteresis control [14] are used. Digital PI control is suitable for both continuous and discontinuous conduction modes of converter operation. The controller can generate high-quality current waveforms over a extensive range of input voltages and power loads. It consists of outer voltage loop with lower bandwidth PI controller and inner current control with higher bandwidth PI controller as shown in Fig. 2(a). DSP TMS320F28335 processor is used to implement the digital PI control to validate the performance of each topology.




**(a)** **(b)**

**Figure 2: (a) Digital PI control implementation of AC/DC converter. (b) PI controller in z-domain using bilinear transformation**

In this technique, the controller multiplies input voltage signal $V_{IN}$ with compensated output voltage $V_{REF} = -V_O$ generates the current reference, while the control loop for current, tracks the average current through the inductor to trail the current reference. The continuous time signal is converted to discrete signal using bilinear transformation technique as shown in Fig. 2 (b). The transformation expression from continuous time system to discrete time system is given as follows:

$$k\frac{(1+sT)}{sT} \Rightarrow k_1 + k_2 \frac{T_s}{2}.\frac{1+z^{-1}}{1-z^{-1}} \tag{1}$$

$$T_s = 1/f_s \tag{2}$$

where $T_s$ is the sampling period, $f_s$ is the switching frequency and $k_1$, $k_2$ are the gains of the PI controller. Three topologies interleaved, semi-bridgeless and bridgeless interleaved are considered for analysis.

## 3. AC/DC PFC BOOST CONVERTER TOPOLOGIES

In this section, the following AC/DC boost converter topologies are discussed.

(i) Interleaved PFC Boost Converter: Interleaved boost converter [15]-[21] is shown in Fig. 3 consists of two individual boost converters connected in parallel to a common bridge rectifier. These parallel converters are made to operate at 180° out of phase. The input current ($I_{IN}$) is the sum of the current through both the inductors $L1$ ($I_{L1}$) and $L2$ ($I_{L2}$).The technique of interleaving reduces the input ripple current; inductor size and also Electro-Magnetic Interference (EMI) filter design. Though the output capacitor ripple is reduced, it still has the problem of heat management due to the presence of the diode bridge rectifier.

(ii) Semi-bridgeless boost converter: Semi-bridgeless PFC boost converter [22]-[26] introduces two more slow diodes ($D_1$ and $D_2$) to bridgeless converter for linking ground of the PFC to the input line as shown in Fig. 4.The operation is similar to bridgeless converter but the load current will flow through the slow diodes for a certain time interval. As the current doesn't flow through the slow diodes always, the conduction losses are less for diodes. This occurs at line frequency and the inductors exhibit low impedance. Large amount of current will flow only through intrinsic body diodes of switches $Q_1$ and $Q_2$. The lesser number of components reduces the charger cost and EMI.

(iii) Bridgeless interleaved PFC boost converter: The bridgeless interleaved boost converter [27],[28] is shown in Fig. 5 comprises of two more switches ($Q_3$ and $Q_4$) and two more fast diodes ($D_3$ and $D_4$) in place of four slow diodes used in the diode bridge rectifier. The circuit comprises of two interleaving inductors connected to each phase.

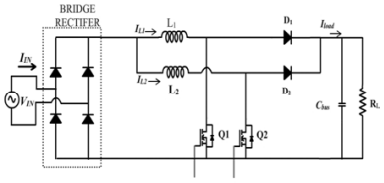



**Figure 3: Interleaved PFC boost converter**

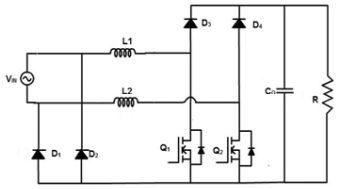



**Figure 4: Semi-bridgeless boost converter**

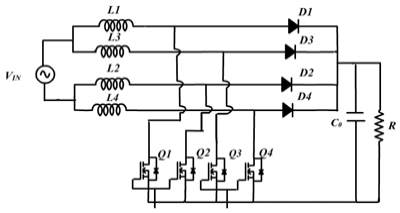



**Figure 5: Bridgeless interleaved PFC Boost converter**

Four channel interleaving further reduces the input current ripple which in turn reduces the EMI filter design. As the topology eliminates the diode bridge rectifier, on-state conduction losses are reduced compared to the interleaved boost converter. Interleaving further reduces RMS current stress on switch. High efficiency over complete load range and high input power factor is achieved. Furthermore, a higher efficiency means more power will be available from the mains to charge the batteries. This is to reduce the charging time and electricity costs.

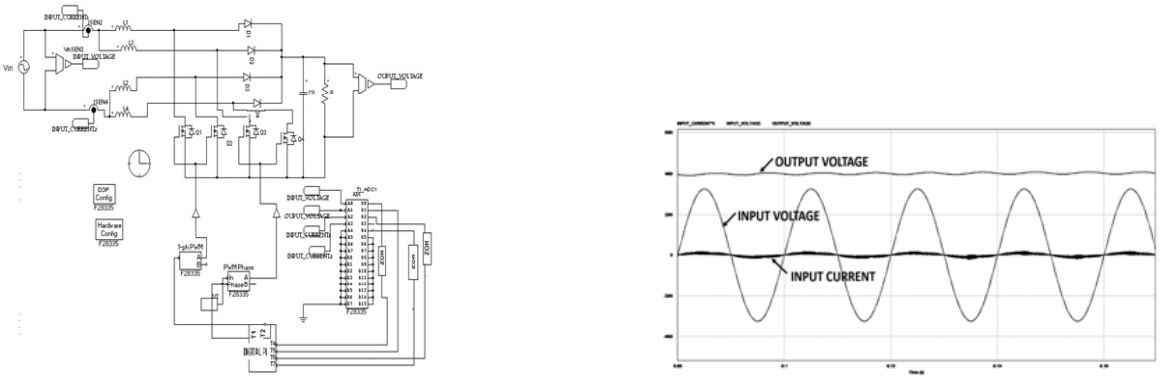
## 4. SIMULATION RESULTS

PSIM software is used for simulation of AC/DC boost converter topologies. The circuit specifications for each converter are given in Table-1.

The simulation diagram for bridgeless interleaved converter is shown in Fig. 6(a). In simulation, the DSP processor (TMS320CF28335) is configured with external clock frequency as 30 MHz and internal speed as 150 MHz. It has 16-channel ADC, single phase PWM generator and phase shift PWM generators. The Code Composer Studio (CCS) version 5 from Texas Instrument (TI) is used for debugging.

**Table 1**
**Specifications of each topology**

| *Topology/Parameters* | *Interleaved Boost Converter* | *Semibridgeless Boost* | *Bridgeless Interleaved Boost* |
|---|---|---|---|
| Output power(W) | 300W | 300W | 300W |
| Input voltage(Vac) | 230V | 230V | 230V |
| Output voltage | 400V | 400V | 400V |
| Switching frequency | 100kHz | 70kHz | 70kHz |
| Inductor | 220µH | 1mH | 0.58mH |
| capacitor | 200µF | 470µF | 470µF |




**(a)** **(b)**

**Figure 6: (a) PSIM simulation of Bridgeless interleaved Boost converter**
**(b) Waveforms showing input voltage ($V_{in}$), current ($I_{in}$) and output voltage ($V_O$)**

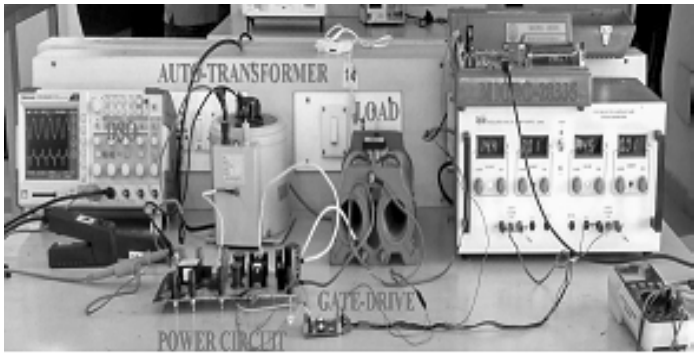
Fig. 6 (b) shows the simulation results for input voltage, input current and output voltage of bridgeless interleaved topology. The waveform shows that the input current is in phase with the voltage, thus achieving high power factor. All the three topologies are analyzed for universal input voltage and the output voltage is regulated to 400V. The power factor is maintained closer to 0.99 under various load conditions.

## 5. HARDWARE RESULTS

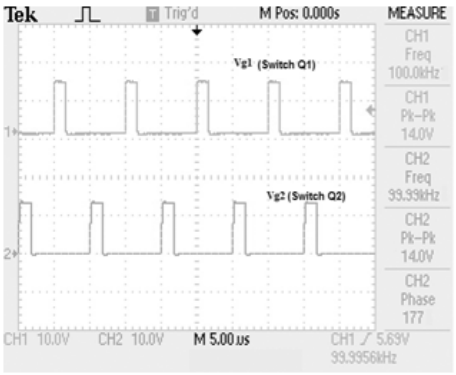
Hardware is implemented for the above topologies, to validate the simulation result. PI controller is implemented using DSP TMS320CF28335 eZdSP board from Texas Instruments. This DSP board is a floating-point DSP, which tenders a supple environment for advanced mathematical calculations. It has an in-built ADC with a sequencer which can able to convert multiple analog signals sequentially. It also has six enhanced PWM (EPWM) modules, which will provide the desired PWM signals with a very high degree of flexibility and accuracy. However, for the higher frequency range, high-resolution EPWM should be used to achieve a high-resolution PWM signal and to shun the instability. The sampling frequency is taken as similar to the switching frequency of the converter.

(i) Interleaved boost converter: The experimental prototype to verify the operation of interleaved boost converter is shown in Fig. 7 (a). The switching pulses to the MOSFET's ($Q_1$ and $Q_2$) from DSP processor is presented in Fig. 7 (b). High switching frequency of 100 kHz is preferred in order to reduce the core and inductor size. Fig. 7(c) shows the waveforms of input current, input voltage of 228V and an output voltage of 383V.

(ii) Semi-bridgeless boost converter: The experimental prototype is done to verify the operation of the semi-bridgeless boost converter. The gating pulses to MOSFETs ($Q_1$ and $Q_2$) with a switching




**(a)**

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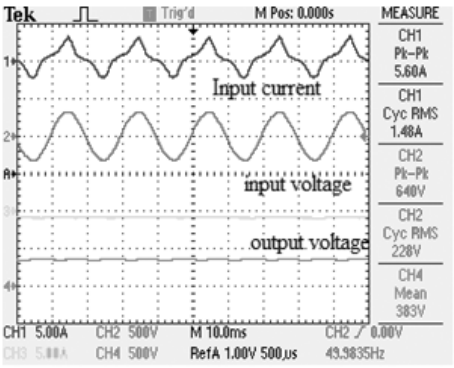
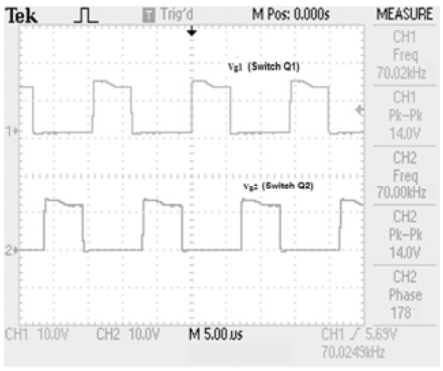
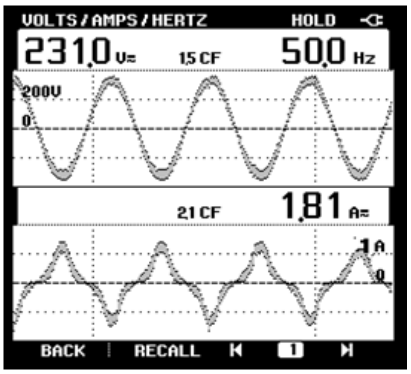



**(c)**

**Figure 7: (a) Hardware setup for interleaved boost converter (b) Gating pulses for 100 kHz switching frequency (c) Input current, input voltage and output voltage waveforms**




**(a)**

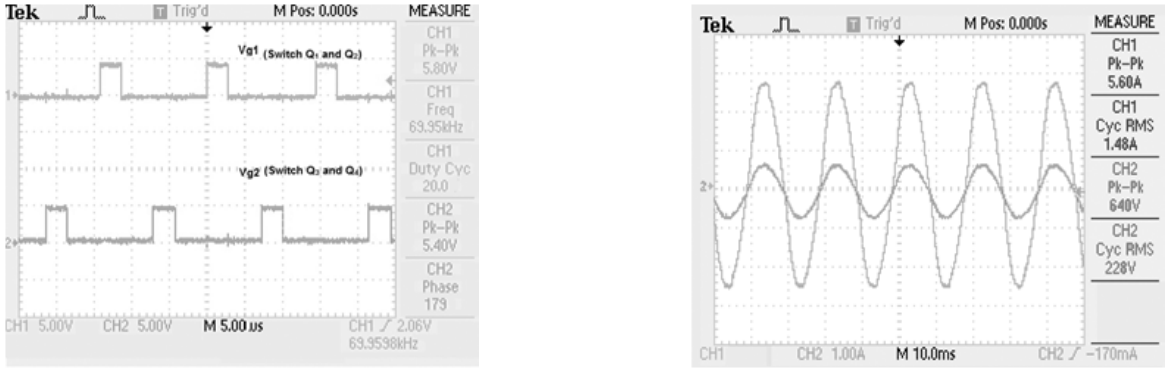



**(b)**

**Figure 8: (a) Gating pulses from DSP processor**
**(b) Input current, input voltage and output voltage waveforms for 80% of the load.**

frequency of 70kHz and duty cycle 40% is shown in Fig. 8(a). Fig. 8(b) reveals the waveforms of input current, input voltage and output voltage tested for =230V.

(iii) Bridgeless interleaved boost converter: The experimental setup for bridgeless interleaved boost converter is shown in Fig. 9(a) and the pulses to the switches with 20% duty cycle are shown in Fig. 9(b).The switching frequency is 70kHz. The four channel interleaving reduces the input current ripple as compared to semi-bridgeless boost converter and The input power factor is 0.94 as shown in Fig. 9(c) when the converter is tested with an input voltage of 230V.




**(a)** **(b)**

**Figure 9: (a) Gating pulses for experimental prototype of Bridgeless interleaved converter (b) Input voltage and input current waveform.**

## 4. COMPARISON OF PFC BOOST CONVERTERS:

The converters are designed under the following assumptions: (i) the converters are operating in continuous conduction mode and (ii) the input line voltage is pure sinusoidal waveform.

Loss analysis: The power losses associated with diode rectifier, switches and the magnetic elements decide the efficiency of the converter. The losses are calculated by considering conducting losses and the reverse recovery loss of the diodes and the switches.

Conducting loss is calculated from equation (3),

$$P_c = V_d * I_d * D_{on} \tag{3}$$

where $V_d$ is the forward voltage drop, $I_d$ is the conduction current and $D_{on}$ is the on duty of the diode. Reverse recovery loss ($P_{trr}$) is obtained from the maximum reverse current $I_{rm}$, reverse breakdown voltage ($V_{BR}$) and the reverse recovery time ($t_{RR}$). ($P_{trr}$) is obtained from equation (4) as given below:

$$P_{trr(diode)} = (t_{rr} * V_{BR} * I_{RM} * f_{sw})/8 \tag{4}$$

Switching losses $P_{sw}$ of MOSFET is given by

$$P_{sw} = 0.5 * V_{out} * I_{rms} * (t_{c(on)} + t_{c(off)}) * f_{sw} \tag{5}$$

where $t_{c(on)}$ is the ON time of the switch, $t_{c(off)}$ is switch off time and $I_{rms}$ is the RMS value of the current through the switches. Conduction loss $P_{cond}$ of switch is calculated as

$$P_{cond} = I_D^2 * R_{DS(on)} * D_{on} \tag{6}$$

where $I_D$ is the conduction current of the switch and $R_{DS(on)}$ is the resistance value during on-time. Magnetic components losses are based on the quality of the magnetic material and volume offered by its manufacturer. In interleaved boost converter, the regular diode in diode bridge rectifiers contributes the largest share of losses. The bridgeless topology eliminates these large loss components. Fast diodes in bridgeless interleaved boost converter have slightly lower power losses. But the switching losses are higher and in addition to that the conduction of intrinsic body diodes of MOSFET. This also contributes to the total power losses.

From Fig. 10 it is clear that, for the same load condition, the total semiconductor losses [41] for the bridgeless interleaved boost converter will be 15% lower than the semi-bridgeless boost converter, while 35% lower than interleaved boost converter. Hence, the efficiency is high for bridgeless interleaved topology. Fig. 11 shows the power factor comparison of the topologies for variable output load ranging from 33% to

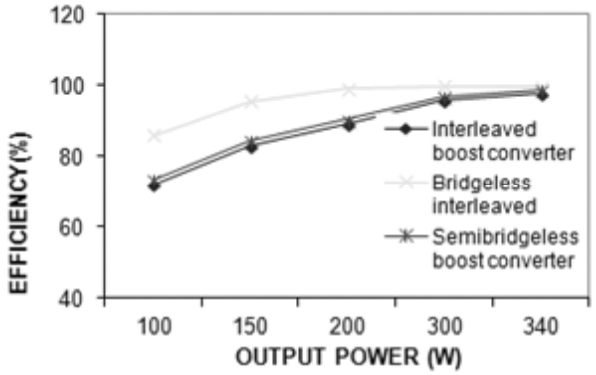



**Figure 10: Efficiency variation with output power**

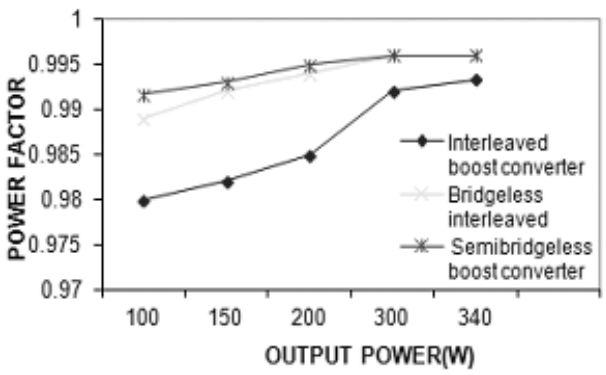



**Figure 11: Power factor variation with output power**

120%. On comparing the topologies, bridgeless interleaved PFC boost converter has power factor closer to 0.99 and efficiency 98% under half load and full load conditions. Thus bridgeless interleaved PFC converter is an optimal topology for Level–2 chargers for PHEV.

## 5. CONCLUSION

A survey aimed at evaluating the driven topologies used in front end ac/dc boost converters for Plug-in automotive applications is discussed in this paper. The performance characteristics of converter topologies with digital PI control under variable load conditions are scrutinized. The result shows that the bridgeless interleaved boost converter is an ideal topology for high power Level-2 charging applications.

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