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A Logic Sort Algorithm based Voltage Balancing of Modular Multilevel Converters in Back to Back HVDC Systems

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ABSTRACT

Modular multilevel converters (MMCs) break brought a breakthrough in the field of high and medium power applications, high voltage direct current (HVDC) is primer applications. The major MMC operational challenges allied with the control and voltage balancing of a sub module capacitor. This paper proposes a logic sort algorithm (LSA) for achieving the optimal value of a sub module capacitor to balance the voltage of MMC. Capacitor voltages are initializing from circulation of currents on upper and lower legs of MMC. MMC upper and lower arms capacitor voltages are measured and are formed in an array, optimum capacitor voltages are in each sub module arranged from the LSA. The LSA further compares the capacitor voltages in the array to obtain an optimal value for the sub module. Similarly by applying active and reactive power controllers to increase the efficiency of the system. This article aims to provide an exhaustive analysis on the design of MMC controller to achieve the optimal performance to improve the efficiency of the converter. The proposed method is tested using MATLAB Software for a five level MMC and the results are presented and analysed.

Keywords: Modular multilevel converter; HVDC applications; Proposed Logic sorting algorithm capacitor voltage balancing; active and reactive power controllers

1. INTRODUCTION

In the HVDC system conversion, MMC type voltage source converter (VSC) have distinctive advantages, mainly due to their excellent harmonic performance at higher voltages, independent control of active and reactive power in transmission lines, voltage control in wind farms, high modularity in their construction, simple scalability, usage of low cost filters, robust control schemes, and wider applications high voltage renewable. However, the MMC is superior to the VSC in many ways. Since MMC is scalable technology, it can be used in HVDC transmission voltages. The problem associated with simultaneous switching in a VSC is irrelevant in MMC. The switching frequency is lower for individual sub modules and hence the switching losses are lower to that of classical VSC. A major advantage of MMC over VSC is the variable voltage on the alternative current side is reduced because the voltage steps of the terminals are minor. The MMC with half bridge configuration cannot obstruct the fault currents at DC pole fault but full bridge sub module configuration is able to suppress. However, a trade off exists between the increased number of semi conductor switches and fault handling capability [1-7].

MMC have few operational issues associated those are sub module capacitance voltage balancing, circulating current suppression control and fault-tolerant process [8]-[10]. An investigated method is balance the sub module capacitor voltages can be summarized as: Generally, multi carrier PWM techniques are used to generate the pulse pattern in MMC. The main advantages of switching techniques are the low

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switching frequency and THD of the voltages. The low frequency modulation techniques are nearest level control (NLC) and similarly Selective harmonic elimination (SHE) [11]-[13]. Implementing of these techniques are the enough to balance the each capacitor voltages. A logical modulation algorithm based on independent both higher side and lower side modulations can help to balance the capacitor, and as well as it provide a method to generate each cell switching signals [14].The most commonly used voltage balancing strategies are based on the sorting algorithms. Conventional capacitor voltage balancing strategy which depends upon the polarity of the arm current has been reported in [15]-[17]. In [18], sorting algorithms with reduced switching frequencies have been proposed. ZixinLi [19] proposed Cross Phase Shift PWM technique to reduce 50 % voltage ripples compared with multi carrier PWM techniques by generating the pulse pattern in MMC. But high frequency modulation imposes to high switching losses compared with fundamental frequency modulation on the MMC. K.Ilves [20], proposed a predictive algorithm for equal distribution among all the sub modules and also proposed sorting algorithm for the reduction of ripples by 24%, when the capacitor voltage is maximum. Kui Wang [21][22] proposed a new MMC connection to reduce voltage oscillations in upper and lower legs connected to the middle of the leg.PedramSotoodeh [23] is proposed three conceptual functions those are active reactive power control, capacitor voltage balancing and generated PWM pulses. This active and reactive power controller is more popular to improve efficiency of converters.The proposed strategies provide an effective solution to avoid unnecessary switching transitions in the sub modules. The main focuses in MMC, Voltage balancing control strategy in each arm. Because of the arm current and the capacitor voltage error generate the modulation index in each cell. If the capacitor corresponding cell charges when error is positive, and if the capacitor of the corresponding cell discharges when error is negative. However, the voltage balancing accuracy is compromised [24]-[30].

In this paper, capacitor voltage balancing of a five level MMC is proposed using logic sort algorithm. This algorithm is applied to the lower arm and the upper arm of MMC. Capacitor voltages are arranged in array and positions are labeled as p, i and j where p represents the position of the first element (pivot element) of array, i represents the position of the element next to pivot element and j represents the position of the last element of array. This method generates optimum values of the capacitor for balancing the voltage of upper and lower leg connections of MMC. Similarly, active and reactive power controllers are incorporated with logic sort algorithm so this total system is developed and results are compared with a controller and without a controller. The intermezzo of the paper is outlined as follows. It deals with the general framework for the capacitor voltage balancing of a MMC, The proposed sorting algorithm has been discussed and reports the controller design and simulation results are discussed.

2. BASIC STRUCTURE OF MODULAR MULTILEVEL CONVERTERS

Fig. 1 represents the schematic diagram of a MMC-HVDC system. The MMC-HVDC system comprises of two similar MMC stations.

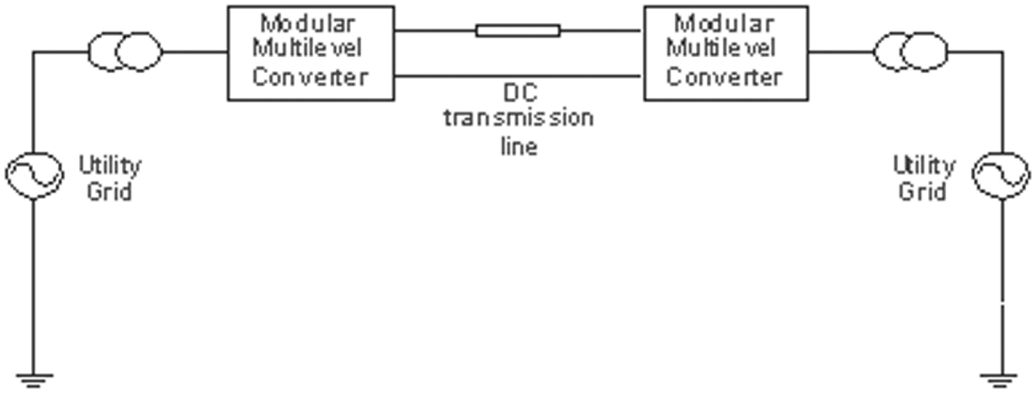

Figure 1: Back to Back HVDC system

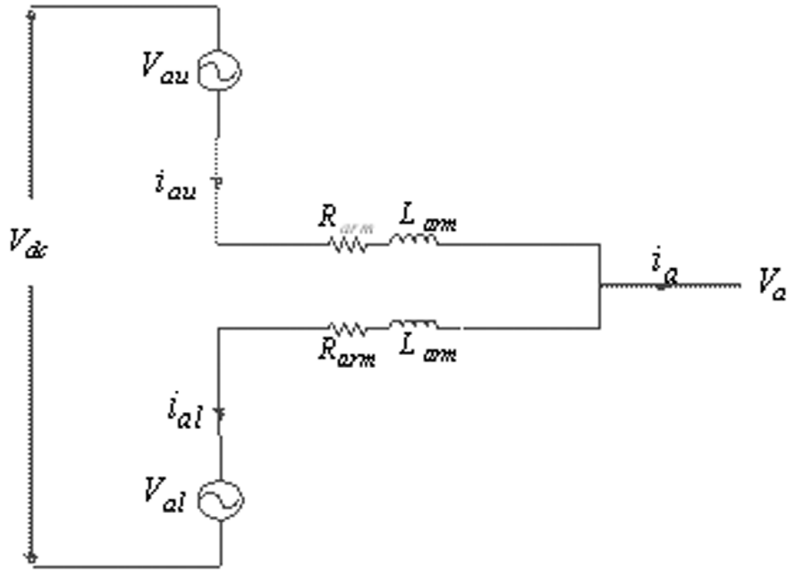

Figure 2: Equivalent model of MMC for phase a

Fig. 2 is the equivalent model of MMC for a single phase. The series connection of sub modules in an arm represents a controlled voltage source.

Applying the KVL to the converter arms of single phase in Fig. 2 yields:

$$L_{arm}\frac{di_{au}}{dt} + R_{arm}i_{au} + V_a - \frac{V_{dc}}{2} + V_{au} = 0 \tag{7}$$

$$V_a = \frac{V_{dc}}{2} - V_{au} - L_{arm}\frac{di_{au}}{dt} - R_{arm}i_{au} \tag{8}$$

$$-L_{arm}\frac{di_{al}}{dt} - R_{arm}i_{al} + V_a + \frac{V_{dc}}{2} - V_{al} = 0 \tag{9}$$

$$V_a = -\frac{V_{dc}}{2} + V_{al} + L_{arm}\frac{di_{al}}{dt} + R_{arm}i_{al} \tag{10}$$

The sum of (8) and (10) equations and also equations(2) & (4) gives

$$V_a = \frac{V_{al} - V_{au}}{2} - \frac{L_{arm}}{2}\left(\frac{di_{au}}{dt} - \frac{di_{al}}{dt}\right) - \frac{R_{arm}}{2}(i_{au} - i_{al}) \tag{11}$$

$$V_a = \frac{V_{al} - V_{au}}{2} - \frac{L_{arm}}{2}\left(\frac{di_a}{dt}\right) - \frac{R_{arm}}{2}(i_a) \tag{12}$$

Subtracting (8) by (10) equations:

$$V_{dc} = V_{au} + V_{al} + L_{arm}\left(\frac{di_{au}}{dt} + \frac{di_{al}}{dt}\right) + R_{arm}(i_{au} + i_{al}) \tag{13}$$

$$V_{dc} = V_{au} + V_{al} + 2L_{arm}\left(\frac{di_{cir}}{dt}\right) + 2R_{arm}(i_{cir}) \tag{14}$$

From equations (13) and (14), it is clear that by controlling the arm voltages, the ac side voltage for an inverter operation and DC side voltage for a rectifier operation can be controlled, which is the functionof MMC.

3. PROPOSED LOGIC SORTING ALGORITHM

Generally, the sub modules are switched ON depending upon the pulse pattern. At every instant, the reference signal is compared with a set of triangular carriers and the pulse pattern is generated irrespective of the capacitor voltages. With this generation, the sub modules which are to be switched ON or OFF cannot be determined specifically. This works well under normal conditions due to the cascaded connection of sub modules. However, in order to ensure a reliable operation in HVDC systems, the sub modules which are to be switched ON or OFF must be precise. This can be accomplished by adopting sorting algorithms for which the direction of arm current and the capacitor voltages acts as inputs. If the sub module is switched ON the arm current is positive then the capacitor charges and the capacitor discharges, if the arm current is negative then. If the sub module is OFF then the capacitor is bypassed. A correlation can be established between the arm current, capacitor voltages and the switching operation of the sub module through which a general sorting algorithm can be derived. During each control period, the capacitor voltages are measured and sorted.

The proposed selection algorithm is to be applied for an upper arm and the lower arm individually. It can be summarized as:

Step1: Input the capacitor voltages into an array a[N], where 'N' denotes the number of sub modules in an arm.

Step2: Assign the positions p, i, j where p represents the position of the first element (pivot element) of array, i represents the position of the element next to pivot element and j represents the position of the last element of array.

Step3: Compare a[p] and a[i]; if a[p]≥ a[i] then increment the value of i by 1; else return the value of i.

Step 4: Compare a[p] and a[j]; if a[p] < a[j] then decrement the value of j by 1; else return the value of j.

Step 5: Compare the values of i and j; if i< j then swap (a[i], a[j]); else swap (a[p], a[j]).

Step 6: After swapping, all the elements above the pivot element are lesser than the pivot element and the elements below the pivot element are greater than the pivot element. Thus, two sub arrays are formed.

Step 7: Recursively, apply the step 4 and step 5 to sort the sub arrays.

Step 8: Stopping criteria: Stop the process when all the elements appear in ascending order.

After sorting, the sub modules which are to be switched ON must be selected. The selection of the sub modules is dependent on the measured capacitor voltages and the arm current. The flowchart is an

Upper arm	Lower arm
Vc1=630V	Vc6=690V
Vc2=610V	Vc7=660V
Vc3=650V	Vc8=700V
Vc4=640V	Vc9=680V
Vc5=620V	Vc10=670V

Figure 3: capacitor voltage before sorting

implementation of capacitor voltage balancing strategy is shown in Fig. 4. An example to describe the selection procedure is as under. Let the number of sub modules in an arm be N = 5. The capacitor voltages of the upper arm are denoted as V_{c1} toV_{c5} and that of the lower arm are denoted as V_{c6} to V_{c10}. Before sorting, the capacitor voltages in the upper arm and the lower arm are as shown in Fig.3.

The proposed sorting algorithm is applied to the upper arm capacitor voltages and the voltages are sorted in ascending order as shown in Fig. 5.

The sorting algorithm is then applied to the lower arm capacitor voltages and the voltages are sorted in ascending order as shown in Fig. 6. The numbers of sub modules to be inserted in the upper and lower arms are determined by using an equation (5) and (6). After sorting, the capacitor voltages in the upper arm and the lower arm are as shown in Fig 7. Let the number of SMs to be inserted in the upper arm be $N_u = 2$. The direction of the upper arm current i_{au} is positive, so the sub modules with the lowest capacitor voltages i.e., SM2 and SM5 must be switched ON and all the remaining sub modules must be bypassed.The number of sub modules to be inserted in the lower arm be $N_l = N\text{-}N_u = 5\text{-}2 = 3$. The direction of the lower arm current i_{al} is negative, so the SMs with the highest capacitor voltages, i.e SM8, SM6 and SM9 are switched ON and the remaining sub modules can be bypassed. Selection of sub modules of phase a based on the proposed algorithm is presented in Fig 8.

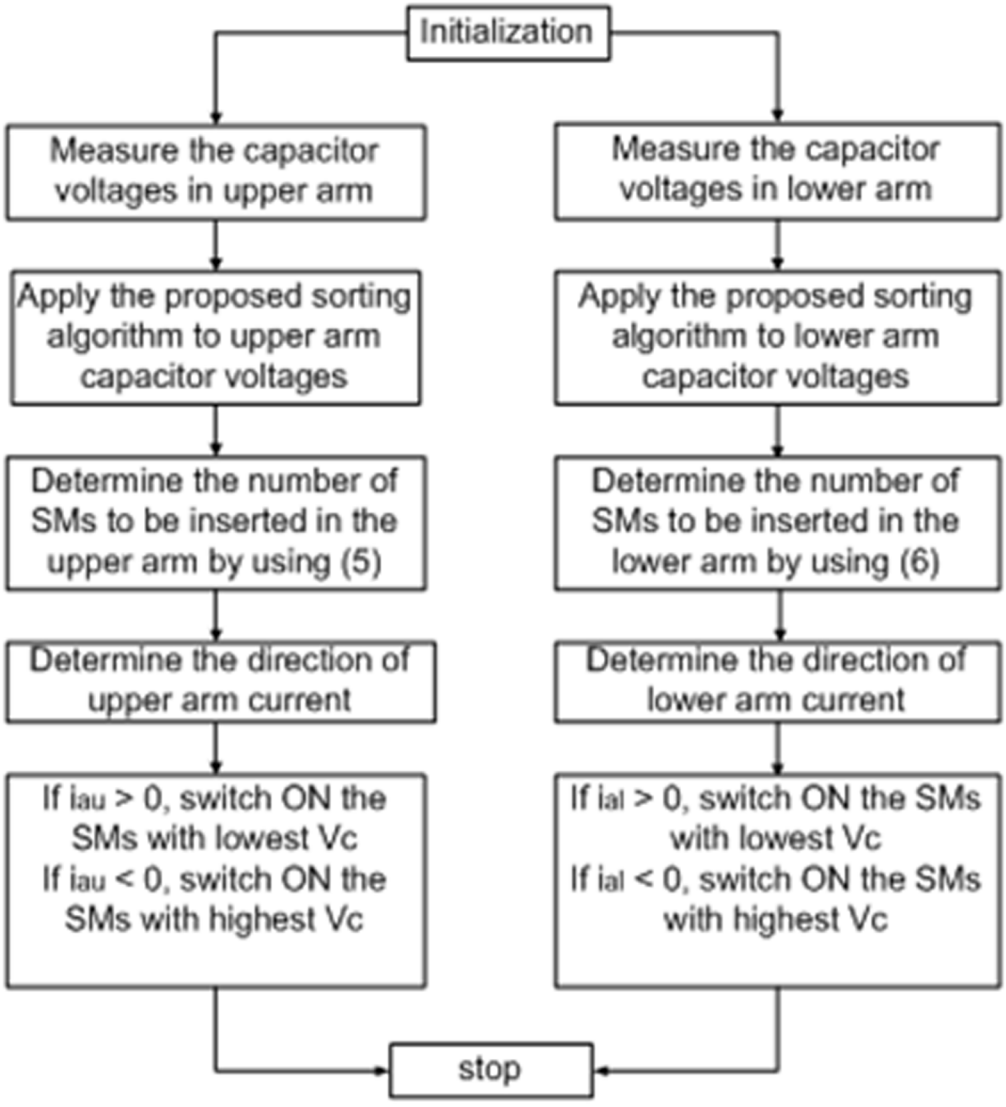

Figure 4: Flow chart for SM capacitor voltage balancing algorithm

4. CONTROL APPROACHES OF MMC

The primary control objective of MMC is to control the voltages and currents at its terminals. Since MMC is a potential candidate for HVDC applications, it must work as an effective energy interface. Furthermore, the secondary control objectives include mitigation of harmonics, control of active and reactive power, capacitor voltage balancing, suppression of circulating currents, reducing the switching losses etc. Therefore, to control the MMC, a controller which can accomplish the primary and secondary control objectives must be designed. A detailed control system which comprises of inner current control, voltage balance control and active-reactive power control is shown Fig. 9 shows the phase locked loop (PLL) which is used for the synchronization of the converter voltage. The PLL mechanism is able to detect the phase angle θ in coordination with the converter output voltage. In addition to synchronizing signals, the PLL can track the frequency also. In the PLL, the angle θ is obtained from the integration the angular frequency ω. Fig. 10 represents the inner current control.

P	0	630
I	1	610
	2	650
	3	640
J	4	620

$630 \geq 610\ T\ i\ ++$
$630 \geq 650\ F$ } $i = 2$
$630 < 620$ Fj = 4
i < j T
swap (a[2], a[4])

(a)

p	0	630
	1	610
i	2	620
	3	640
J	4	650

$630 \geq 620\ T\ i\ ++$
$630 \geq 640\ F$ } $i = 3$
$630 < 650\ T\ j\ --$
$630 < 640\ T\ j\ --$ } $j = 2$
$630 < 620\ F$
i < j F
swap (a[0], a[2])

(b)

p	0	620
	I	610
j	2	630
i	3	640
	4	650

$620 \geq 640$ Fi = 3
$620 < 630\ T\ j\ --$
$620 < 610\ F$ } $j = 1$
$620 < 610$ F
i < j F
swap (a[0], a[1])

(c)

p	0	660
j	1	670
	2	680
	3	690
i	4	700

(d)

Figure 5: (a)-(d) Sorting the upper arm capacitor voltages by using logic sort

p	0	690
i	1	660
	2	700
	3	680
j	4	670

$690 \geq 660\ T\ i\ ++$
$690 \geq 700\ F$ } $i = 2$
$690 < 670\ F$ $j = 4$
i < j T
swap (a[2], a[4])

(a)

p	0	690
	1	660
i	2	670
	3	680
j	4	700

$690 \geq 670\ T\ i\ ++$
$690 \geq 680\ T\ i\ ++$ } $i = 4$
$690 \geq 700\ F$
$690 < 700\ T\ j\ --$
$690 < 680\ F$ } $j = 3$
i < j F
swap (a[0], a[3])

(b)

p	0	680
	1	660
	2	670
j	3	690
i	4	700

$670 \geq 700$ F i = 4

$670 < 680$ T j −−

$670 < 660$ F $\Big\} j = 1$

i < j F

swap (a[0], a[1])

(c)

p	0	670
	1	660
j	2	680
	3	690
i	4	700

$680 \geq 700$ F i = 4

$680 < 690$ T j −−

$680 < 670$ F $\Big\} j = 2$

i < j F

swap (a[0], a[2])

(d)

p	0	660
j	1	670
	2	680
	3	690
i	4	700

(e)

Figure 6: (a)-(e) Sorting the lower arm capacitor voltages by using logic sort

Upper arm	Lower arm
Vc2 = 610V	Vc7 = 660V
Vc5 = 620V	Vc10 = 670V
Vc1 = 630V	Vc9 = 680V
Vc4 = 640V	Vc6 = 690V
Vc3 = 650V	Vc8 = 700V

Figure 7: capacitor voltages after sorting

In this control, the converter phase current in dq axis is compared with reference current command and the error is processed through a regulator to generate the voltage command. The reference current command I_{ref_dq} is obtained from active-reactive power control. The generated voltage is then limited and it is converted from dq reference frame to abc reference frame. Fig. 11 represents the active-reactive power control of the MMC.

This control block is used to track the current reference in dq axis. The instantaneous active and reactive power that flow within the converter cells is given by (15) & (16) equations. The power control acts in such a way that the current is controlled by a calculated reference value to assure that the active and reactive powers are set points as shown in Fig. 12.

$$P_{meas} = U_d I_d + U_q I_q \tag{15}$$

$$Q_{meas} = U_d I_q - U_q I_d \tag{16}$$

MMC has ability of energy balancing under unbalanced conditions. However, a DC voltage regulator unit is added which regulates the mean value of all DC link capacitor voltages. In this control, regulation of the mean value of DC link voltage, phase currents leads to the generation of balanced voltages in this control technique. The generated voltage command is obtained from the inner current control.

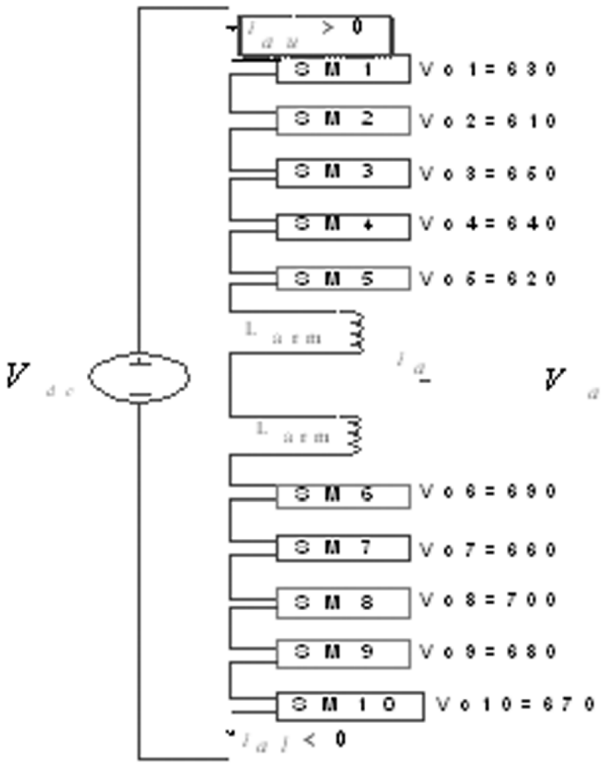

Figure 8: Capacitor voltages after Logic sort Algorithm

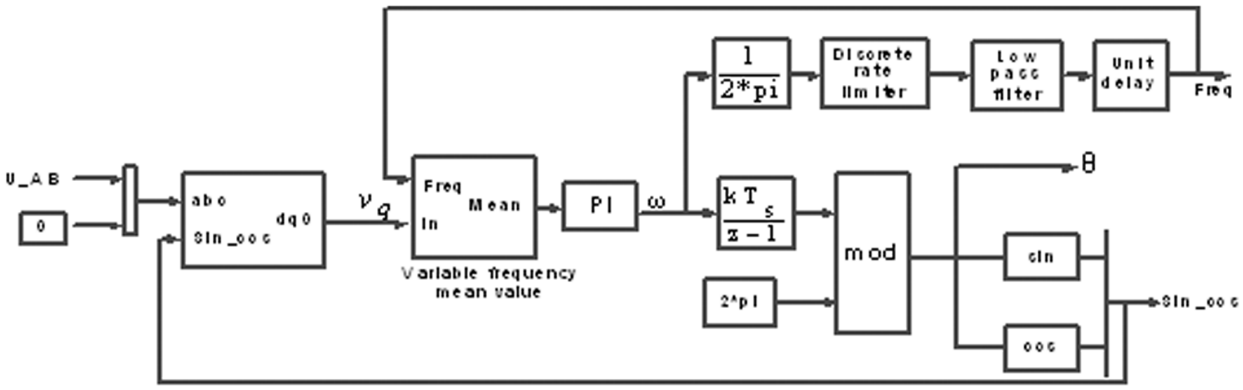

Figure 9: Phase locked loop

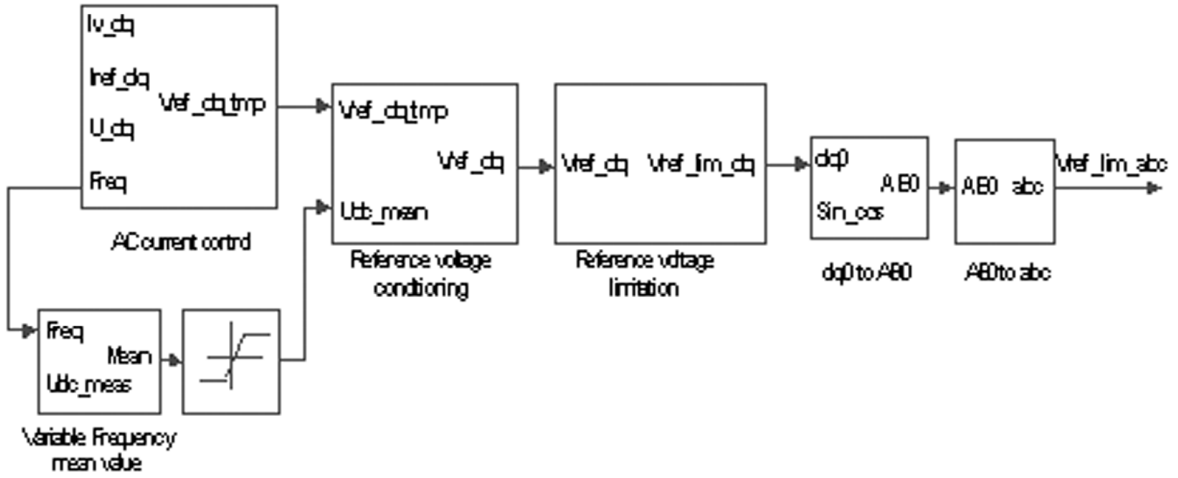

Figure 10: Inner current control

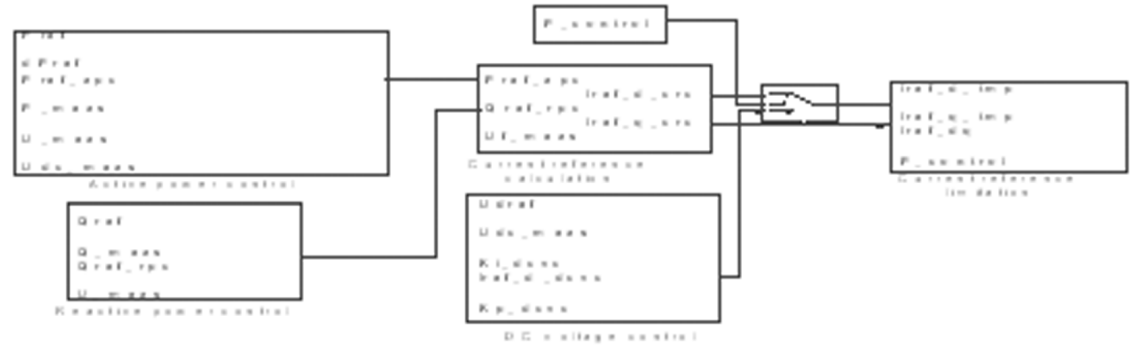

Figure 11: Active and reactive power control

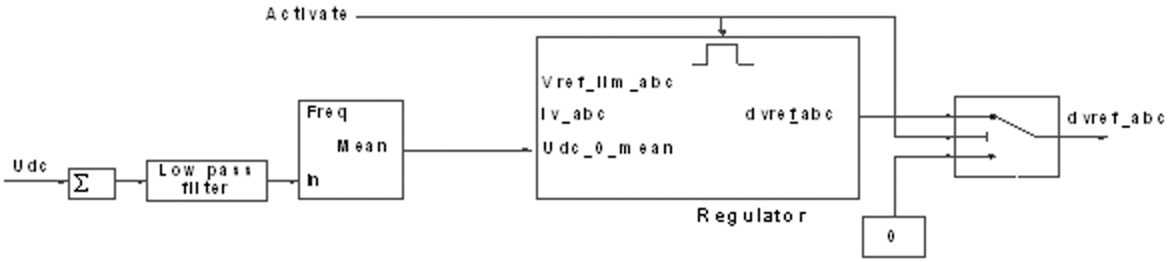

Figure 12: DC voltage balance control

5. RESULTS AND DISCUSSIONS

In order to verify the operation of MMC with the active, reactive power controller and LSA, a three phase MMC with two sub modules per arm is simulated in MATLAB software. The output voltages of MMC without a controller and with a controller are shown in Fig. 13(a) and Fig. 14(a) respectively. The output voltage of MMC with the controller exactly swings between the voltage levels $\frac{-V_{dc}}{2}$ and $\frac{+V_{dc}}{2}$. The THD of output voltage of a five level MMC without a controller is observed to be 21.02%. Generally, in order to reduce the THD the number of levels of the converter must be increased. But, instead of increasing the number of levels, the total harmonic distortion of the output voltage by implementing the proposed converter is observed to be 6.38%. Furthermore, it can be noted that the voltage ripple has been considerably reduced for MMC with controller. The phase currents of MMC without controller and with a controller are shown in Fig. 13(b) and Fig. 14(b) respectively. The THD of the phase current without and with controller is observed to be 12.32% and 1.79% respectively. The line currents of MMC without a controller and with a controller are shown in Fig.13(c) and Fig. 14(c) respectively. The THD of the line current without and with controller are observed to be 13.06% and 2.56% respectively. It implies that the integration of the proposed controller with the converter system can effectively reduce the harmonics, which is one of the desirable factors of MMC. It is observed that the active power and reactive power of the converter can be controlled through implementing the proposed controller. Fig. 13(d) represents the ac side the reactive power and the active power of MMC without a controller. The reactive power and the active power that flow within the converter are observed as 0.098MW and 0.275MVAR for the system in the absence of the controller. Moreover, the ac-side active power ripple is more predominant and it cannot be reduced. The active power and the reactive power of the converter with the proposed controller are shown in Fig. 14(d). With the introduction of the controller, the active power and the reactive power of the converter are observed as 0.115MW and 0.27MVAR.

Initially, the reference values of active and reactive power are set to zero. The active power ripple is considerably reduced with the adoption of the proposed control method. The input dc power of the converter without a controller and with a controller is maintained constant at 1.2MW as shown in Fig. 13(e) and Fig.

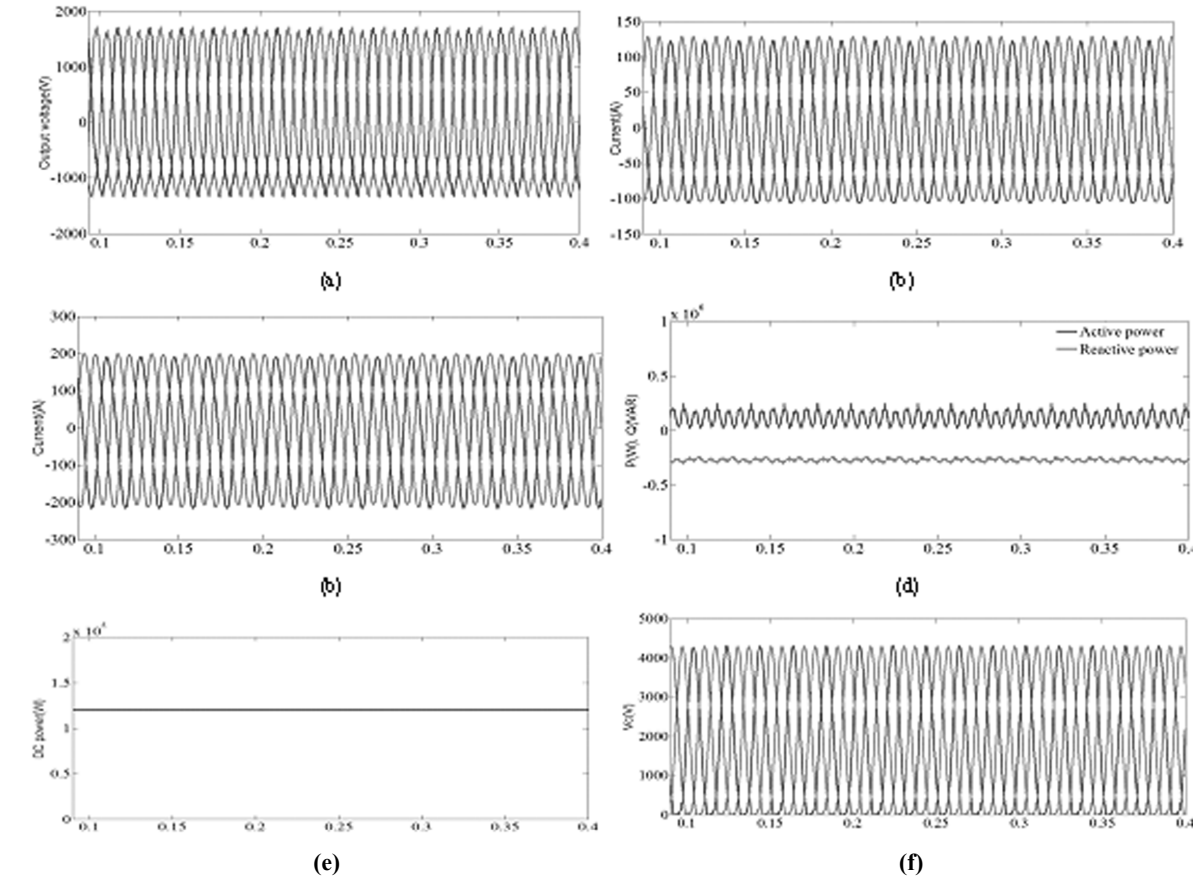

Figure 13: Simulation results of a three phase five level MMC without controller (a) AC side voltage (b) Phase currents (c) Line currents (d) Active and reactive power (e) DC power (f) Capacitor voltages

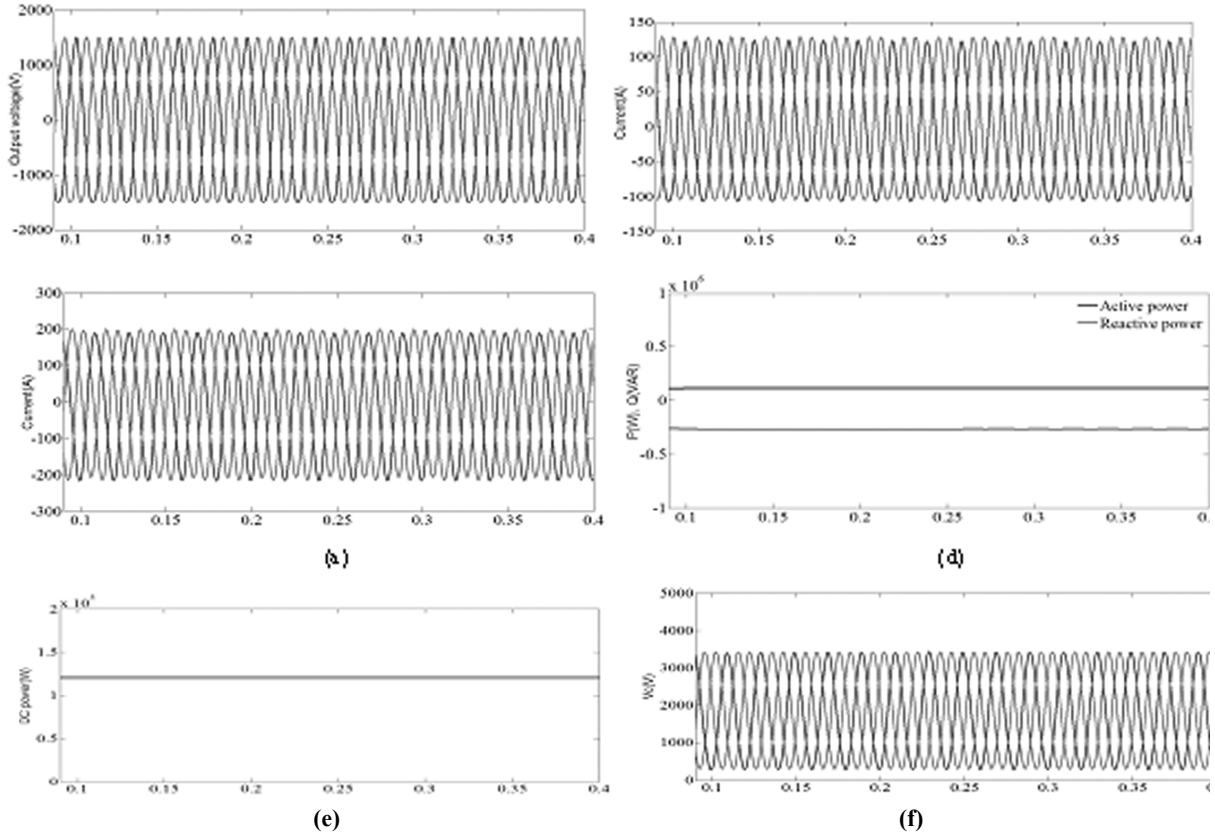

Figure 14: Simulation results of a three phase five level MMC with controller (a) AC side voltage (b) Phase currents (c) Line currents (d) Active and reactive power (e) DC power (f) Capacitor voltages

14(e). With the advent of the controller, the converter efficiency has been increased from 81.6% to 95.83%. The capacitor voltages are well balanced in the MMC by adopting the controller. The results of capacitor voltage balancing without a controller and with a controller can be observed in Fig. 13(f) and Fig. 14(f). From the obtained results the following conclusions can be made: the output voltage of the converter is controlled which is the primary control objective of MMC. The THD of ac voltage and current is within the permissible limits. The ac voltage and current has low harmonic content. The active and the reactive powers are controlled. The input DC power of the converter is regulated without any deviation. The converter efficiency has been improved which implies that the converter losses are reduced. The capacitor voltages are regulated and well balanced.

6. CONCLUSION

In this paper, a novel capacitor voltage balancing strategy has been proposed. Its presents and evaluates a voltage Logic sorting algorithm which enables the capacitor voltage balancing in MMC, demonstrates a control system based on a five level MMC. With the control system, all the control objectives of MMC can be accomplished. A comparison of MMC without a controller and with a controller has been presented. It is obvious that the converter with the controller exhibits a promising performance as compared with the converter without a controller. The results show that the overall efficiency of the converter has been enhanced with the use of a controller. Furthermore, the control characteristic of MMC renders it as the most potential configuration in high/medium power applications.

REFERENCES

[1] J. Rodriguez, J.S. Lai, and F.Z. Peng, “Multilevel inverters: A survey of topologies, controls, and applications,” IEEE Transactions on Industrial electronics, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[2] J. Rodriguez, S. Bernet, B. Wu, J. Pontt, and S. Kouro, “Multilevel voltage-source-converter topologies for industrial medium-voltage drives,” IEEE Transactions on Industrial electronics, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[3] R. Marquardt, “Modular multilevel converter: an universal concept for HVDC networks and extended dc-bus-applications” IEEE International Power Electronics Conference, pp.502-507,2010.

[4] M. Bahrman and B. Johnson, “The ABCs of HVDC transmission technologies,” IEEE Power Energy Mag., vol. 5, no. 2, pp. 32–44, Mar./Apr. 2007.

[5] B. Chuco and E. Watanabe,”A comparative study of dynamic performance of HVDC system based on conventional VSC and MMC-VSC,” IREP Symp. Bulk Power system Dynamics and Control, pp. 1–6, Aug. 2010.

[6] T. Modeer, H. P. Nee, and S. Norrga,”Loss comparison of different sub-module implementations for modular multilevel converters in HVDC applications,”European Power Electronics and Drives Journal, vol. 22, no. 3, pp 32–38, Sep. 2012.

[7] D. Deepak Chowdary and G.V.Nagesh Kumar, “Restoration of Single Phase Distribution System Voltage under Fault Conditions with DVR using Sliding Mode Control”, Indian Journal of Science and Technology, October 2008, Volume 1, No: 5, Page(s): 1-5, Gandhi nagar, Adyar, Chennai, India.

[8] LV Suresh Kumar, GV Nagesh Kumar. “Harmonic comparison with modular multilevel converter of multi connection wind energy systems.” Electrical, Electronics, Signals, Communication and Optimization (EESCO), 2015 International Conference on. IEEE, 2015.

[9] G. P. Adam, O. Anaya-Lara, G. M. Burt, D. Telford, B. W. Williams, and J. R. McDonald, “Modular multilevel inverter: Pulse width modulation and capacitor balancing technique,” IET Power Electronics, vol. 3, no. 5, pp. 702–715, Sep. 2010.

[10] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, R. Lizana “Circuit Topologies, Modelling, Control Schemes and Applications of Modular Multilevel Converters” IEEE Transaction on Power Electronics, vol. 30, no. 1, pp 4-17, January 2005.

[11] M. Sreedhar, D. Abhijit and M. Sambeet,”Voltage Balancing Scheme in MMC–A New Approach,” International Journal of Emerging Electric Power Systems, vol. 15, no. 4, pp. no. 389-399, Jul. 2014.

[12] K. Wang, Y. Li, Z. Zheng, and L. Xu, “Voltage balancing and fluctuation suppression method of floating capacitors in a new modular multilevel converter,” IEEE Trans. on Ind. Electron., no. 99, May 2012.

[13] J. Qin and M. Saeedifard, "Reduced switching-frequency voltage-balancing strategies for modular multilevel HVDC converters," IEEE Trans. on Power Del., Vol. 28, No. 4, pp. 2403-2410, October 2013.

[14] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, P. Barbosa, "Operation, Control, and Applications of the Modular Multilevel Converter: A Review," IEEE Transaction on Power Electronics, vol. 30, no. 1, pp. 37-53, Jan. 2015.

[15] M. Sreedhar, D. Abhijit and J. Shivaji,"A Survey and experimental verification of Modular Multilevel Converters," International Journal of Power Electronics and Drive Systems (IJPEDS), vol. 4, no. 3, pp. 363-375, Sep. 2014.

[16] M. Sreedhar and D. Abhijit, "Modular Multilevel Converters Part-I: A Review on Topologies, Modulation, Modeling and Control Schemes," International Journal of Power Electronics and Drive Systems (IJPEDS), vol. 4, no. 1, pp. 36-50, Mar. 2014.

[17] S. Du, J. Liu and T. Liu, "Modulation and Closed-Loop-Based DC Capacitor Voltage Control for MMC With Fundamental Switching Frequency," IEEE Transactions on Power Electronics, Vol. 30, no. 1, pp. 327-338, Jan. 2015.

[18] Li, Z., Wang, P., Li, Y. and Gao, F "A new single-phase five-level inverter with no problem of voltage balancing"In Energy Conversion Congress and Exposition (ECCE), pp. 2065-2071,EEE.sep 2011.

[19] Li, Z., Gao, F., Xu, F., Ma, X., Chu, Z., Wang, P., Gou, R. and Li, Y., "Power Module Capacitor Voltage Balancing Method for a±350 kV/1000 MW Modular Multilevel Converter"IEEE Transactions on Power Electronics, Vol. 31, no. 6, pp. 3977-3984, Jan. 2016.

[20] Ilves, Kalle, LennartHarnefors, StaffanNorrga, and H-P. Nee. "Predictive sorting algorithm for modular multilevel converters minimizing the spread in the submodule capacitor voltages."Power Electronics, IEEE Transactions on , vol.30, no.1 PP. 440-449, Jan 2015.

[21] Wang, Kui, Yongdong Li, Zedong Zheng, and Lie Xu. "Voltage balancing and fluctuation-suppression methods of floating capacitors in a new modular multilevel converter." Industrial Electronics, IEEE Transactions,vv.60, no. 5, pp.1943-1954, Jan 2013.

[22] Lie X, YongdongL, Kui W, Clare JC, Wheeler PW "Research on the amplitude coefficient for multilevel matrix converter space vector modulation"Power Electronics, IEEE Transactions,vol.60, Pp.3544-56. May 2013.

[23] Sotoodeh, P. and Miller, R.D. "Design and implementation of an 11-level inverter with FACTS capability for distributed energy systemsPower Electronics, IEEE Transactions, vol.2, no.1,Pp.87-96. Jan2014.

[24] M. Hagiwara and H. Akagi, "Control and analysis of modular multilevel cascade converter based on double-star chopper-cells (MMCC–DSCC)," IEEE Trans. Power Electron., vol. 26, no. 6, pp. 1649–1658, Jun. 2011.

[25] K. Wang, Y. Li, Z. Zheng, and L. Xu, "Voltage balancing and fluctuation suppression methods of floating capacitors in a new modular multilevel converter," IEEE Trans. Ind. Electron., vol. 60, no. 5, pp. 1943–1954, May 2013.

[26] E. Solas, G. Abad, J. Barrena, S. Aurtenetxea, A. Carcar, and L. Zajac, "Modular multilevel converter with different submodule concepts-part I: Capacitor voltage balancing method," IEEE Trans. Ind. Electron., vol. 60, no. 10, pp. 4525–4535, Oct. 2013.

[27] E. Solas, G. Abad, J. Barrena, S. Aurtenetxea, A. Carcar, and L. Zajac, "Modular multilevel converter with different submodule concepts-part II: Experimental validation and comparison for HVDC application," IEEE Trans. Ind. Electron., vol. 60, no. 10, pp. 4536-4545, Oct.2013.

[28] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," IEEE Trans. Power Del., vol. 25, no. 4, pp. 2903–2912, Oct. 2010.

[29] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses, and semiconductor requirements of modular multilevel converters," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2633–2642, Aug. 2010.

[30] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modelling, simulation and analysis of a modular multilevel converter for medium voltage applications," in Proc. IEEE Int. Conf. Ind. Techno., pp. 775–782, 2010.