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Design of Level Shifter for Multiple Supply Voltage SOC

R. Geethalakshmi* & K. Arun Kumar**

Abstract: Level shifter is an interfacing device playing a wide application in System On Chip (SOC) design. Modern SOC utilize Multi Supply Voltage Design (MSVD) because of their low static and dynamic power consumption. When a high voltage supplied cell of SOC is driven by a low voltage supplied cell then their occur error due to inability of low signal to drive a high voltage cell. For interfacing these two different voltage driven cells a level shifter is necessary between them. Since Multi Supply Voltage Design is adopted to reduce power consumption the added interfacing device should not degrade its value. In this paper I compared a variety of existing level shifter up-converting near/sub threshold level to super threshold levels in terms of power and delay. From the comparison I came to know DCVS level shifter be the best among all other level shifter circuit. Thus I proposed DCVS with NMOS diode current limiter level shifter to provide improved conversion range with less power consumption and reduced delay. CADENCE Virtuoso 180 nm CMOS technology is utilized for performing simulation, layout editing, RC extraction and post layout simulation.

Index Terms: Delay, dynamic power consumption, Level shifter, Multi Supply Voltage Design, static power consumption, System On Chip.

1. INTRODUCTION

Portable devices like mobile phones, laptop, digital camera etc., all they operate under battery, in which power consumption is one of the main criterion. The requirement of the customer is to operate these devices for a long period of time. In order to operate these devices for such a long period of time power consumed by these devices has to be reduced. Since CMOS transistor consume low power compared to all other transistor technology they are widely utilized in the design of portable devices. Further reduction of power is needed. Thus the power consumed by the CMOS circuit is to be considered here. The power consumed by the CMOS circuit is of two major categories one of which is static power consumption and another is dynamic power consumption. Static power consumption is mainly due to leakage current that will flow due to non ideal behavior of circuit which is negligible since it consumes 1% of total power consumption; the remaining is mainly due to dynamic power consumption. Dynamic power consumption is mainly due to two main components one is switching power arises due charging and discharging of the load capacitance, second is short circuit power due to non-zero rise and fall time of the input waveform [1]. Since dynamic power consumption contributes more to total power consumption of CMOS circuit it should be minimized to reduce power consumption in portable devices. Dynamic power consumption in CMOS circuit is given by

$$P(dynamic) = CV_{DD}^2F \quad (1)$$

C – Load capacitance.

V_{DD} – supply voltage.

F – Frequency of operation.

* Student, Saveetha Engineering college, Thandalam, Chennai, *Email: geetha0052@gmail.com*

** Assistant professor, ECE, Saveetha Engineering College, Thandalam, Chennai, *Email: arunkumar@saveetha.ac.in*

From the above equation (1) it is clear that dynamic power consumption depends on square the supply voltage. Thus reducing the supply voltage provides quadratic reduction in dynamic power consumption and static power consumption also reduced since gate leakage reduces.

$$T_p = \frac{CV_{DD}}{K(V_{DD} - V_{th})^2} \tag{2}$$

Tp – Propagation delay.

K – $\frac{\beta W}{L}$

V_{th} – Threshold voltage.

From the above expression (2) the propagation delay is inversely proportional to supply voltage V_{DD}. Reducing the supply voltage increase delay which significantly impacts on performance of the devices [2]. Thus voltage scaling is performed based on critical path i.e., circuit which are insensitive to delay are scaled down to VDDL whereas delay sensitive circuit operates at its normal supply voltage VDDH. Thus some cells in the SOC operate at the conventional voltage while other cells operate at scaled voltage leading to different supply voltage logic. This above stated phenomenon is said to be "Multiple Supply Voltage Design (MSVD)" [3] which is predominantly utilized in SOC because of it low static and dynamic power consumption in recent years. Even if the entire core cells in SOC operate at scaled voltage level we need to supply a normal supply voltage to IO pad cell which are digital usually supplied with 3.3 or 5V. Since input and output pad has to communicate with core cell for its proper function we need an interface between the core and IO pads.

Thus level shifter plays a significant role in SOC design. Level shifter provides communication between two different voltage domains without including any extra supply pins [4]. Several level shifters have been designed, analyzed and tested to provide a wide voltage conversion with low power and delay. This paper provides a comparison of a wide variety of level shifters for their extreme case of shifting between near/sub and super threshold levels, with less power consumption and reduced delay variation. A novel level shifter based on DCVS with NMOS diode current limiter is proposed here for its less power consumption and reduced delay. The future aim of this research is to utilize multiple threshold voltage concept in the proposed design that will be used to convert sub-threshold input with ultra-low power consumption and reduced delay.

This paper is organized as follows. Section II describes complete backgrounds of related work. Section III describes circuit and operation of various existing level shifter circuit. Section IV provides comparison of various level shifters. Section V describes proposed level shifter circuit. Section VI describes simulation result of proposed level shifter and layout design of proposed level shifter. Section VII concludes the paper.

2. RELATED WORK

Traditionally transistor sizing is preferred for optimizing power consumption. After that many research went to scale the supply voltage which results in quadratic reduction in dynamic power consumption. Since voltage scaling affect performance, the concept of dual supply design arises [5] where they utilized Clustered Voltage Scaling (CVS) approach to reduce power consumption. Since no level shifter is required when high voltage cell drives a low voltage cell. In CVS the entire cells are arranged in such a way that no high voltage cell is driven by low voltage cell. Thus CVS is based on a topological constraint which is difficult to implement in a large SOC. ECVS (Extended CVS) eliminate the topological constraint by allowing low

voltage cell to drive high voltage cell by inserting a level shifter between them. DCVS based level shifter is utilized for interfacing these dual supplies. DCVS based level shifter has two limitations one being a ratioed logic the sizing of the pull up and pull down network become critical and another one is contention which limits the speed.

In order to overcome these limitations of conventional level shifter several research works has been conducted [6]. Timing algorithm and power optimization technique has been exercised here to reduce the number of level shifter requirement. Timing algorithm called GECVS (Gate Extended Clustered Voltage Scaling) is utilized which combines both greedy and iterative optimization approaches. Here greedy algorithm is utilized to assign the supply voltage of all the gates to scaled supply voltage VDDL and the iterative optimization reassign the gates with speed dependency to standard supply voltage VDDH. Level shifter for low power application [7] here modification of conventional level shifter is done. In order to reduce the contention the drive strength of pull down network has to be improved. Thus stacking of NMOS transistor is implemented to improve drive strength of pull down network. As a result delay gets reduced but stacking leads to power penalty.

The variation of conventional level shifter is proposed in subsequent year such that current mirror, contention mitigate, Wilson current mirror level shifter [8] [9] [10]. Contention mitigate circuit also reduce the power by using quasi inverter pull down network thereby it reduces contention. Current mirror replaces the cross coupled pull up network by a current mirror load which is utilized when wide voltage conversion is required. Wilson current mirror is modification of current mirror circuit by adding additional PMOS to reduce leakage current that will flow when both pull up and pull down network turns ON same time leading to power dissipation. Level shifter circuit based on multi threshold design is proposed in [11]. Instead of using different logic in implementing level shifter the conventional level shifter logic is utilized but multi threshold CMOS is used here for low power and wide range voltage conversion. In order to provide fast, wide range and low power consumption a modified version of the level shifter using multi threshold design [11] is proposed in [12]. The comparison of these circuits has been provided in subsequent sections.

3. LEVEL SHIFTERS AND ITS OPERATIONS

The different forms of level shifter has been listed below

a) Dual Supply Level Shifter (DSLS).

b) Single Supply Level Shifter (SSLS)

c) Pass transistor half latch

d) Precharge circuit.

Among these Level Shifter circuits first two circuits has been widely used in SOC. DSLS has been widely used in SOC because of its wide range voltage conversion. SSLS also be used because of its layout compact ability. Pass transistor half latch and precharge are not widely used because of its small voltage conversion range and more power consumption of clock synchronizer respectively. Thus in this paper I concentrate only on DSLS and SSLS based Level Shifter.

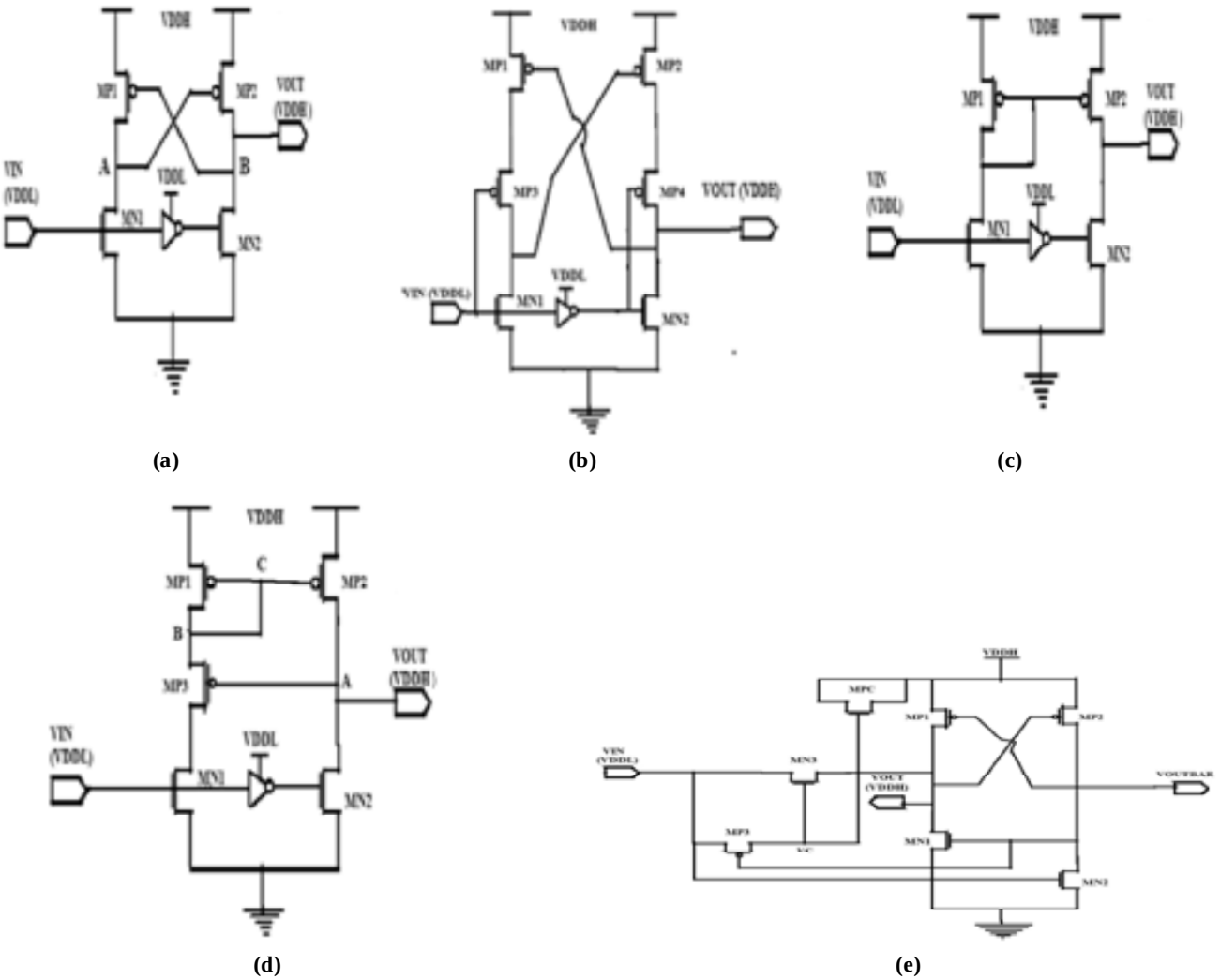
The DSLS itself can be implemented using several logic 1) Differential Cascade Voltage Switch Logic (DCVS). 2) Contention Mitigate. 3) Current Mirror. 4) Wilson Current Mirror.

The conventional level shifter is the Differential Cascaded Voltage Switch (DCVS) logic otherwise it is said to be cross coupled level shifter. The DCVS level shifter design is shown in Figure 1(a) which utilizes a positive feedback circuitry. The drive strength of NMOS transistor has to be increased to overcome the leakage caused by weekly conducting PMOS transistor. Thus NMOS has to be properly sized to perform proper function. Thus DCVS is a ratioed logic. One research [4] has been proven that the required NMOS

to PMOS ratio grows exponentially when lower supply voltage scales down because the pull down transistor has to drive low voltage whereas pull up half latch is at high voltage the sub threshold on current may flow when the ratio get mismatched. For converting sub threshold to above threshold voltage in 90nm technology NMOS to PMOS ratio of ~2400 is required.

In order to overcome the limitation of DCVS several solution has been proposed one of which be contention mitigate level shifter in which a quasi inverter logic is adopted in pull down network Figure 1(b) to increase drive strength of pull down network. Here the input is applied to the quasi inverter instead of applying it to the NMOS compared to DCVS logic. Delay variation due to different current driving capability is eliminated in this design.

Figure 1(c) shows level shifter that uses current mirror load. The current driving capability of DCVS depends on the the gate to source voltage (Vgs) of MN1 and MN2 which depends on VDDH whereas in current mirror saturation current of MP1 decides current driving capability. Thus in current mirror stable current driving capability is obtained because it is not affected by IO voltage or VDDH or threshold voltage. This circuit is mainly utilized for wide range voltage conversion. Since current mirror level shifter has these feature they not used in wide application because of its high leakage power consumption due leakage current that will flow when the input is in supera threshold. Thus power consumption in current mirror level shifter is high compared to that of conventional level shifter.



(a) **(b)** **(c)**

(d) **(e)**

Figure 1: Conventional level shifter using (a) Differential Cascaded Voltage Switch (DCVS) (b) Contention Mitigate (c) Current Mirror (d) Wilson current mirror (e) Single supply level shifter.

In order to eliminate the leakage current in current mirror level shifter, wilson current mirror level shifter Figure 1(d) has been proposed. The Wilson current mirror has an additional PMOS which ensures no leakage current at supra-threshold input. Since this PMOS MP3 turns off either the MP1 or MN1 turns ON eliminating the static current path from VDD to VSS. The delay in Wilson current mirror level shifter is more compared to that of conventional level shifter.

So far I discussed several level shifters which are Dual supply level shifter it utilize both the low and high supply line which become difficult during physical design. In order to make routing flexibility and compact ability the single supply level shifter has been proposed Figure 1(e). In single supply level shifter only the high supply line alone is utilized. Thus single supply level shifter has advantage of reduced pin count, routing congestion and cost of system. Apart from these advantage single supply level shifter has nothing to add regarding voltage conversion. It dissipates more power due leakage current and also more delay.

4. COMPARATIVE ANALYSIS

From the comparison table the following thing I infer, The DCVS logic i.e., conventional level shifter designed for voltage level shifting contain less number of transistor compared to all other level shifter design, power and energy consumption is also less compared to other level shifter design. Thus I took this cross coupled level shifter for further reduction power and delay.

TABLE 1
QUALITATIVE COMPARISON OF VARIOUS LEVEL SHIFTER DESIGN

Criterion	*DCVS*	*Contention mitigate*	*Current mirror*	*Wilson current mirror*	*Single supply*
Less no. of transistor i.e., area	√		√		
Wide conversion range	√		√	√	
Low power consumption	√			√	
Less Energy consumption	√			√	
Less propagation delay		√	√		√

5. PROPOSED SYSTEM

The proposed Level shifter is shown in Fig 2 which includes the conventional level shifter with NMOS current limiting diode. The modification is done to provide a wide voltage conversion with less power consumption and reduced delay variation. Here the modification is provided in voltage conversion stage where a NMOS current limiter is added in pull up network. Current limiting diode limits the current over a wide voltage range. Current liming diode is obtained by shorting the gate and the source of NMOS transistor function similar to that of zener diode. One difference is that zener diode is a voltage regulator whereas current limiting diode is a current regulator. Current limiting diode allows a current to vary linear with voltage to specific value, when that specific value is reached current become constant with increase in voltage. Thus by utilizing current limiting diode in DCVS, reduces the power consumption.

When the input VIN changes from low (0) to high (VDDL), the internal point N1 is grasped to ground despite of the weak strength of the pull-down device. MP2 turns ON due to the ground potential at its gate. Thus the supply voltage of VDDH is connected to the output buffer and the output VOUT be the pulse of low (0) to high (VDDH). Similarly when input changes from high (VDDL) to low (0) MN1 turn off and the MN2 turn ON because of the inverted input at its gate here internal node N1 charges immediately to VDDH because of turned ON MP1 due to ground potential from MN2. High potential at N1 cause MP2 turns OFF

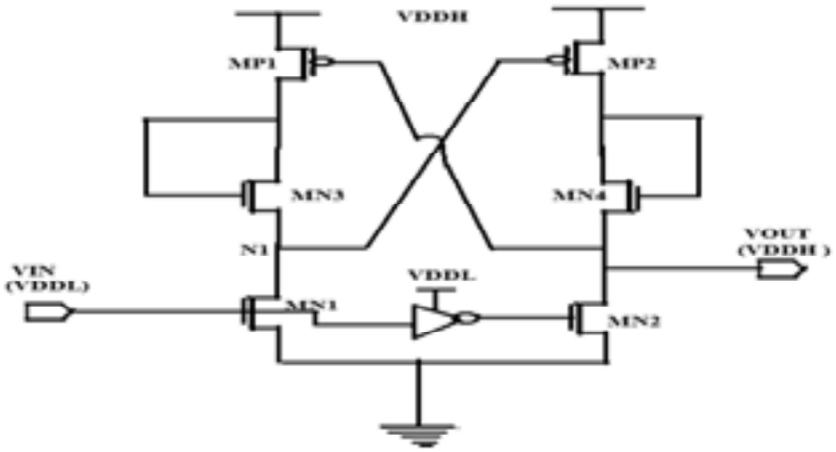


Figure 2: DCVS with NMOS Current Limiting Diode

immediately causing ground to be connected to output buffer and the output VOUT be the pulse of high (VDDH) to low (0).

The conventional level shifter cannot convert voltage below 1V because of PMOS to NMOS ratio. In order to make conventional level shifter to convert voltage below 1V size of PMOS and NMOS has to be ratioed in such a way to make NMOS drive such a low voltage. The research work [5] states that for 90nm technology the ratio of PMOS to NMOS is ~2400 for converting sub-threshold voltage level. The inclusion of diode current limiter improves the drive strength of NMOS transistor. Here I utilized the same size for both PMOS and NMOS. Since the size are identical there will be no ratioed logic issue in the proposed level shifter design and also the same circuit is capable of converting voltage below 1V with reduced power conversion and delay. The proposed level shifter design has been simulated, provides conversion range of 0.8 to 5V which is wide when compared to that of conventional DCVS. The power and delay estimated from the simulated result also give better performance value.

6. EXPERIMENTAL RESULTS

The proposed level shifter circuit is implemented using cadence 180nm CMOS technology and the spectre tool is utilized for simulation, The Fig 3 shows the simulated results of proposed level shifter. Here the input voltage of 0.8V VDDL is provided to level shifter which provides an output of 5V after shifting. The proposed level shifter is examined for power, energy and delay variation. The result of the examination provides the power consumption of 60.6ìW, energy consumption of 25.45pJ, delay of 371.2pS. Thus

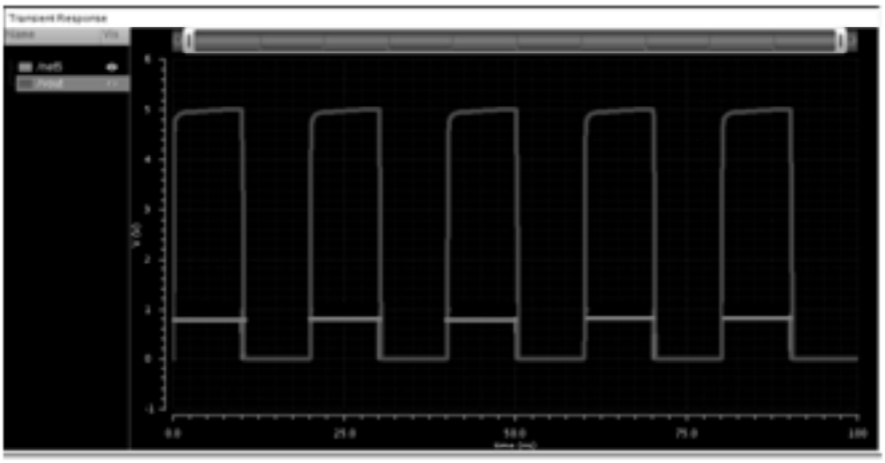


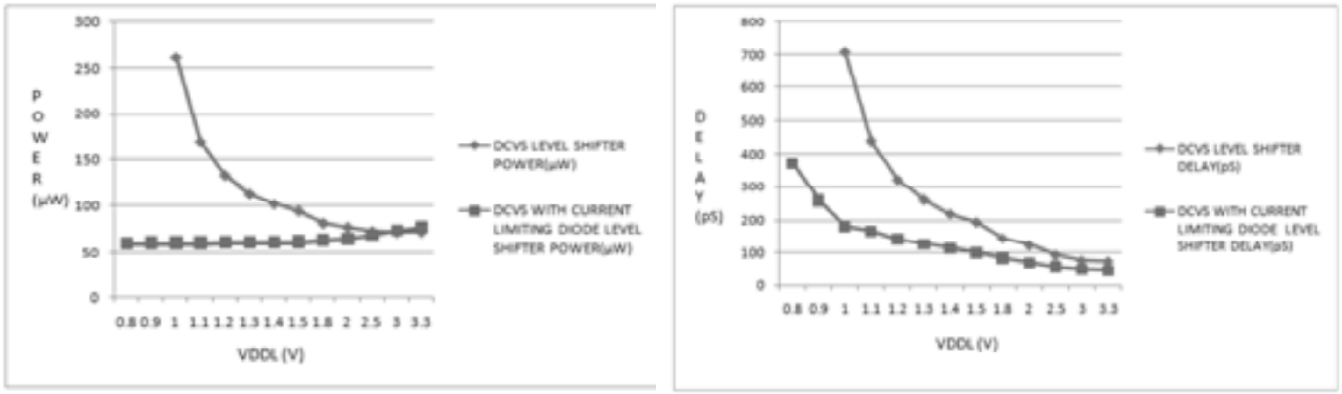
Figure 3: Simulation Result of DCVS with diode current limiter

comparing with conventional level shifter the conversion range is thrice improved in the proposed level shifter. The power and delay variation of DCVS and proposed level shifter are measured.

From the simulation results the power and delay of DCVS and DCVS with current limiting diode is compared at the standard supply voltage VDDH of 5V. The average power consumption of DCVS and DCVS with current limiting diode level shifter against the scaled supply voltage is shown in the fig 4(a). The propagation delay of DCVS and DCVS with current limiting diode is shown in the fig 4(b). From the plotted graph we can observe that the proposed DCVS with current limiting diode is the robust comparing with the DCVS level shifter. The power consumption of the proposed level shifter decrease when the conversion range increases. The propagation delay which is nothing but average of rise and fall time delay has been plotted against VDDL which clearly shows that proposed level shifter is the best compared with the conventional level shifter.

The physical design of the proposed level shifter is designed using cadence virtuoso 180nm CMOS technology. is shown in the fig 5 where the two NMOS pull down devices, two NMOS current limiting diode, two PMOS pull up devices, and finally inverter logic is created.

Robust level shifter design requires both VDDL and VDDH to be power supply has to be supplied to the cell. Since SSLS requires only VDDH to be routed they suffer from a problem of delay and leakage. An



(a) **(b)**

Figure 4: Simulation results (a) Average power of the proposed and conventional level shifter against scaled supply voltage. (b) Propagation delay of proposed and conventional level shifter against scaled supply voltage (VDDL).

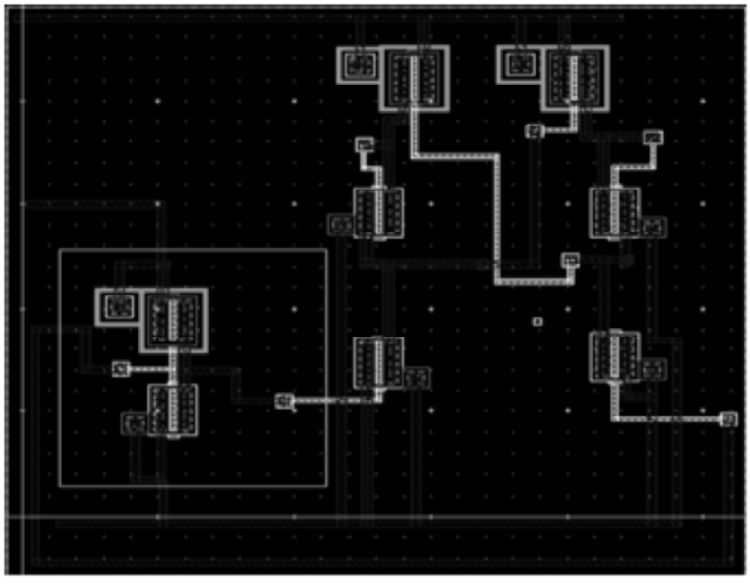


Figure 5 Layout of Proposed Level Shifter.

alternate solution is to implement the dual-rail cell in which the two supply lines made to route side-by-side in order to provide the two voltages to the cell. Unfortunately such a layout does not coincide with the conventional ASIC standard-cell routing. In this work, I employ a double-cell-height architecture in which VDDL and VDDH supplies are provided at the top and the centre metal-1 rails, respectively, while the ground rail travels at the bottom of the cell. The width of the ground rail is twice the width of the other rails in order to have consistent abutment with neighboring single-height ASIC cells [5]. Note that the use of the double-height layout strategy allows well-sharing between PMOS transistors driven by the same power supply in different standard-cell rows, thus leading to more compact system layouts Signals routing have been realized using only metal layers 1, thereby keeping the other metal layers available for interconnections on higher abstraction levels.

The post layout simulation is performed to verify the performance of proposed level shifter in the presence of parasitic effects. The power and delay has been estimated after the post layout simulation which provide satisfied performance.

7. CONCLUSION

In this paper I conclude that the conventional level shifter i.e. DCVS contain advantages of less number of transistor, low power and energy consumption. Only drawback of DCVS is more delay variation due to contention. Thus DCVS level shifter has been modified to reduce contention. The proposed DCVS level shifter provides a voltage conversion of 0.8 to 5V with Power consumption of 60.6ìW, Energy of 25.45pJ and delay of 371.2pS. The simulation results of the DCVS with diode current limiter level shifter in a 180nm process technology show that the circuit topology offers good performance, low power dissipation and delay. The layout of this proposed DCVS level shifter circuit, RC parasitic extraction and finally post layout simulation provide better result compared to conventional DCVS. Further I have an idea to implement the multi threshold concept in my design to provide sub threshold conversion.

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