Cascaded H-Bridge Multilevel Inverter

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ABSTRACT

This paper Presents design and simulation of a cascade H bridge multilevel inverter using sinusoidal pulse width modulation technique. The purpose of multilevel inverter is to generate stair case sinusoidal pulse using different DC Supply. In this paper we generate carrier based SPWM scheme using PD, POD, APOD compare it for five level and seven level by doing FFT analysis in order to find optimized output voltage quality. The MATLAB, Simulink result shows that seven level inverter voltages has less total harmonic distortion in comparison with five level inverter.

1. INTRODUCTION

Ac loads may require constant or adjustable voltage at their input terminals. When such load fed by inverter, it is essential that output voltage of the inverter is so controlled as to fulfill the requirement of Ac load [1]. The concept of multilevel inverter has been purposed on 1975. The purpose of multilevel inverter to generate desired multi-staircase single or three phase voltage by combining several DC voltage sources. Solar cells, fuel cells, batteries and ultra-capacitors are the most common independent sources used. One important application of multilevel converters is focused on medium and high-power [2]. In multilevel inverter the term level is referred to as the number of node to which the inverter can be accessible [3]. In this output voltage can be defined as voltage Dr. Ajay Kumar Bansal.

Across output terminal of the inverter and the ground point and input node voltage and Current is referred to input terminal of the inverter with reference to ground. The structural switches, be capable of withstanding very high input voltage for high power application and lower switching frequency for each switching device.

Multilevel inverter is replacing conventional inverter and step-up transformer because of its upgrading features like increment in output voltage and power does not require an increase in rating of individual device.

1.1. 3phase Cascaded H bridge Multilevel Inverter

Cascade H-bridge is new advance exiting technology of dc to ac conversion system. In 3phase system a single leg of cascaded H-bridge represents a phase. In cascaded H bridge inverter H bridge are connected in series connection, number of H bridges depends on required level. Number of bridge of bridge is defined by H, number of Level defined by M and number of switch is defined by S.

Number of bridge required for M level is equal to $H = \dfrac{M-1}{2}$.

Number of switch required for M level inverter is equal to $S = 2(M - 1)$

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For example A five level inverter required H-bridge is equal to $\dfrac{5-1}{2} = 4$

Number of Switch required are $2(5 - 1) = 8$.

Fig. 1 shows fundamental construction of 3phase 3level cascade H Bridge here each leg of inverter represent each phases. Dc voltage is equally distributed in every leg of inverter. Each leg contain eight switches and whole inverter twenty four switches.

2. VOLTAGE CONTROL OF MULTILEVEL INVERTER

There is various method of voltage control.

1. Single–pulse-width modulation
2. Multilevel-pulse–width modulation
3. Sinusoidal pulse–width modulation
4. phase-displacement control

In proposed model SPWM technique is used for controlling the output voltage of inverter.

3. SINUSOIDAL PULSE WIDTH MODULATION

SPWM technique commonly used for industrial purpose. In this technique gating signal are generate by comparing the sine wave with triangular carrier wave.
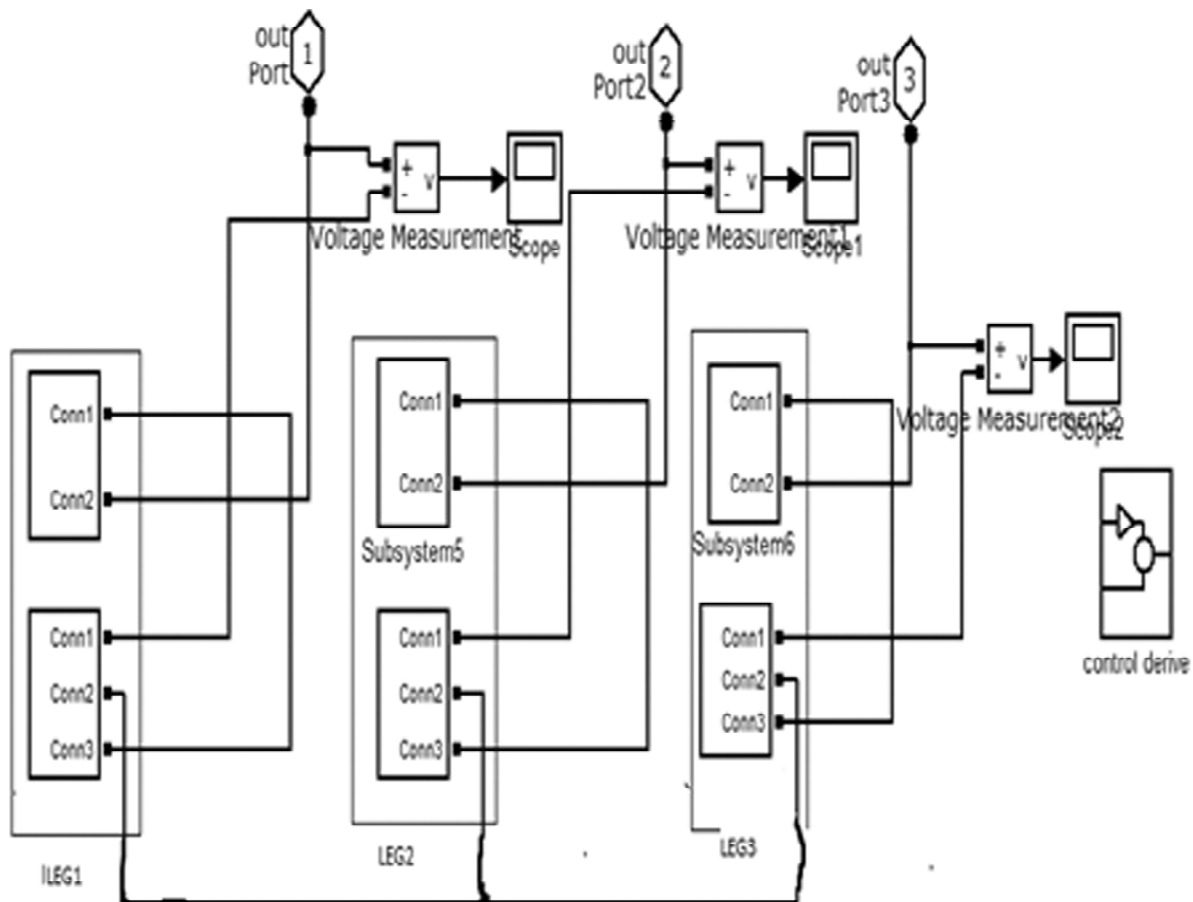
Figure 1: Fundamental construction of 3Level 3phase cascade H bridge

The frequencies of reference signal determine the inverter output frequency f_0 and its Peak amplitude A_r control the modulation index. The Amplitude modulation index is denote by Ma is equal to is the ratio of carrier wave Amplitude to modulated Amplitude.

3.1. Calculation for Madulation Index

FOR five level CHB

Madulation index = *Mcr/Mm*

$$314/315.4$$

$$M = .99$$

$$M \cong 1$$

FOR seven level CHB

Madulation index = *Mcr/Mm*

$$314/313.9$$

$$M = 1$$

The tigring circuit is designed is based on Three phase voltage control there are three reference voltage waves (v_{ra}, v_{rb}, v_{rc}) each shifted by 120^0[4],[5] for carrier wave source parameter, the time value of each carrier wave set as [0 0.0005 0.001] while output value set according to the disposition of carrier wave. After comparing, The output signal of comparator transmitted to igbt.
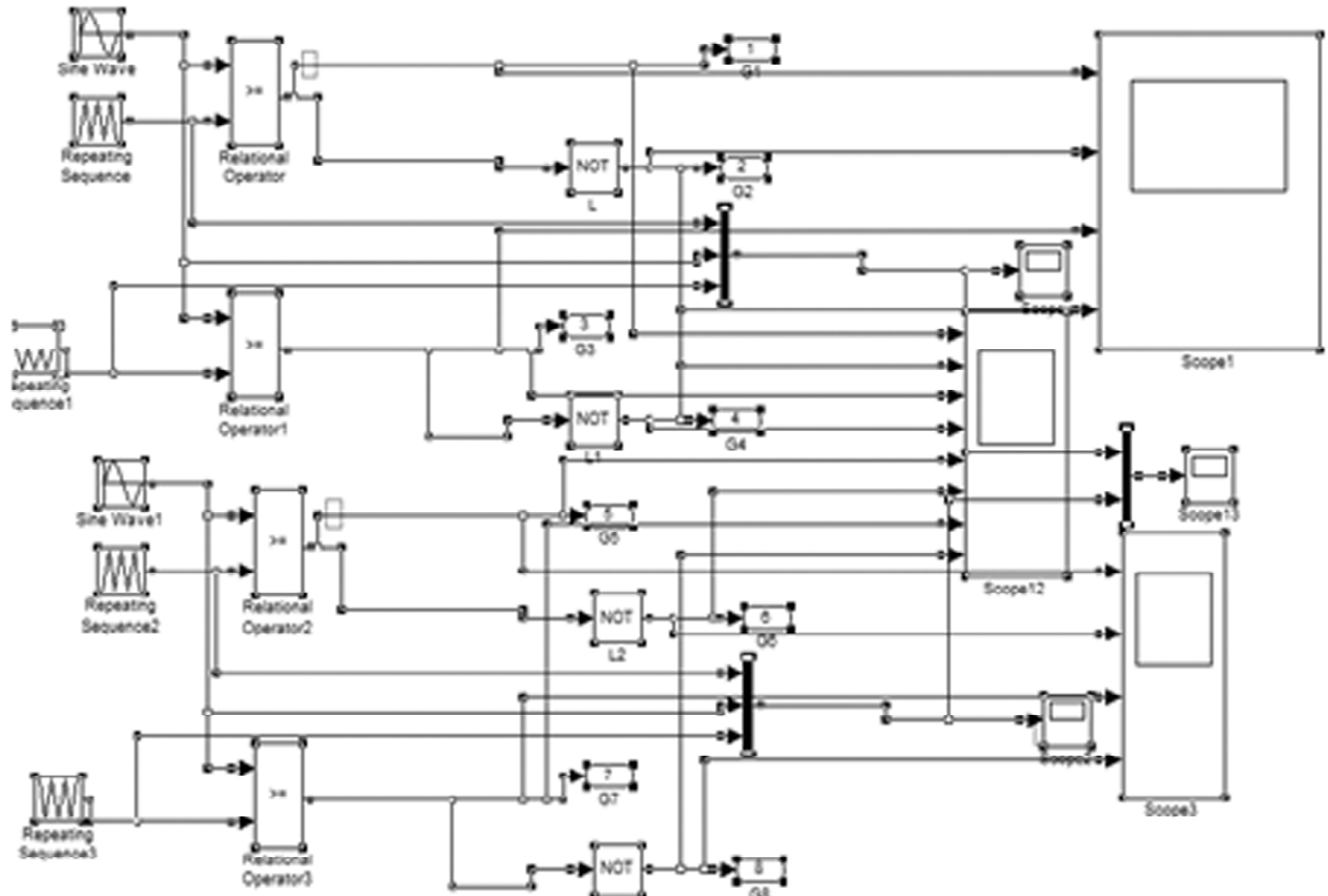
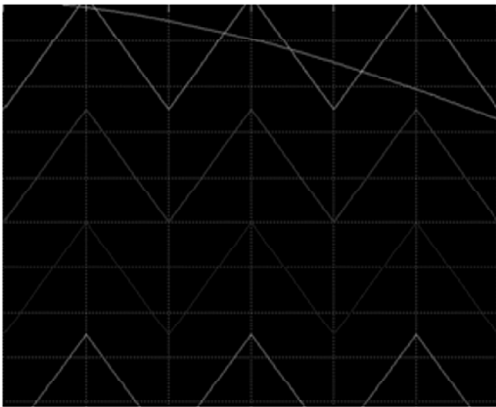**Figure 2: Show the tiggering circuit**
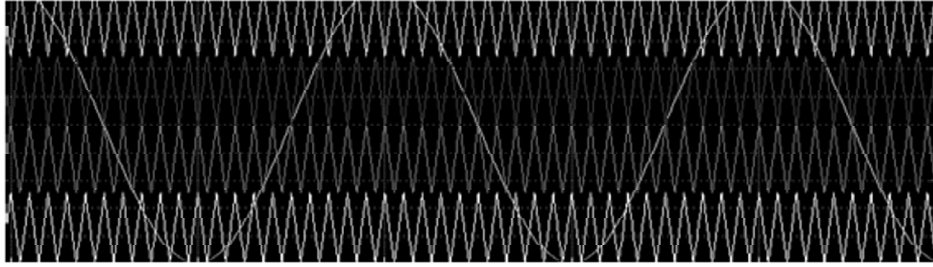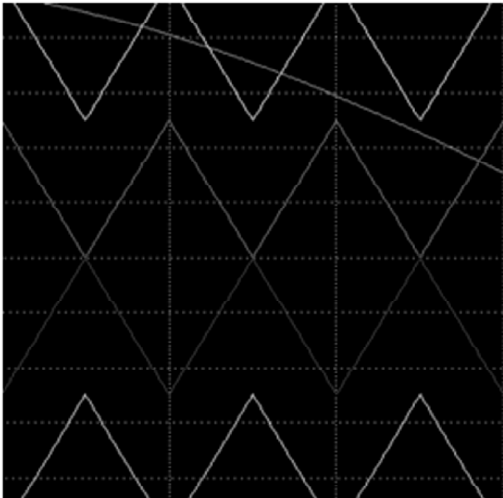
Figure 3: (spwm wave for one leg)

4.   TYPES OF CARRIER BASED PWM TECHNIQUE

Basically there are five tenchiques present like PD, POD, APOD, COPWM, VFPWM.In this paper comprsion of three technique PD, POD, APOD is done.
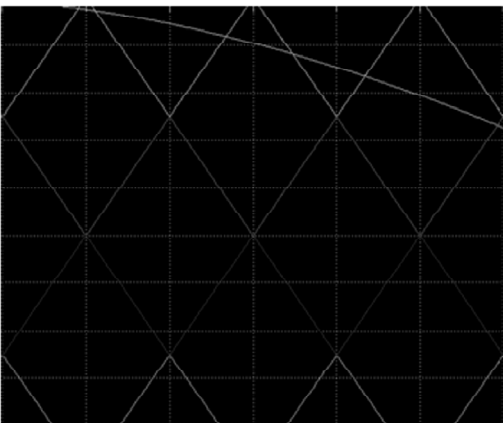

a) **Phase disposition carrier waveform**

   In this technique all carrier wave in same phase.

b) **Phase opposition Disposition**

   In technique the carrier wave above the zero reference in phase shifted by 180^0 by those wave below the zero reference.

c) **Alternate ohase opposition and disposition**

   In this type every carrier wave is in out of phase with its neighbor carrier shifted by 180^0.

5. DESIGN OF FIVE LEVEL AND SEVEN LEVEL CASCADED H-BRIDGE INVERTER

Fig. 4, 5 shows fundamental construction of 3phase 7level cascade H Bridge here each leg of inverter represent each phases. Dc voltage is equally distributed in every leg of inverter. Each leg contains twelve switches and whole inverter thirty six switches.
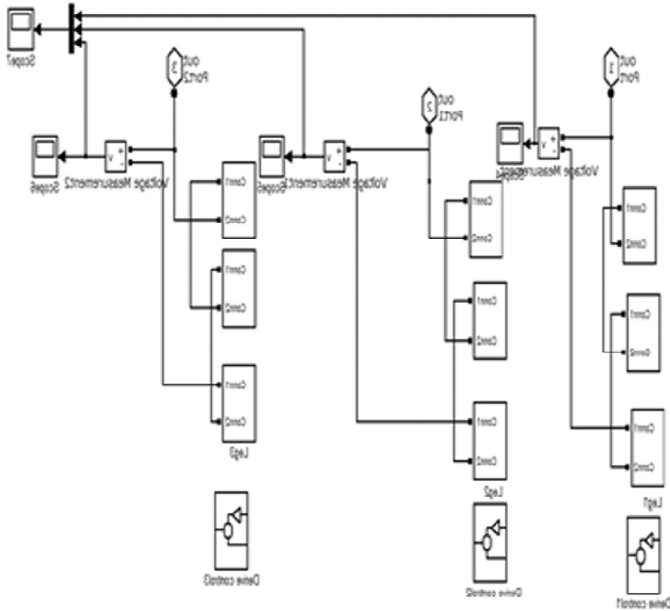

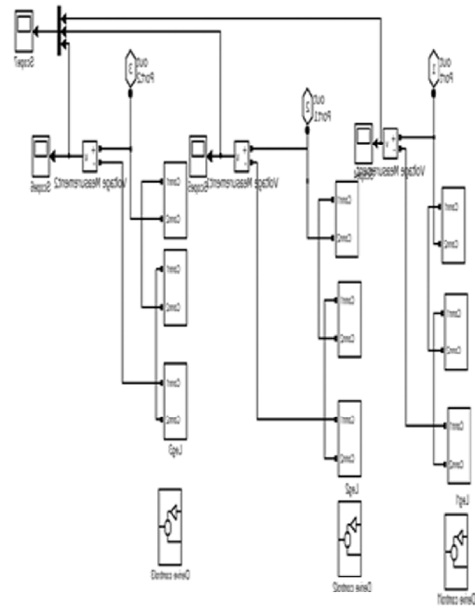**Figure 4: Fundamental construction of 7level h bridges inverter**

Figure 5: Fundamental construction of 7 level h bridges inverter
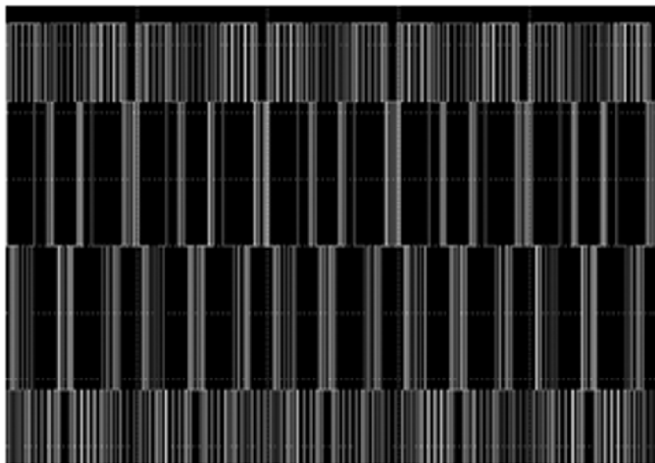

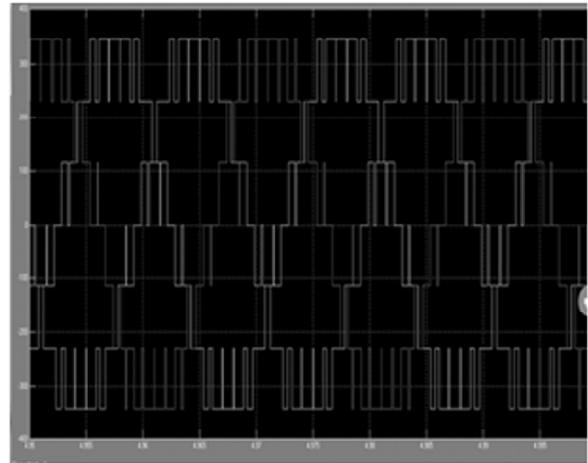**Figure 6: Output wave of 5level h bridge inverter**

Figure 7: output wave form of H bridge seven level h bridge inverter

6. SIMULATION RESULT

Simulation studies are performed by using matlab simulink.following parameter used for simulation

$$Vdc = 315$$
$$Fc = 314$$
$$Load = \text{induction motor}$$

Rs = 0.1589,   Rr = 0.2447

Lm = 60.6639e-3,   Lr = 63.456e3,

Ls = 62.6956e-3

Fig. 8, 9, 10 show output wave form of five level inverter at PD, POD, APOD respectively and total harmonic distortion is 26.86%,27.38% and 25.59% respectively. For seven level total harmonic distortion is 17.92%,16.01%and 17.45 respectively.

Five Level Inverter Voltage THD at various switching patter
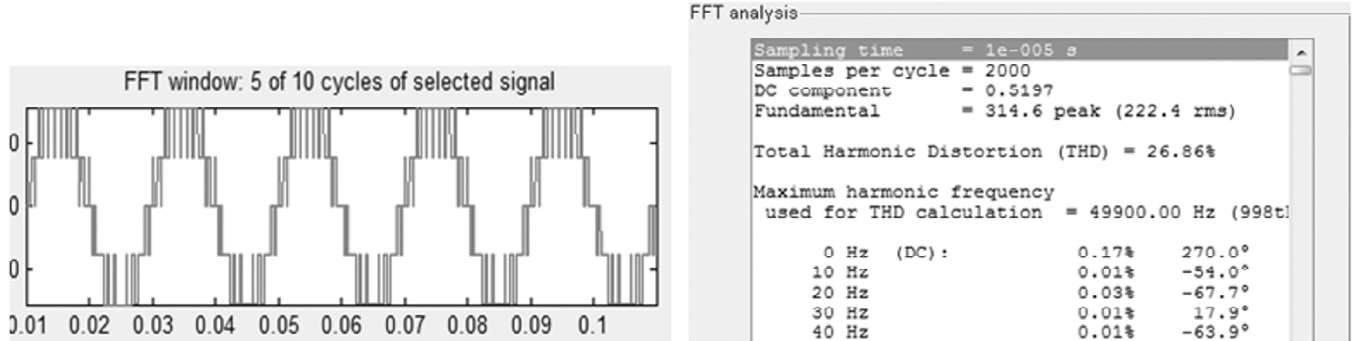## PD Voltage Wave
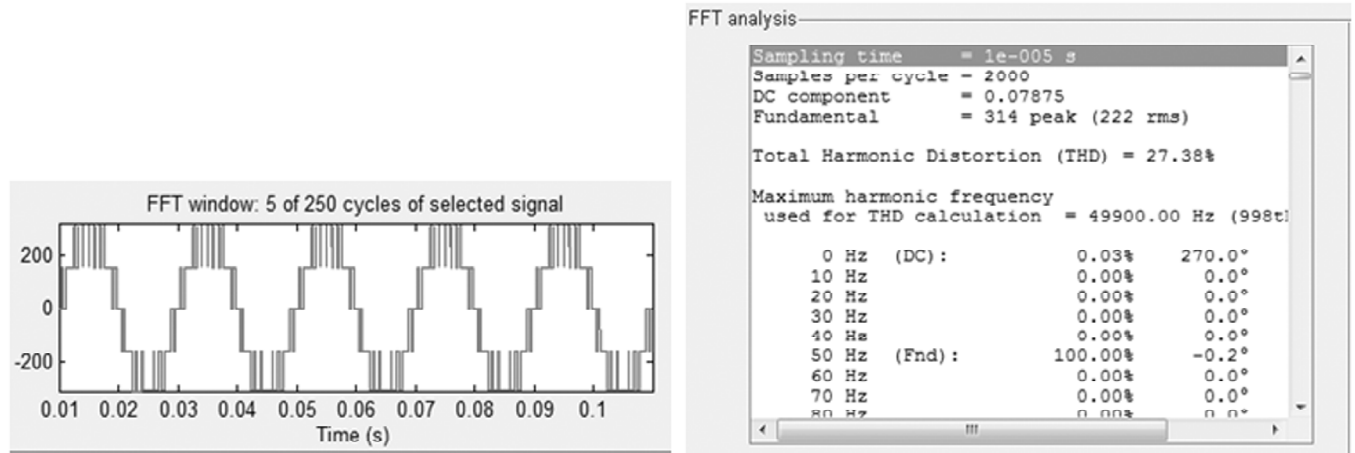

Figure 8:

POD Volatge Wave

Figure 9:

Seven Level Inverter Voltage THD at various switching patter
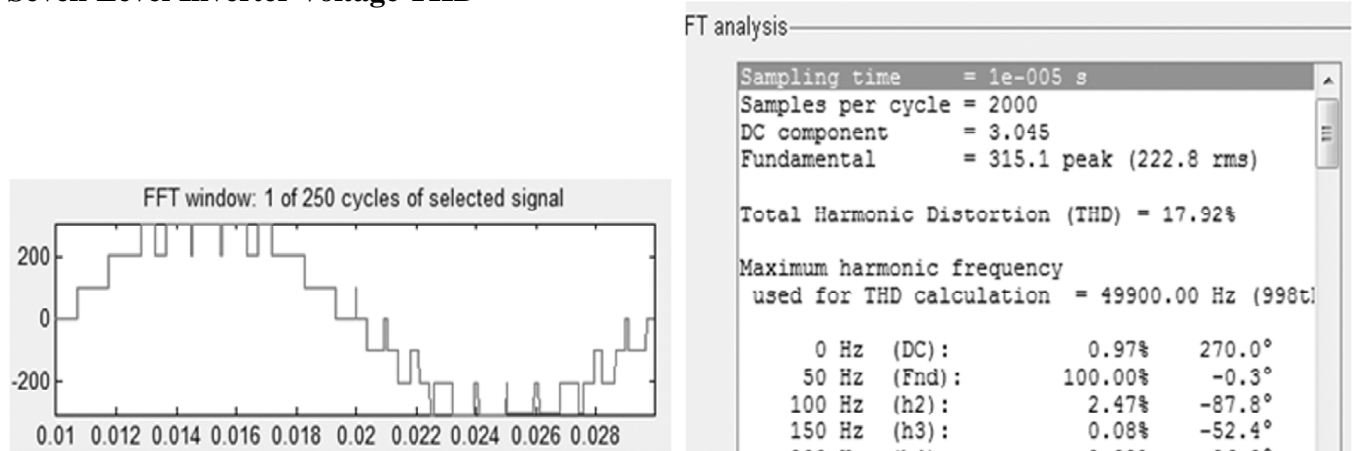## PD Voltage Wave
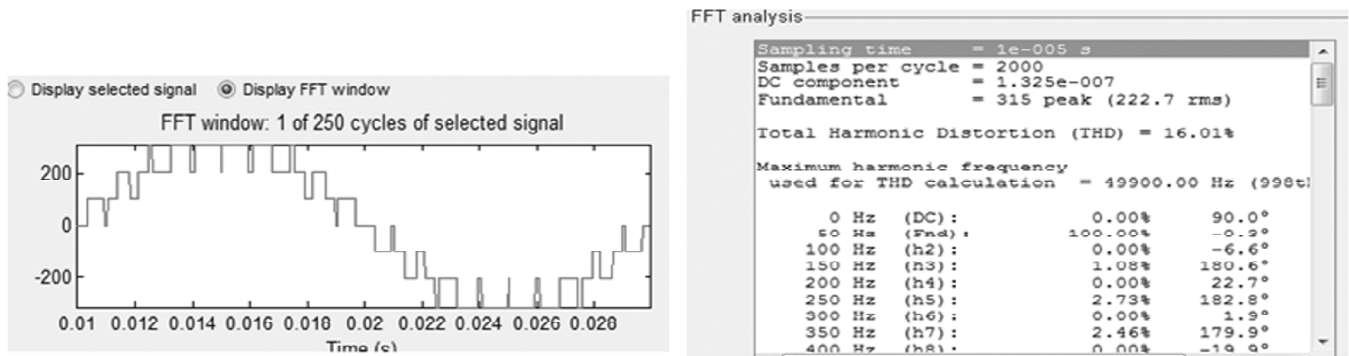## Seven Level Inverter Voltage THD

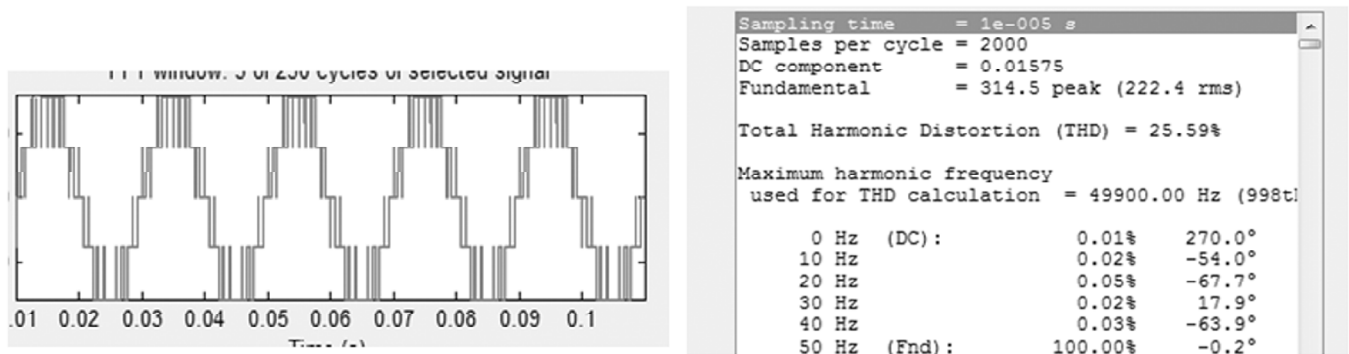**Figure 10:**

POD Voltage Wave

Figure 11:

APOD Wave

Figure 12:

APOD Wave
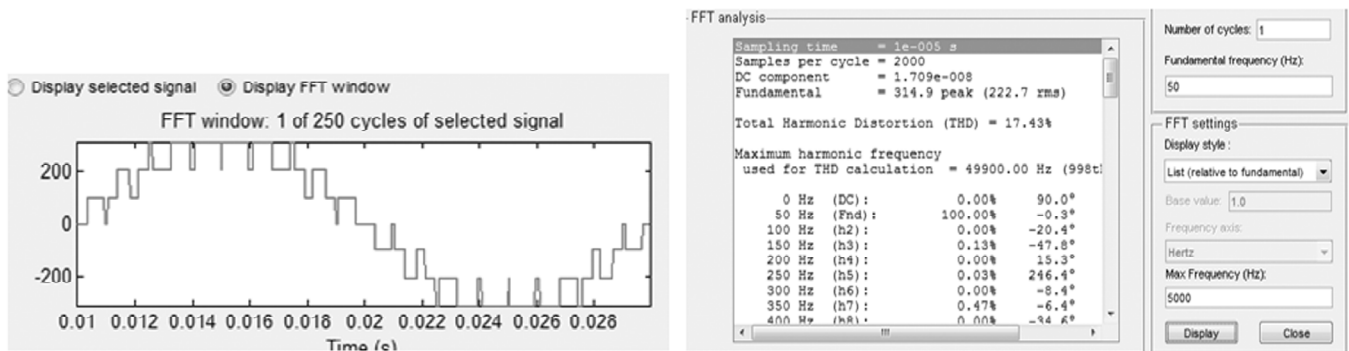
Figure 13:

Comparison of Third Harmonic Content

strategy	Five level	Seven level
PD	0.08%	0.08%
POD	0.59%	1.08%
APOD	0.03%	0.13%

7. FUTURE SCOPE

In Future we can implement this on hardware project and also perform this at different dc voltage source and by using single dc source. Power electronic has very vast area so we can implement any advance technique for Pwm wave generation like Space vector modulation

8. CONCLUSION

From the simulation result it has been clearly seen that by increasing the number of level from 5 to 7 the Total Harmonic Distortion is decreasing from 25.59% to 16.01%. Hence It can be concluded that the quality of power improved by using multi-level inverter.

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[3]	Dr M H.Rashid "Power Electronic circuit, device and application".

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