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Reduction of Area and Power of Shift Register Using Pulsed Latches

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ABSTRACT

The timing element and clock interconnection networks, such as flip flops and latches, which consume more power and area in VLSI world. This paper focuses on reduction of area and power of shift register using pulsed latches. The shift register using static differential sense amplification shared pulse latches, consist less number of transistors among all pulsed latches and compare with the power Pc style flip flop which consist smallest number of transistors among flip flops. Shift register fabricated using 180nm CMOS technology in virtuoso tool. The proposed shift register saves more power and area compared to the conventional shift register.

Index Terms: Power pc style flip flops, static differential sense amplification shared pulse latch, delayed pulse clock generator, CMOS technology.

I. INTRODUCTION

As we know that shift register which used a cascaded flip flops i.e. output of one flip flop is input of another flip flop. Considering of shift register's speed is less important compare to power consuming and required area because shift register which has not any circuit in between of two consecutive storage element. Recently shift register which replaced the flip flops by pulsed latches in many applications because pulsed latch which consume less area and power compare with flip flops such as digital filters[2], communication receivers [3] and image processing[4-5]. But problem is that we cannot be used precisely pulsed latches in shift register due to timing constrain. Here this paper proposed a shift register which consume less power and area, simulated in cadence design systems at 180 nm technology.

(A) Power PC style flip flop

Transistors comparison among the flip flops like The Power-PC-style style flip flop (PPCFF)[6], Strong-Arm flip-flop (SAFF)[6], Data mapping flip-flop (DMFF)[8], Conditional precharge sense-amplifier flip-flop (CPSAFF)[9], sense-amplifier flip-flop (SAFF), conditional capture flip-flops (CCFF)[10], adaptive coupling flip-flops (ACFF). Among all flip flops PPCFF which consumes less number of transistors which is 16 and number of transistors which is connected to clock is 8. Among all flip flops PPCFF consist maximum no. of clock connected transistors. Here shows schematic of PPCFF and simulation waveform. In Table I, it shows that the total number of transistor according to the storage elements (flip flops).

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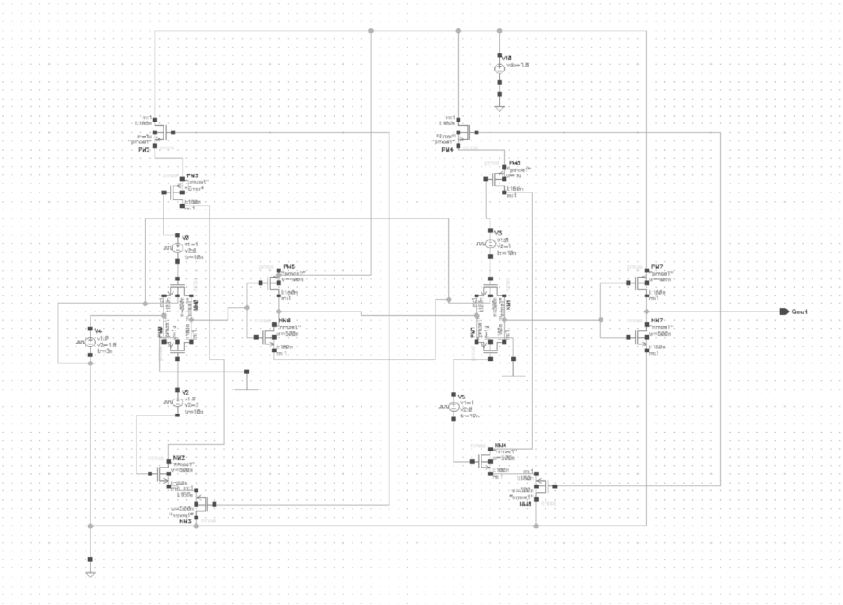
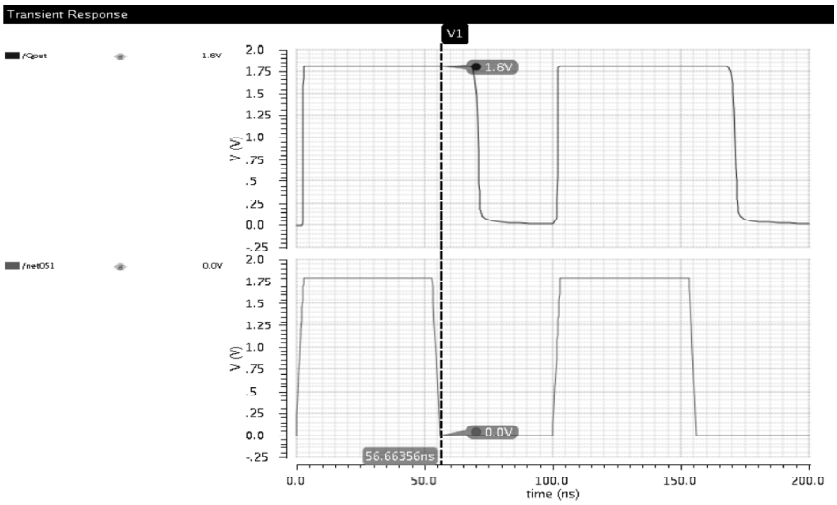
Table I
Transistors Comparision of Flip Flop

Flip flops	*No. of transistors*
data mapping flip-flop[8]	22
PPCFF[6]	16
Strong arm flip flop[6]	18
conditional precharge sense-amplifier flip-flop[9]	28
conditional capture flip-flop[10]	28



(a)

Fig. 1.(a) shows schematic design of PPCFF which is composed of two latches and act as a master slave flip flop. There are two transmission gate is used in this flip flop one is in master and another one is in slave part. At a time one part will be in transition mode and another one is in hold mode. Out of 16 transistors 8 transistors connected to clock. The PPCFF simulated at 1.8v in 180nm technology of cadence tool and the power consumption by PPCFF is in uW.Fig.1.(b) shows simulation waveform of PPCFF.



(b)

Figure 1: (a) Schematic design of the PPCFF.(b)Simulation waveform of the PPCFF.

By the using of PPCFF designed a 4-bit shift register and the power consumed by shift register is in uW.

(B) Pulsed latch

Pulsed latch which is much faster than flip flops and they required less no. of clock transistors than flip flops that's why it consume less power as well as area. Pulsed latch which is designed by the conventional cmos transparent latch which is driven through the narrow clock pulse driven through the clock pulse generator which is also said to be clock chopper. Pulse generator which used to weak inverter to produce Pulse, which is one-sixth of the nominal pulse width. The internal nodes of pulse generator which flows very high in short duration or momentarily but there is no requirement of keeper circuit because pulse duration is very short or less. Pulsed latch is one of the attractive solution to reduce the power and area compared to flip flops. In Table II shows some pulsed latches and used no. of transistors.

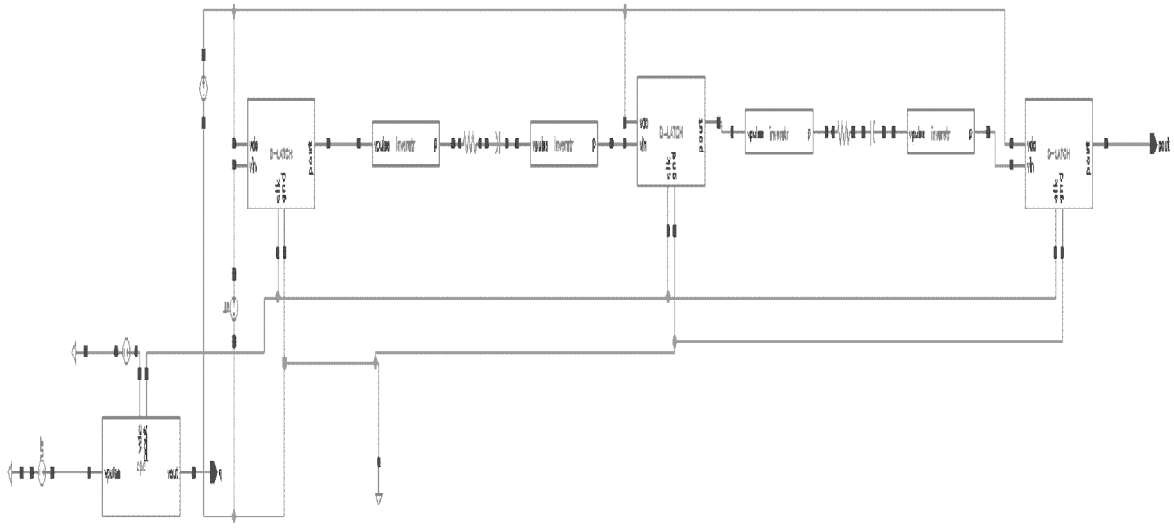
SSASPL stands for static differential sense amp shared pulse latch (7 transistors) and only transistor is attached to clock[6]. In transmission gate pulsed latch there are 10 transistors and 4 transistors connected to clock[7], hybrid latch flip flop required 14 transistors and 2 transistors required for clock[10], conditional push-pull pulsed latch required 26 transistors and 6 transistors required to connect with clock[7]. Among all of the pulsed latch SSASPL required less no. of transistors.

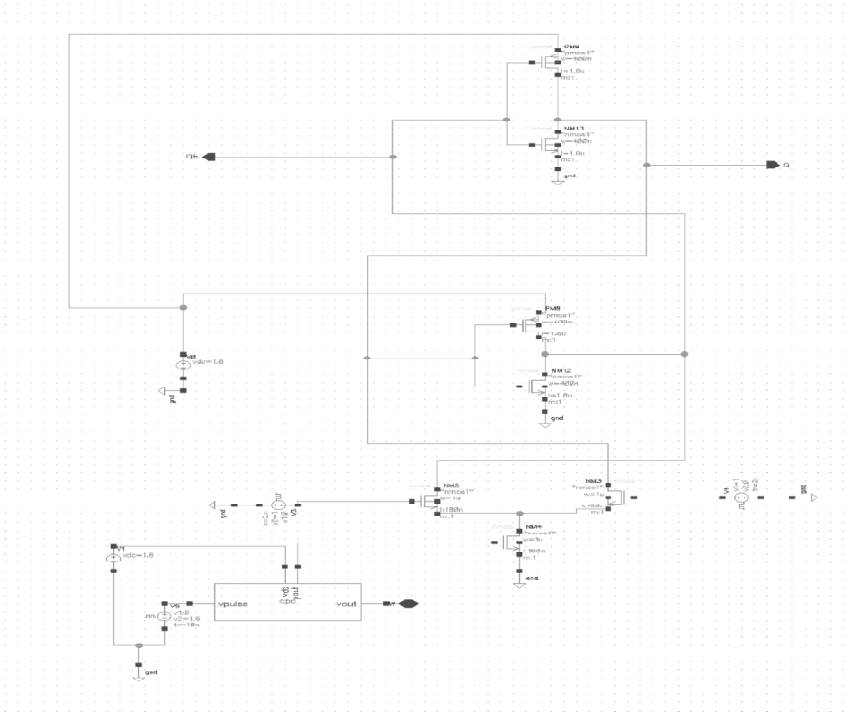
Table II
Transistors Comparision of Pulsed Latch

Pulsed latch	*No. of transistors*
SSASPL[6]	7
TGPL [7]	10
HLFF[10]	14
CP3L[7]	26

(C) Static differential sense amp shared pulse latch

SSASPL is the one of smallest pulsed latch among all pulsed latches [7]. Conventional SSASPL used 9 transistors but here one inverter is removed. Only one transistor is driven through the pulsed clock that's why it consume lowest power. There are two inverter which is cross coupled i.e. 4 transistors which holds the data and three nmos transistors which updates the data. There are two differential input and two differential outputs shows in Fig.2.(a).When clock pulse is high it updates the data shows in Fig2.(b).The output nodes will be pull down to ground according to input. SSASPL is implemented in 180nm cadence tool.





(a)

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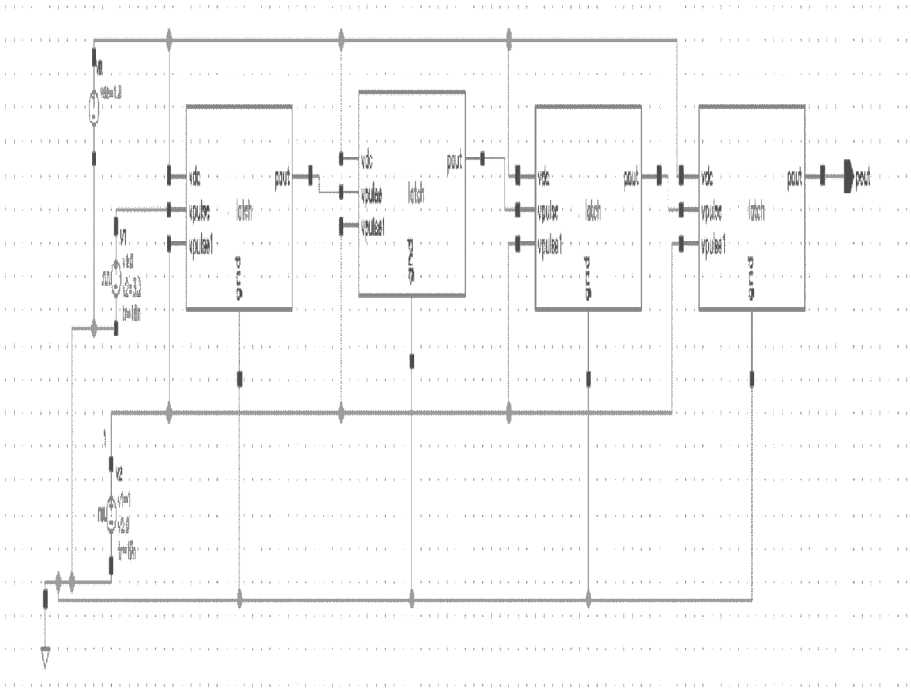
Figure 2: (a)Schematic design of SSASPL.(b)Simulation waveform.

II. ARCHITECTURE

The pulsed latches directly cannot be use due to timing inhibit as shows in Fig.3.(a).



(a)

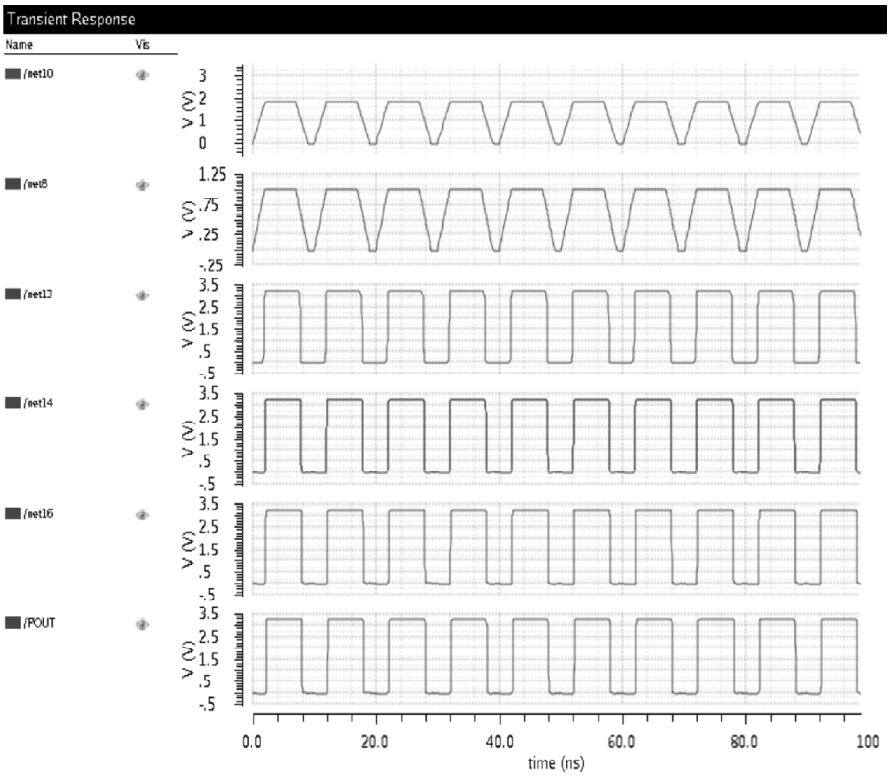


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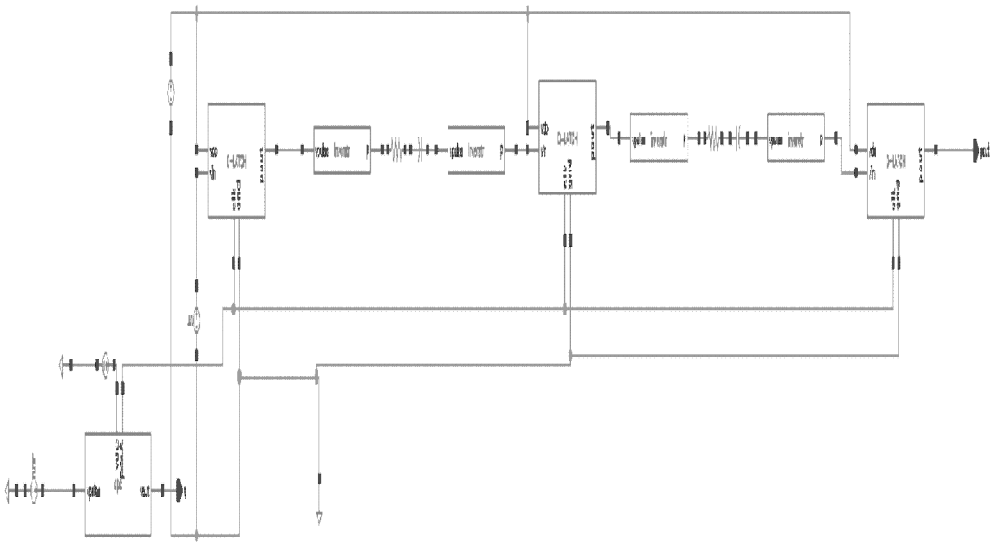
Figure 3: (a)Schematic design of shift register.(b) Simulation waveform

In Fig.3.(a) shift register there are 4 latches, the input of first latch is changed but the second is not corrected well as shows in Fig.3.(b).

This problem occurs due to timing inhibit, output of first storage element due to input signal is changed well but second one is constant due to input signal change during the clock pulsed width. To solve this

problem, proposed a new architecture where add a delay circuit in between of two consecutive latches and getting delayed output i.e. after clock pulse as shows in Fig.4.(a).Output of one latch is the input of other latch which changes correctly shows in Fig.4.(b).There is no any timing problem each latch gets constant input signal. However the using of delay circuit may be cause of the more power consumption and large area. Here in Fig.4.(a).shift register which is designed by the using of pulsed latch. The cascaded pulsed latch which is operated by the pulsed delay generator which reduced the no. of delayed clock pulse show in Fig.5.(a).



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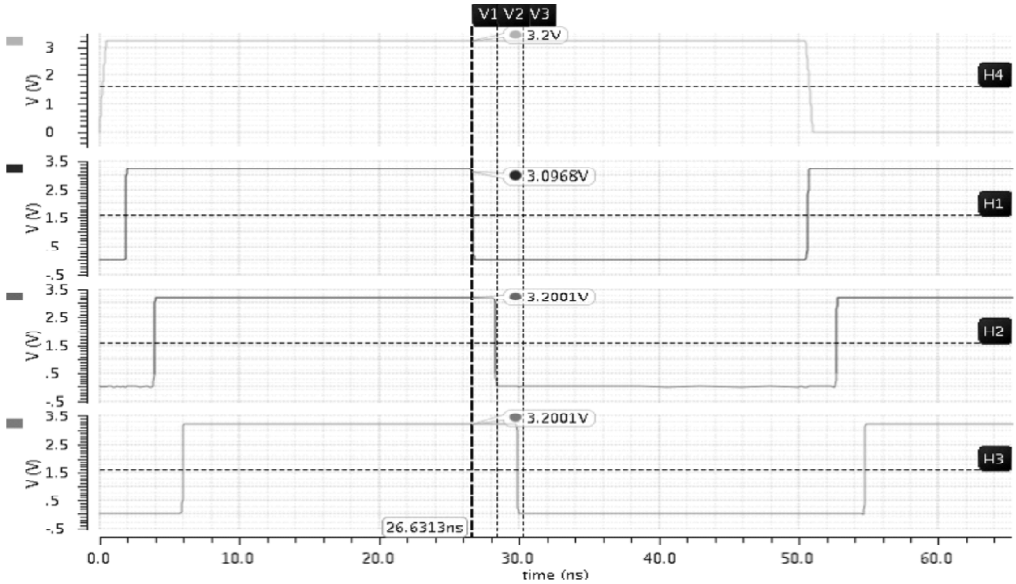
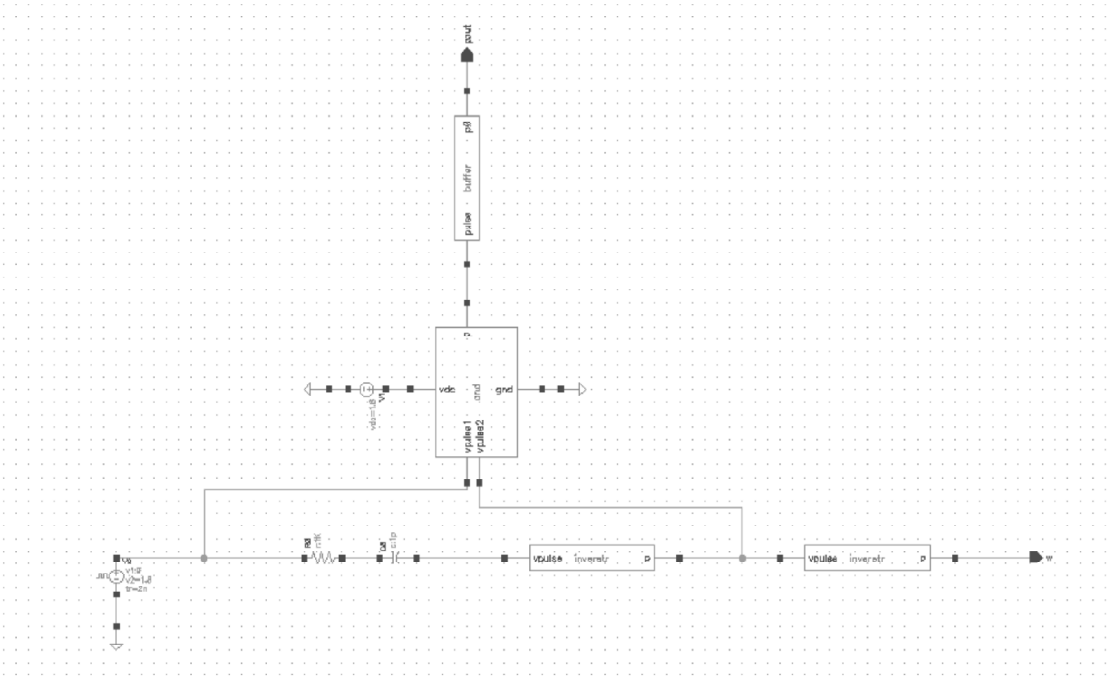


(b)

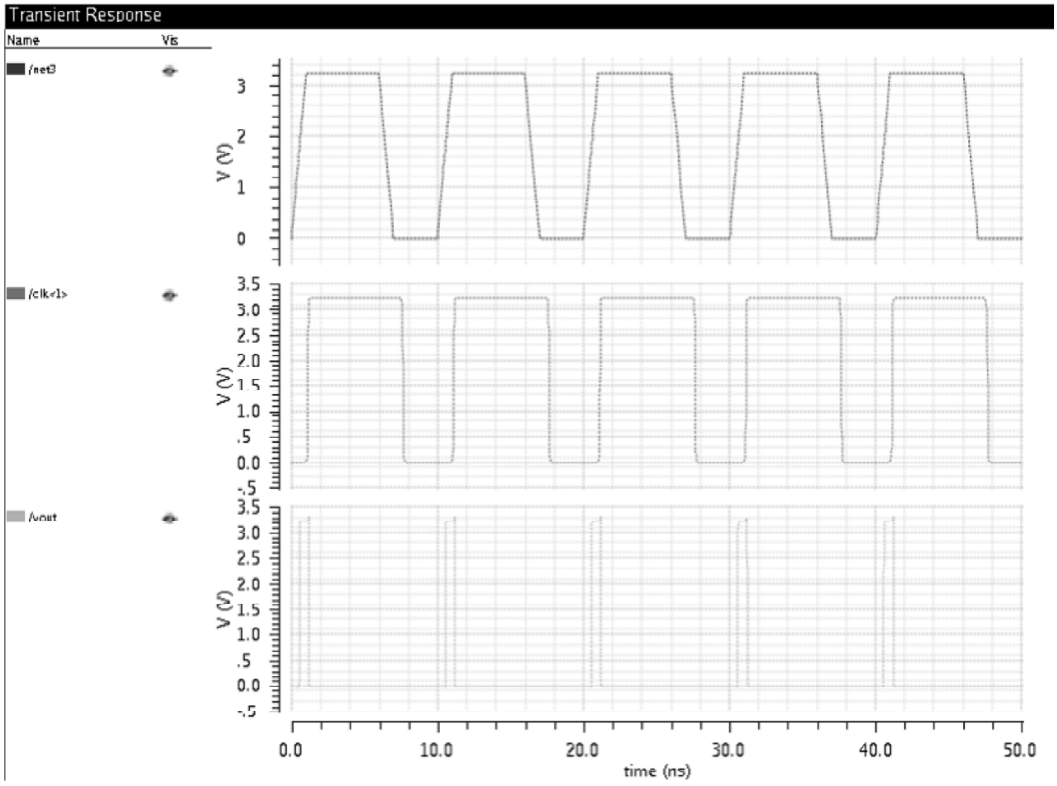
Figure 4: (a)Shift register with delayed circuit and pulse clock. (b) Simulation waveform

Delayed pulse clock generator consist of delay circuit (rc delay), AND gate and single buffer the reason behind the using of AND gate is it allows the pass the data through channel, measured the frequency and gating the pulse[1]. Buffer which helps to solve the clock skew problem because in a long shift register at the ending of clock pulse would be degraded, to overcome this used a clock buffer. Simulated waveform shows

in Fig.5.(b).In which delayed clock pulse is generated by clock pulsed generator which gives the output in between of start and stop time. Start time act as a input signal and stop time and stop time as a output .In between of this specified time delay i.e. pulsed delayed output.



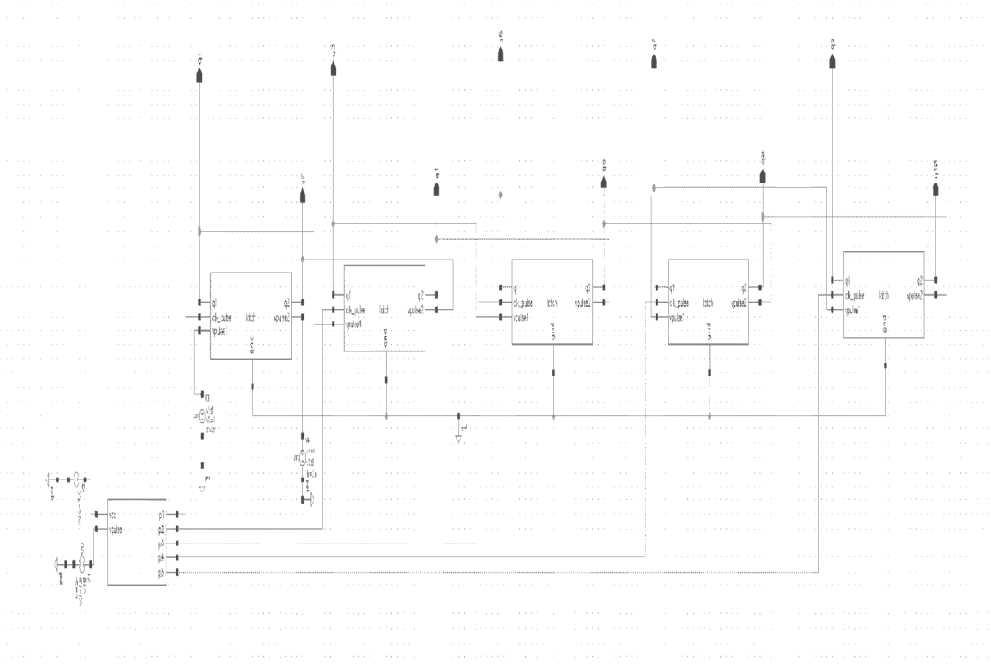
(a)



(b)

Figure 5: (a) pulse delayed generator. (b) Simulation waveform

The 4-bit shift register is designed by the static differential sense amplification shared pulse latch which is succesefully designed in 180nm technology of cadence virtuoso tool at 1.8v. Gating pulse which is given by the clock pulse delayed generator to each of the latch including temporary latch also. By the using of pulse delayed generator we fixed the timing inhibit and strongly or well designed. The shift register which consist low power as well as area,by the designing of layout determine the efficient area. So designed shift register shows in Fig.6(a) and successfully simulated waveform shows in Fig.6(b).



(a)

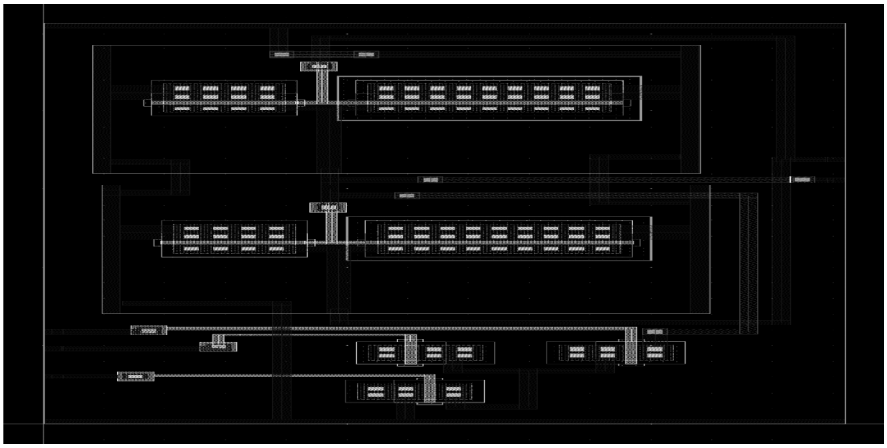
(b)

Figure 6: (a)Schematic design of shift register.(b)Simulation waveform

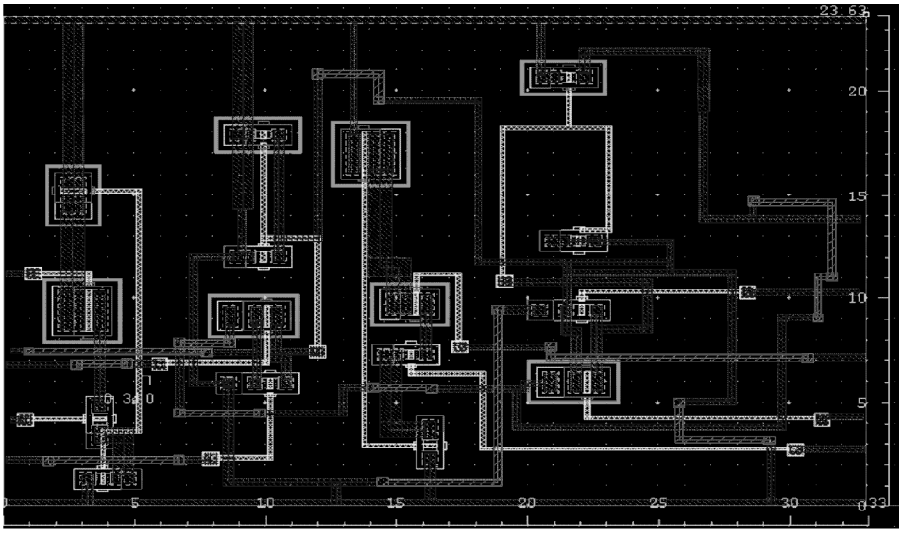
Table III
Power Comparision

SSASPL	736.8nw
PPCFF	5.853uw
Shift register with PPCFF	21.23uw
Shift register with SSASPL	8.619uw

Productive power shows in TableIII. Area of PPCFF and SSASPL is determined by the designing of layout. The efficient area which is shown in Table IV.



(a)



(b)

Figure 7: layout design of (a) static differential sense amplification shared pulse latch. (b) Power pc style flip flop.

Table IV
Area Comparision

PPCFF	35.09um^2
SSASPL	15.14um^2
Shift register with SSASPL	78.2um^2
Shift register with PPCFF	146.19um^2

III. CONCLUSION

In this work analyzed the power and area of power pc style flip flop and static differential sense amp shared pulse latch with sufficient results and reduce the power and area. Furthermore designed and simulated using of the static differential sense amp shared pulse latch in shift register obtain acceptable results of designing the shift register using pulsed latch. Furthermore the shift register power and area reduced by the using of pulsed latch. The design was simulated in 180nm CMOS technology in virtuoso tool.

ACKNOWLEDGMENT

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REFERENCES

[1] Byung-Do Yang Low-Power and Area-Efficient Shift Register Using Pulsed Latches IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMSI : REGULAR PAPERS, VOL. 62, NO. 6, JUNE 2015.

[2] P. Reyes, P. Reviriego, J. A. Maestro, and O. Ruano, "New protection techniques against SEUs for moving average filters in a radiation environment," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 4, pp. 957–964, Aug. 2007.

[3] M. Hatamian *et al.*, "Design considerations for gigabit ethernet 1000 base-T twisted pair transceivers," *Proc. IEEE Custom Integr. Circuits Conf.*, pp. 335–342, 1998.

[4] H. Yamasaki and T. Shibata, "A real-time image-feature-extraction and vector-generation vlsi employing arrayed-shift-register architecture," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 2046–2053, Sep. 2007.

[5] H.-S. Kim, J.-H. Yang, S.-H. Park, S.-T. Ryu, and G.-H. Cho, "A 10-bit column-driver IC with parasitic-insensitive iterative charge-sharing based capacitor-string interpolation for mobile active-matrix LCDs," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 766–782, Mar. 2014.

[6] S. Heo, R. Krashinsky, and K. Asanovic, "Activity-sensitive flip-flop and latch selection for reduced energy," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 15, no. 9, pp. 1060–1064, Sep. 2007.

[7] E. Consoli, M. Alioto, G. Palumbo, and J. Rabaey, "Conditional push-pull pulsed latch with 726 fJops energy delay product in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2012, pp. 482–483.

[8] S. Nomura *et al.*, "A 9.7 mW AAC-decoding, 620 mW H.264 720p 60fps decoding, 8-core media processor with embedded forwardbody- biasing and power-gating circuit in 65 nm CMOS technology," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2008, pp. 262–264.

[9] Y. Ueda *et al.*, "6.33 mW MPEG audio decoding on a multimedia processor," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2006, pp. 1636–1637. [15] B.-S. Kong, S.-S. Kim, and Y.-H. Jun, "Conditional-capture flip flop for statistical power reduction," *IEEE J. Solid-State Circuits*, vol. 36,pp. 1263–1271, Aug. 2001.

[10] B.-S. Kong, S.-S. Kim, and Y.-H. Jun, "Conditional-capture flip-flop for statistical power reduction," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1263–1271, Aug. 2001.