**IJCTA,** 9(39), 2016, pp. 173-186


# SMC Based Synchronization and Anti-Synchronization of Chaotic Systems for Secure Communication and Analog Circuit Realization

**P. P. Singh* J. P. Singh** and B. K. Roy****

***Abstract :*** In this paper, synchronization and anti-synchronization of Bhalekar-Gejji chaotic system is proposed with application to secure communication. Further its analog circuit design and simulation is carried out using analog components. Proposed synchronization and anti-synchronization with application to secure communication is achieved using robust SMC. For communication, the information signal is masked with any single state. Lyapunov stability theory is used and required condition is derived to ensure the stability of error dynamics. Controller and stable switching surface is designed to insure the system trajectory with in the sliding manifold. Further analog circuit simulation is achieved to interface system with proposed scheme into the real world. MATLAB and MULTISIM platforms are used for simulation and circuit design. Simulation and realization results suggest that proposed scheme for synchronization and anti-synchronization of Bhalekar-Gejji (BG) chaotic system with application to secure communication is working satisfactorily.

***Keywords :*** Synchronization; Anti-synchronization; Chaotic System Synchronization; Sliding Mode Control; Lyapunov Stability Theory; Multisim Circuit Design.

## 1. INTRODUCTION

Chaotic systems are being potentially used for secure communication and signal processing because of their potential mechanism for signal design and generation. Chaotic signal can be used in various ways for masking information bearing waveforms, because they are typically noise like and broadband, therefore difficult to predict [1]. The other important property of chaotic system is aperiodic long time behavior arises from deterministic dynamical system which is sensitivity to initial condition [2]. Synchronization means if two systems have similar behavior at same time or they share common time. It is possible to make two chaotic system get synchronized, because of above property. This important property leads to some interesting and common applications in the field of secure communication [3, 4]. Synchronization of two identical chaotic systems with different initial condition was illustrated by Pecora & Carroll in 1990 [5].

During last two decades, chaos synchronization has attracted a great attention from various fields [2]. There are two methods for synchronization of chaotic system as drive-response scheme and coupling scheme. Drive-response also called master-slave system which is widely used. Synchronization is achieved when error between the states of the master and slave systems tends to zero. Various control schemes have been developed for synchronization of chaotic system in the last two decades such as active control method [6, 7], adaptive control method [8], backstepping control method [9], sampled data feedback method [10], time delay feedback method [11], sliding mode control method [12], passive control [13],

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optimal control [14], fuzzy control [15], PID control [16] etc. So many techniques are also available related to synchronization known as lag synchronization [17], phase synchronization [18], projective synchronization [19], generalized projective [20], exponential synchronization [21], anti-synchronization [7, 22] and hybrid synchronization [23, 24]. Meanwhile, another important phenomenon has devised is anti-synchronization between master-slave systems with many chaotic systems. Anti-synchronization is achieved when sum of states of two chaotic systems (master-slave) will asymptotically converge to zero, having equal amplitude and opposite phase between the state of master-slave systems [25].

In this paper, SMC is used for synchronization and anti-synchronization of two Bhalekar-Gejji (BG) [26, 27] chaotic systems. SMC is used because of its inherent advantages of robust realization, fast response as well as its insensitivity to parameter uncertainties and disturbances [28]. Synchronization property used here to show secure communication between the master and slave systems. For illustration purpose the message signal is transmitted at transmitter end in the form of sin wave and same message is recovered back at the receiver end.

Rest of paper is organized as follows. In Section 2, problem statement for synchronization of chaotic system is discussed. In Section 3, synchronization of Bhalekar-Gejji (BG) chaotic system using SMC is presented. In Section 4, problem formulation for anti-synchronization is discussed. In Section 5, anti-synchronization of BG chaotic system using SMC is discussed. MULTISIM circuit design and realization for synchronization, anti-synchronization for proposed scheme based on BG chaotic system is achieved in Section 6. In Section 7, secure communication scheme based upon on synchronization is discussed. In Section 8, description of switching surface and controller for application to secure communication using Bhalekar-Gejji chaotic system is given and analog circuit is designed. In Section 9, simulation and circuit design results are shown for validation and verification of proposed scheme. Finally, Section 10 conclusions and future scope is addressed.

## 2. PROBLEM FORMULATION FOR SYNCHRONIZATION

In this section, synchronization of Bhalekar-Gejji chaotic systems based on sliding mode control is discussed. In 2011, S. B. Bhalekar and V. D. Gejji proposed the Bhalekar-Gejji (BG) chaotic dynamical system as:

$$\begin{cases} \dot{x}_1 = wx_1 - x_2^2 \\ \dot{x}_2 = \mu(x_3 - x_2) \\ \dot{x}_3 = \alpha x_2 - \beta x_3 + x_1 x_2 \end{cases} \tag{1}$$

where $x_1, x_2, x_3$ are the states. The system exhibit chaotic behavior for $w = -2.667$, $\mu = 10$, $\alpha = 27.3$, $\beta = 1$. The master dynamics is defined by (1). The slave system along with controller is described as:

$$\begin{cases} \dot{y}_1 = wy_1 - y_2^2 + u_1 \\ \dot{y}_2 = \mu(y_3 - y_2) \\ \dot{y}_3 = \alpha y_2 - \beta y_3 + y_1 y_2 + u_2 \end{cases} \tag{2}$$

where $y_1, y_2, y_3$ are states of slave system (2) and $u_1$, $u_2$ are the control inputs. Synchronization between the master and slave systems can be achieved for any initial conditions, if

$$\lim_{t \to \infty} \|e_i(t)\| \text{ for } i = 1, 2, 3 \tag{3}$$

The error dynamics is obtained as follows:

$$\begin{cases} \dot{e}_1 = we_1 - y_2^2 + x_3^2 + u_1 \\ \dot{e}_2 = -\mu\, e_2 + \mu\, e_3 \\ \dot{e}_3 = ae_2 - be_3 + y_1 y_2 - x_1 x_2 + u_2 \end{cases} \tag{4}$$

Our aim is to design a sliding mode controller such that resulting error dynamics satisfies condition (3) to synchronize the master and slave chaotic systems defined in (1) and (2). Based on the SMC theory, synchronization of BG chaotic system is discussed in the next section.

## 3. SYNCHRONIZATION OF BG CHAOTIC SYSTEM USING SMC

The SMC technique is used to achieve synchronization for pair of chaotic system (1) and (2), involves two major steps. First, selects appropriate switching surfaces which guaranteed stability of equivalent dynamics in sliding mode such that synchronization error (22) converge to zero. Second, to establish the control law which guaranteed the existence of sliding mode $s(t) = 0$, is defined as provided $k_1, k_2 > 0$

$$\begin{cases} s_1 = e_1 + \int_0^t k_1 e_1 \, d\tau \\ s_2 = e_3 + \int_0^t (\mu e_2 + k_2 e_3) \, d\tau \end{cases} \tag{5}$$

System trajectory operates in sliding mode (Itkis, 1976), when it satisfies: $\dot{s}_1 = 0$ and $\dot{s}_2 = 0$. So, (5) is written as:

$$\begin{cases} \dot{s}_1 = \dot{e}_1 + k_1 e_1 \\ \dot{s}_2 = \dot{e}_3 + \mu e_2 + k_2 e_3 \end{cases} \tag{6}$$

Resulting in the form of (7) as:

$$\begin{cases} \dot{e}_1 = -k_1 e_1 \\ \dot{e}_3 = -\mu e_2 - k_2 e_3 \end{cases} \tag{7}$$

Using (4) and (7), the equivalent sliding mode error dynamics is written as:

$$\begin{cases} \dot{e}_1 = -k_1 e_1 \\ \dot{e}_2 = -\mu e_2 + \mu e_3 \\ \dot{e}_3 = -\mu e_3 - k_2 e_3 \end{cases} \tag{8}$$

To ensure the occurrence of sliding motion, the controller is proposed in (9).

$$\begin{cases} u_1 = we_1 - x_2^2 + y_2^2 - k_1 e_1 - \psi\,(\mathrm{sign}(s_1)) \\ u_2 = -ae_2 + be_3 - y_1 y_2 + x_1 x_2 - \mu e_2 - k_2 e_3 - \psi\,(\mathrm{sign}(s_2)) \end{cases} \tag{9}$$

where $\psi > 0$ has to be selected suitably.

**Theorem :** The control inputs $u_1$, $u_2$ of (9) causes to converge the state trajectories of the systems (1) and (2) onto the sliding surface $s(t) = 0$ and holds $\lim(t_{\to\infty}) \|e_i(t)\| = 0$.

**Proof :** Let a Lyapunov function be defined as

$$\mathrm{V}(s) \;=\; \frac{1}{2}(s_2^2 + s_2^2) \tag{10}$$

Having the first order continuous derivative of V($s$) and using (4), we have

$$\dot{\mathrm{V}}(s) \;=\; s_1[we_1 - y_2^2 + x_2^2 + u_1 + k_1 e_1] + s_2[ae_2 - be_3 + y_1 y_2 - x_1 x_2 + u_2 + \mu e_2 + k_2 e_3] \tag{11}$$

By using the control law (9) we have

$$\dot{\mathrm{V}}(s) \;=\; -\psi|s_1| - \psi|s_2| \le 0 \tag{12}$$

For $s(t) = 0$ and $\psi > 0$ according to suitable choice, following holds

$$\dot{\mathrm{V}}(s) \;=\; s_1\dot{s}_1 + s_2\dot{s}_2 < 0$$

Thus, according to Lyapunov stability theory $s(t)$ always converges to switching surface $s(t) = 0$. Hence, error dynamics in sliding manifold is asymptotically stable and the error dynamics converges to zero.

## 4. PROBLEM FORMULATION FOR ANTI-SYNCHRONIZATION

The master dynamics is defined in (1). The slave system is described in (2). The anti-synchronization error between the master and slave systems is obtained as follows:

$$\begin{cases} \dot{e}_1 = we_1 - y_2^2 - x_2^2 + u_1 \\ \dot{e}_2 = -\mu e_2 + \mu e_3 \\ \dot{e}_3 = ae_1 - be_3 + y_1 y_2 + x_1 x_2 + u_2 \end{cases} \tag{13}$$

To synchronize the master-slave chaotic systems in (1) and (2), respectively, our aim is to design a SMC such that the resulting error vector satisfies condition (3).

## 5. ANTI-SYNCHRONIZATION OF BG CHAOTIC SYSTEM USING SMC

In this section, we discuss the anti-synchronization of two identical Bhalekar-Gejji chaotic systems based on sliding mode control. The appropriate switching surface is defined as in (34) provided $k_1$, $k_2 > 0$.

$$\begin{cases} s_1 = e_1 + \int_0^t k_1 e_1 \, d\tau \\ s_2 = e_3 + \int_0^t (k_2 e_3 + \mu e_2) d\tau \end{cases} \tag{14}$$

where $e_1$, $e_2$ and $e3$ are the anti-synchronization errors. To ensure the occurrence of the sliding motion, the controller is proposed in (15).

$$\begin{cases} u_1 = we_1 + x_2^2 + y_2^2 - k_1 e_1 - \psi(\text{sign}(s_1)) \\ u_2 = -ae_2 + be_3 - y_1 y_2 - x_1 x_2 - \mu e_2 - k_2 e_3 - \psi(\text{sign}(s_2)) \end{cases} \tag{15}$$

where $\psi > 0$ has to be selected suitably. The control inputs $u_1$, $u_2$ of (15) causes to converge the system trajectory of (1) and (2) onto the sliding surface $s(t) = 0$. Let us consider a Lyapunov function and having first order continuous differentiation and using the control law of (15) results a negative definite function $\dot{\mathrm{V}}(s)$ as:

$$\dot{\mathrm{V}}(s) \;=\; -\psi|s_1| - \psi|s_2| \;\leq 0 \tag{16}$$

For $s(t) = 0$ and a suitable choice of $\psi > 0$ holds $\dot{\mathrm{V}}(s) = s_1\dot{s}_1 + s_2\dot{s}_2 < 0$.

Thus, according to the Lyapunov stability theory $s(t)$ always converges to switching surface $s(t) = 0$. Hence, the error dynamics in sliding manifold is asymptotically stable according to (16), and error dynamics converges to zero. Based on synchronization and anti-synchronization scheme developed in the previous sections, analog circuit design using MULTISIM is given in the next section.

## 6. MULTISIM CIRCUIT DESIGN AND REALIZATION

In this section, the circuit simulation of BG chaotic system its synchronization and anti-synchronization scheme is shown using NI Multisim 11.0.

### 6.1. Circuit simulation for Bhalekar-Gejji chaotic system

Here, BG chaotic system (1) is simulated using analog components resistance, capacitance and Op-amp of different values using MULTISIM is shown in the Fig. 1. Phase plane of BG chaotic system is shown in MULTISIM Oscilloscope in the Fig. 2.

### 6.2. Circuit simulation for synchronization of Bhalekar-Gejji chaotic system

In this subsection, synchronization error dynamics, sliding surface, control law describes in 4), (5) and (9), respectively, are simulated using analog components resistance, capacitance, Op-amp of different values. The dynamics of (9) and (5) in terms of analog circuit design are given in (17) and (18), respectively. Circuit simulation for synchronization scheme between the master and slave system is shown in the Fig. 3.

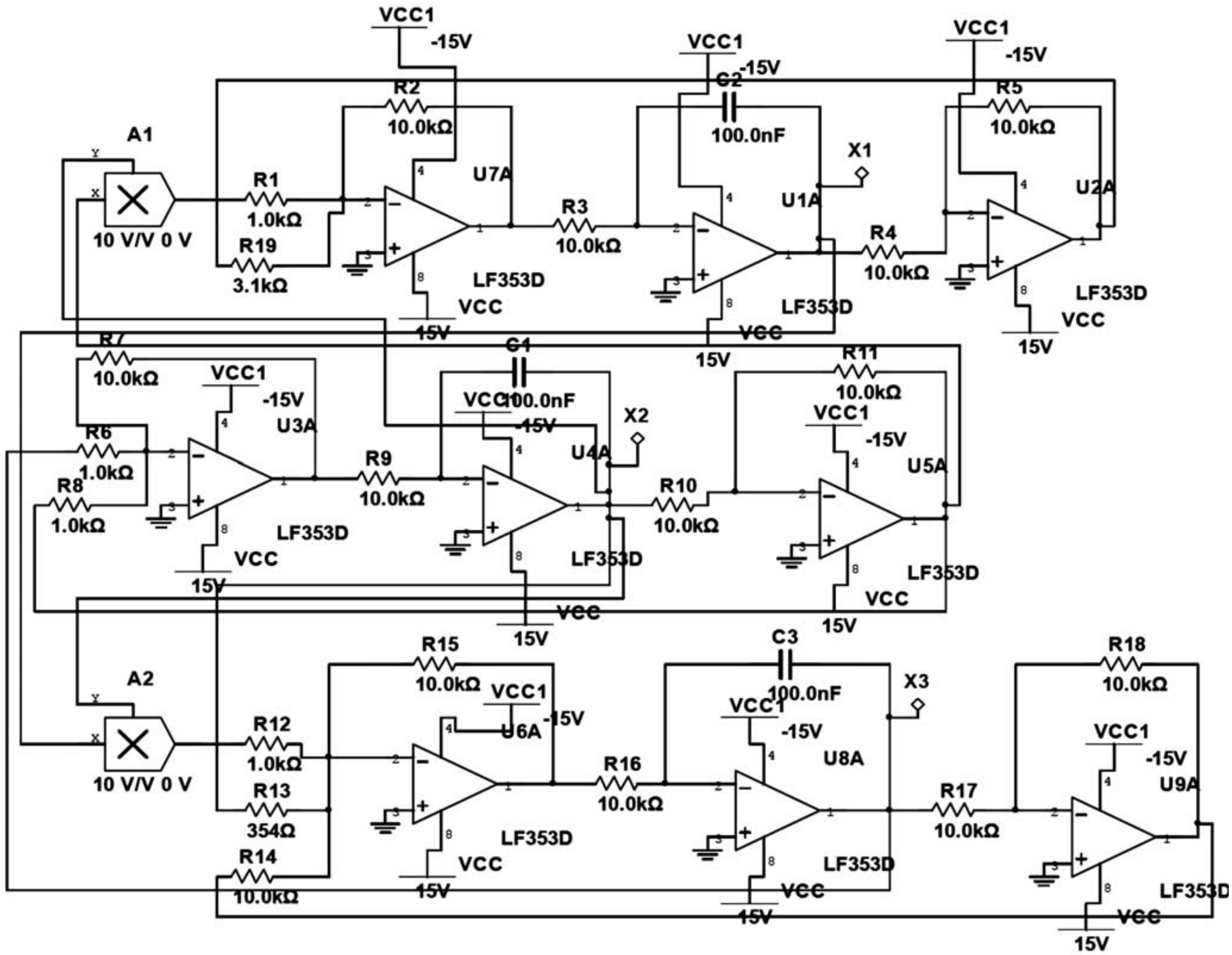



**Figure 1: Circuit simulation of Bhalekar-Gejji (BG) chaotic system**

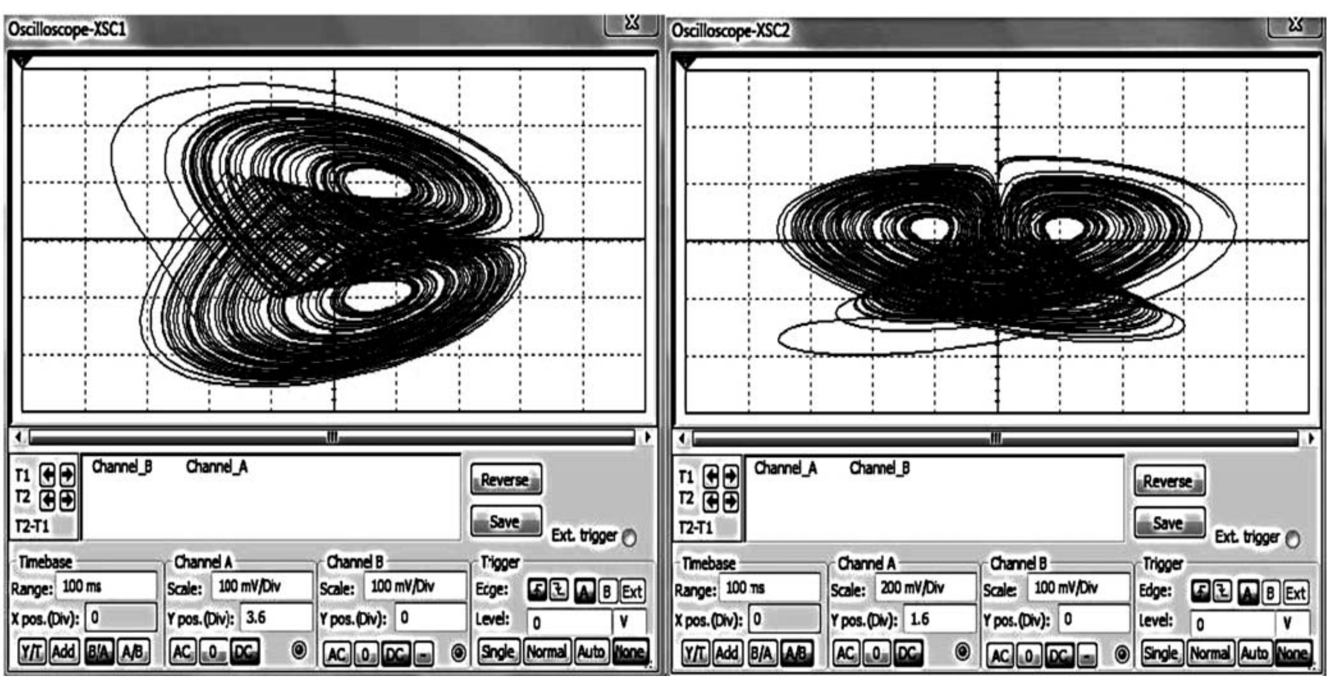



**Figure 2: Phase plane of Bhalekar-Gejji chaotic system with respect to $x_1$, $x_2$ plane in Oscilloscope-XSC1 and with respect to $x_1$,$x_3$ plane in Oscilloscope-XSC2**

$$\begin{cases} u_1 = -\left(\frac{R_{21}}{R_{59}}\right)y_1 - \left(\frac{R_{21}}{R_{60}}\right)x_1 + \left(\frac{R_{21}}{R_{61}}\right)\frac{y_2^2}{10} - \left(\frac{R_{21}}{R_{62}}\right)\frac{x_2^2}{10} - \left(\frac{R_{21}}{R_{81}}\right)s_1 - \left(\frac{R_{21}}{R_{84}}\right)e_1 \\ u_2 = -\left(\frac{R_{34}}{R_{64}}\right)y_2 + \left(\frac{R_{34}}{R_{65}}\right)y_3 + \left(\frac{R_{34}}{R_{31}}\right)\frac{y_1y_2}{10} + \left(\frac{R_{34}}{R_{69}}\right)\frac{x_1x_2}{10} + \left(\frac{R_{34}}{R_{69}}\right)x_2 - \left(\frac{R_{34}}{R_{68}}\right)x_3 \\ \qquad - \left(\frac{R_{34}}{R_{72}}\right)e_2 - \left(\frac{R_{34}}{R_{75}}\right)e_3 - \left(\frac{R_{34}}{R_{78}}\right)s_2 \end{cases} \tag{17}$$

where

$$\begin{cases} s_1 = \left(\frac{1}{R_{46}c_8}\right)\left[\left(\frac{R_{44}}{R_{43}}\right)\dot{e}_1 - \left(\frac{R_{44}}{R_{43}}\right)e_1\right] \\ s_2 = \left(\frac{1}{R_{54}c_{10}}\right)\left[\left(\frac{R_{52}}{R_{51}}\right)\dot{e}_3 + \left(\frac{R_{52}}{R_{53}}\right)e_3 + \left(\frac{R_{52}}{R_{58}}\right)e_2\right] \end{cases} \tag{18}$$

### 6.3. Circuit simulation for anti-synchronization of Bhalekar-Gejji chaotic system

Here, anti-synchronization error dynamics, sliding surface, control law describes in (13), (14) and (15), respectively, are simulated using analog components resistance, capacitance, Op-amp of different values. Circuit simulation for anti-synchronization scheme between the master and slave system is achieved in the similar fashion and not shown here to avoid repetition. The dynamics of (15) and (14) in terms of analog circuit design are given in (19) and (20), respectively.

$$\begin{cases} u_1 = \left(\frac{R_{21}}{R_{59}}\right)y_1 + \left(\frac{R_{21}}{R_{60}}\right)x_1 + \left(\frac{R_{21}}{R_{61}}\right)\frac{y_2^2}{10} + \left(\frac{R_{21}}{R_{62}}\right)\frac{x_2^2}{10} - \left(\frac{R_{21}}{R_{81}}\right)s_1 - \left(\frac{R_{21}}{R_{84}}\right)e_1 \\ u_2 = \left(\frac{R_{34}}{R_{64}}\right)y_2 + \left(\frac{R_{34}}{R_{65}}\right)y_3 - \left(\frac{R_{34}}{R_{31}}\right)\frac{y_1y_2}{10} - \left(\frac{R_{34}}{R_{69}}\right)\frac{x_1x_2}{10} - \left(\frac{R_{34}}{R_{69}}\right)x_2 + \left(\frac{R_{34}}{R_{68}}\right)x_3 \\ \qquad - \left(\frac{R_{34}}{R_{72}}\right)e_2 - \left(\frac{R_{34}}{R_{75}}\right)e_3 - \left(\frac{R_{34}}{R_{78}}\right)s_2 \end{cases} \tag{19}$$

where

$$\begin{cases} s_1 = \left(\frac{1}{R_{64}c_8}\right)\left[\left(\frac{R_{44}}{R_{43}}\right)\dot{e}_1 - \left(\frac{R_{44}}{R_{45}}\right)e_1\right] \\ s_2 = \left(\frac{1}{R_{54}c_{10}}\right)\left[\left(\frac{R_{52}}{R_{51}}\right)\dot{e}_3 + \left(\frac{R_{52}}{R_{53}}\right)e_3 + \left(\frac{R_{52}}{R_{58}}\right)e_2\right] \end{cases} \tag{20}$$

## 7. APPLICATION TO SECURE COMMUNICATION

A potential approach of synchronization of chaotic system for communication is based on chaotic signal masking and its recovery. Let's consider an example, a signal m is added to state $x_1$ of the transmitter as $s = x_1 + m$. It is assumed that for masking signal to noise ratio of $m$(t) is lower than $x_1$. Here, the basic idea is to use the received signal to generate masking signal at the receiver and subtract it from the received signal to recover $m$. If the receiver has synchronized with $s$ as the drive, the $y_1 = x_1$ and consequently $m(t)$ is recovered as $\hat{m} = \mathrm{s} - y_1$. Using above synchronization scheme, synchronizing error dynamics between transmitter and receiver can be written as:

$$\begin{cases} \dot{e}_1 = wm - y_2^2 + x_2^2 + u_1 \\ \dot{e}_2 = -\mu e_2 + \mu e_3 \\ \dot{e}_3 = ae_2 - be_3 + my_2 = x_1e_2 + u_2 \end{cases} \tag{21}$$

# 8. 8.DESIGN OF SWITCHING SURFACE AND CONTROLLER

The SMC technique to achieve synchronization for secure communication for pair of chaotic system (19) and (20) involves two major steps as discussed in Section 5 provided selection of sliding surfaces in (23). So, that equivalent sliding mode error dynamics is written as:

$$\begin{cases} \dot{e}_1 = -k_1 e_1 \\ \dot{e}_2 = -\mu e_2 + \mu e_3 \\ \dot{e}_3 = -\mu e_2 - k_2 e_3 \end{cases} \tag{22}$$

To ensure the occurrence of the sliding motion, controller is proposed as follows:

$$\begin{cases} u_1 = wm - x_2^2 + y_2^2 - k_1 e_1 - \psi(\mathrm{sign}(s_1)) \\ u_2 = -ae_2 + be_2 - my_2 - x_1 e_2 - \mu e_2 - k_2 e_3 - \psi(\mathrm{sign}(s_2)) \end{cases} \tag{23}$$

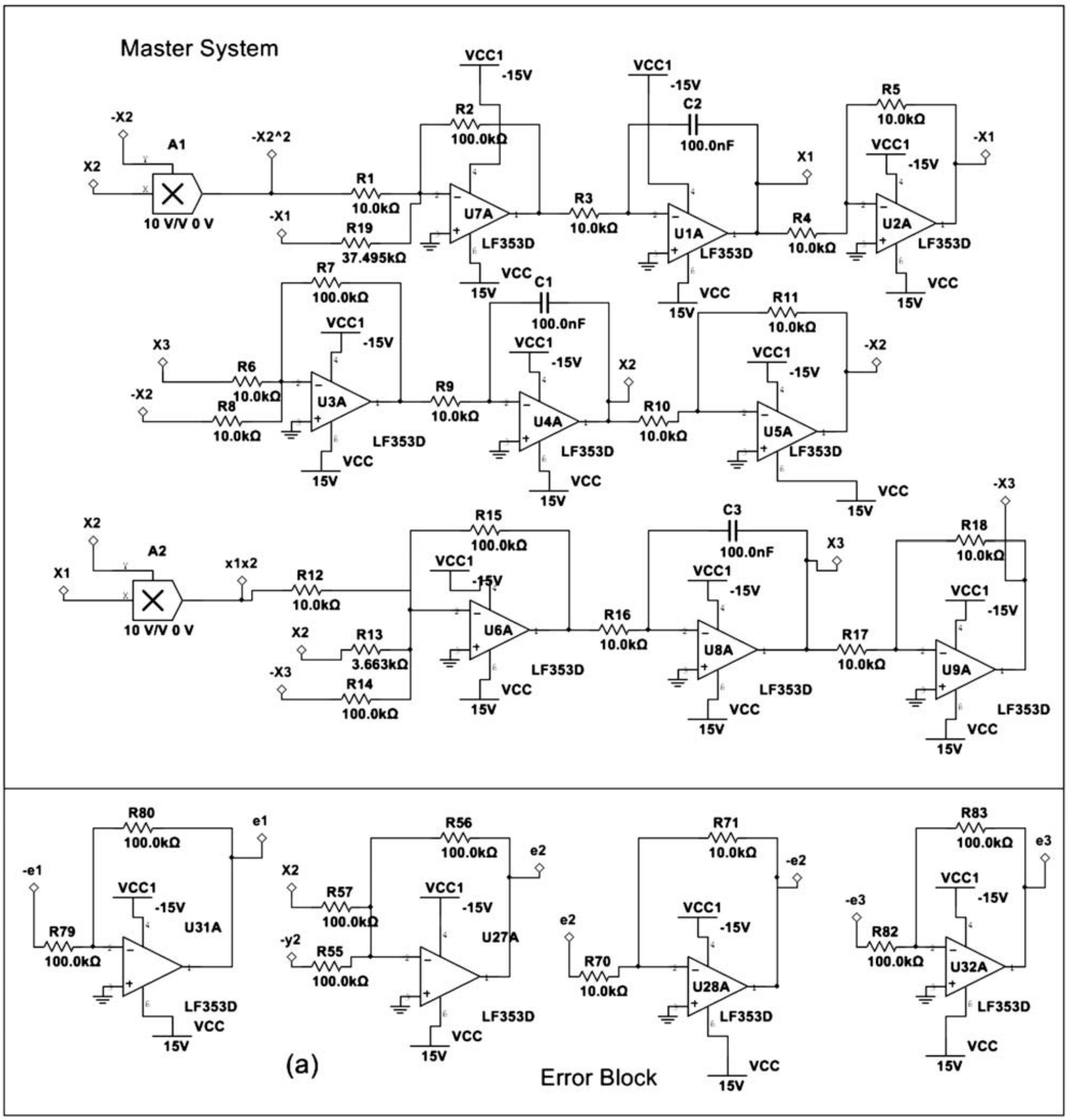



**Figure 3: (*a*)**

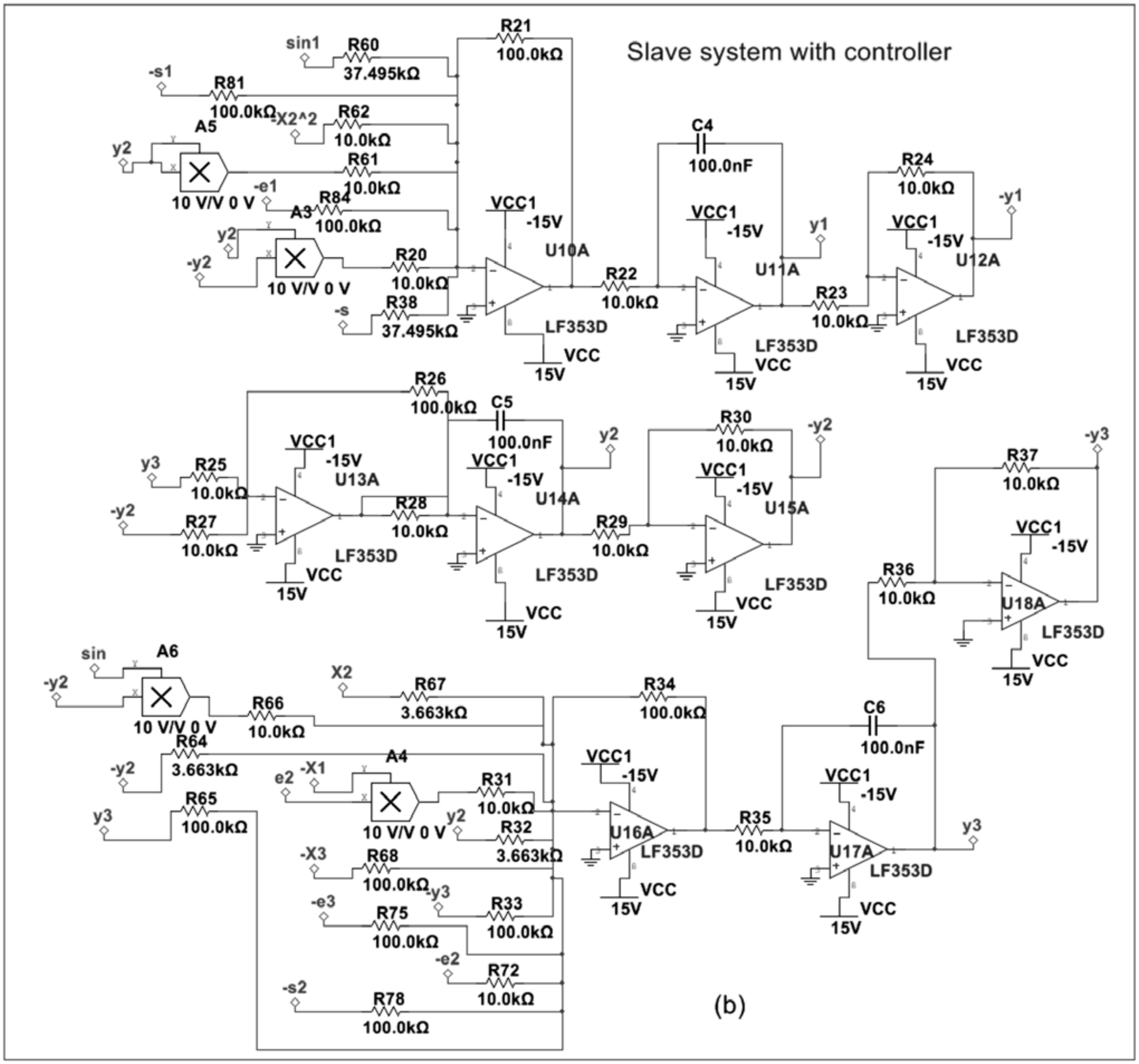



**Figure 3: (*b*)**

where, $\psi > 0$ has to be selected suitably. As per Theorem control $u_1$, $u_2$ of (23) causes the trajectory of the master and slave systems to converge onto the sliding surface $s(t) = 0$ and satisfies $\lim_{t \to \infty} \|e_i(t)\| = 0$. Thus, according to Lyapunov stability theory $s(t)$ always converges to switching surface s(t)=0. Hence, error dynamics in sliding manifold is asymptotically stable and error dynamics converges to zero and message can be retrieve at the receiver. The circuit design is shown for the secure communication in the Fig. 3.

## 9. RESULTS AND DISCUSSION

Results are simulating with time step 0.005 and running for 10 seconds. For analog circuit design and simulation MULTISIM is used. Circuit simulation of system synchronization, anti-synchronization and respective controllers, sliding surfaces is designed successfully with application to secure communication.

### 9.1. MATLAB Simulation Results

The initial conditions to simulate the synchronization and anti-synchronization, corresponding controllers and the error dynamics are $x(0) = [(10\ 20\ 30)]^T$ and $y(0) = [17\ \ 22\ 9)]^T$. Parameters of BG system (1) for chaotic behavior are $\alpha = 27.3$, $\beta = 1$, $\mu = 10$, $w = -2.667$ [27]. Please refer Figs. 4-6 for the simulation results.

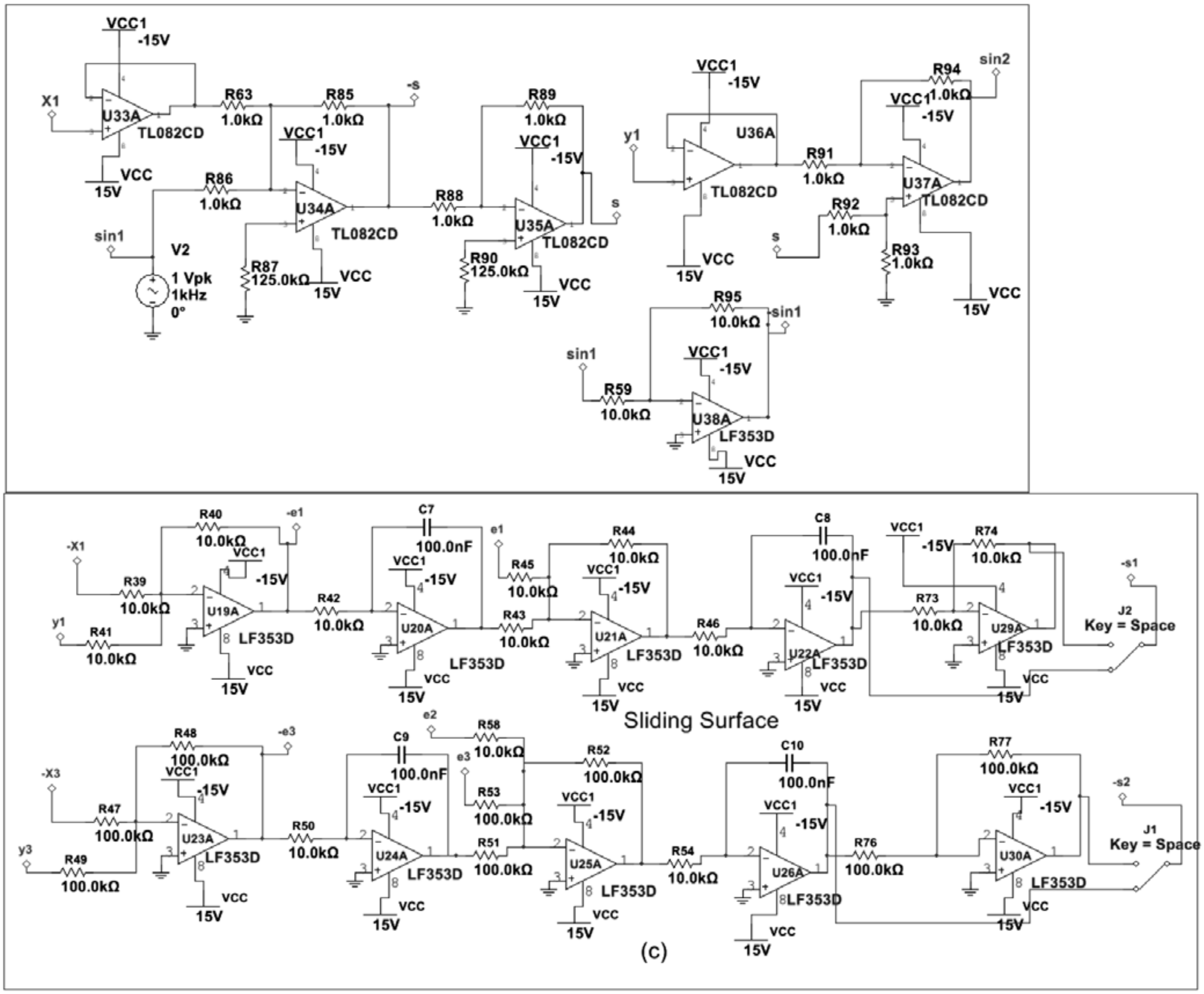


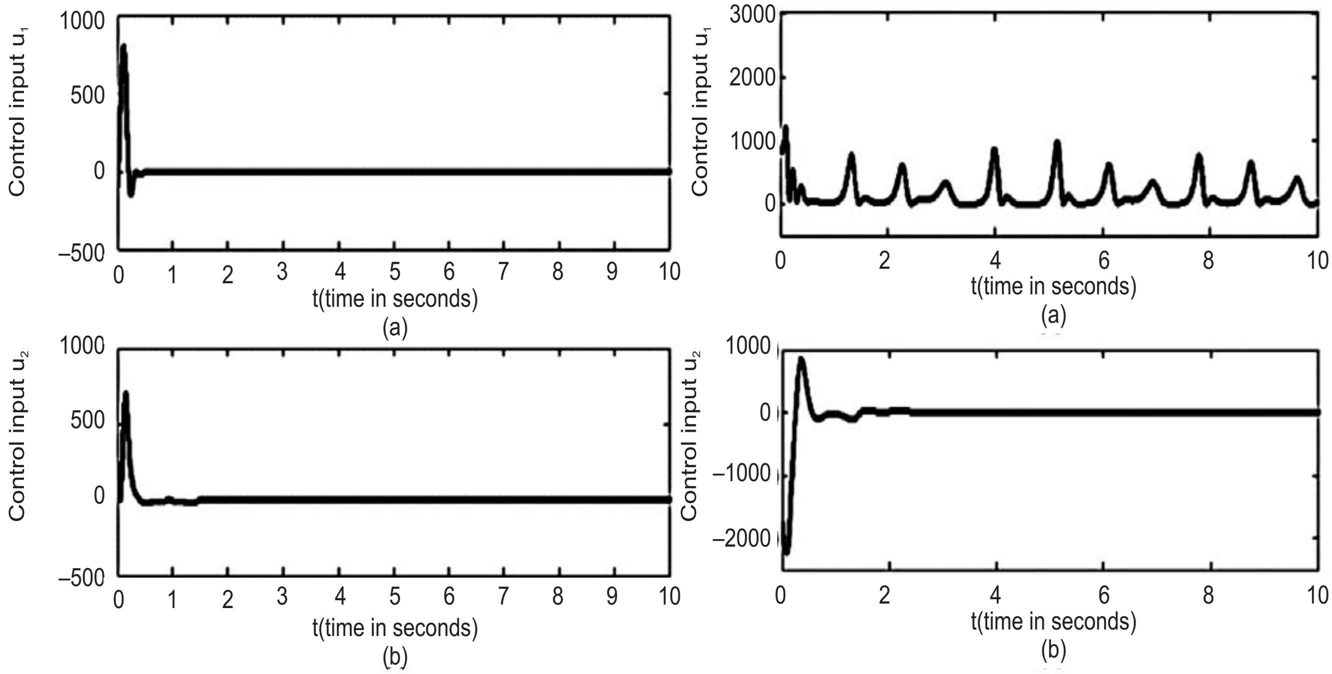

**Figure 3: Circuit design for secure communication using Bhalekar-Gejji chaotic system**

## 9.2. MULTISIM Circuit Simulation Results

The initial conditions for simulating the synchronization and anti-synchronization of states, controllers and error dynamics, are $x(0) = [(0\ \ 0.2\ \ 0.2)]^T$ and $y(0) = [(0\ \ 0\ \ 0)]^T$. Synchronized and anti-synchronized states response is given in the Fig. 7 in LHS and RHS, respectively. Communication circuit design (Fig. 3) and message signal at the transmitter end and recovered signal at receiver end using Multisim is shown in Fig. 8 in LHS and RHS, respectively.

## 10. CONCLUSIONS AND FUTURE SCOPE

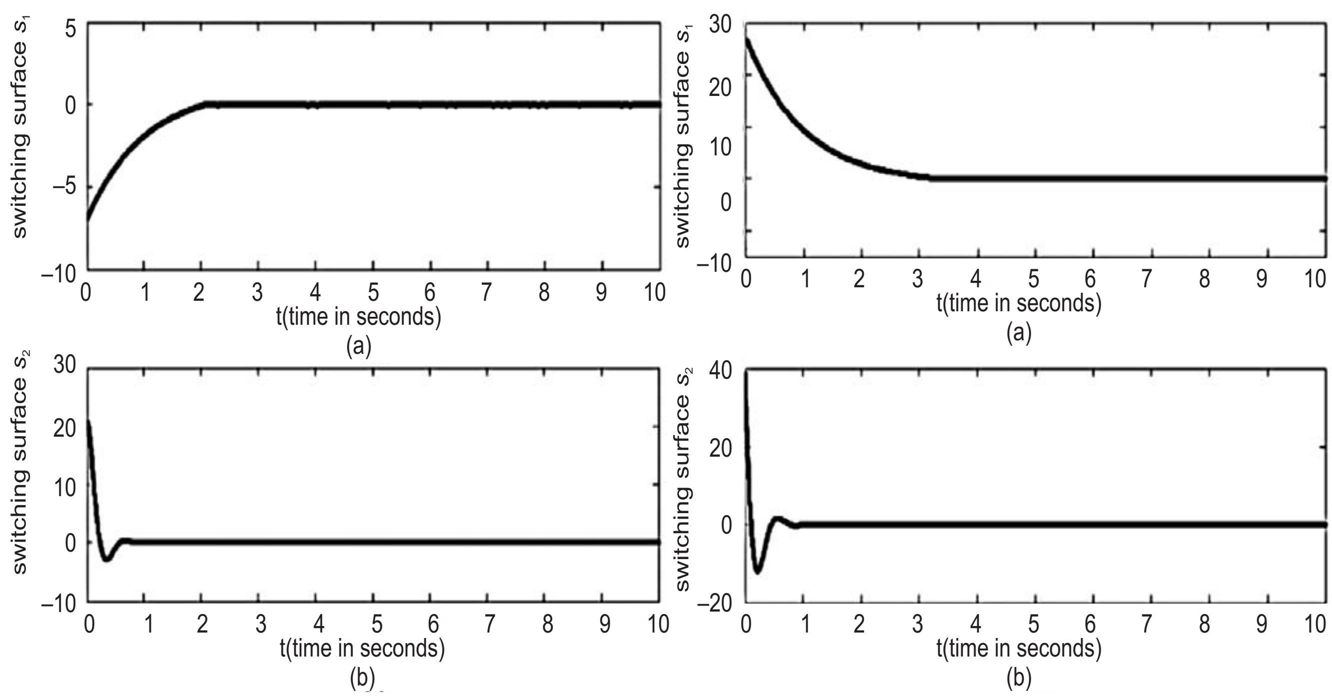
In this paper, global synchronization and anti-synchronization scheme with application to secure communication is presented to investigate first time in literature for newly developed Bhalekar-Gejji (BG) systems. SMC have been proposed to guarantee the occurrence of global asymptotic stability. It has been shown that the master and slave systems are synchronized and anti-synchronized by proper design of the control and stable switching surface. The proposed control forces the system states onto the switching surface. Application to secure communication shows the synchronizability of Bhalekar-Gejji chaotic systems in the drive-response framework. Finally, numerical simulations are presented to show the effectiveness of the proposed synchronization and anti-synchronization schemes. Further, analog circuit design and realization for proposed synchronization, anti-synchronization and application to secure communication is carried out and achieved for hardware realization. Proposed synchronization scheme can also be used in the complex dynamical network such as small world network and scale-free networks. It may be the future direction for researchers to precede and explore this work further.




I. Variation of control input with respect to time for synchronization. (*a*) control input $u_1$ with respect time, and (*b*) control input $u_2$ with respect to time.

II. Variation of control input with respect to time for anti-synchronization. (*a*) control input $u_1$ with respect time, and (*b*) control input $u_2$ with respect to time.

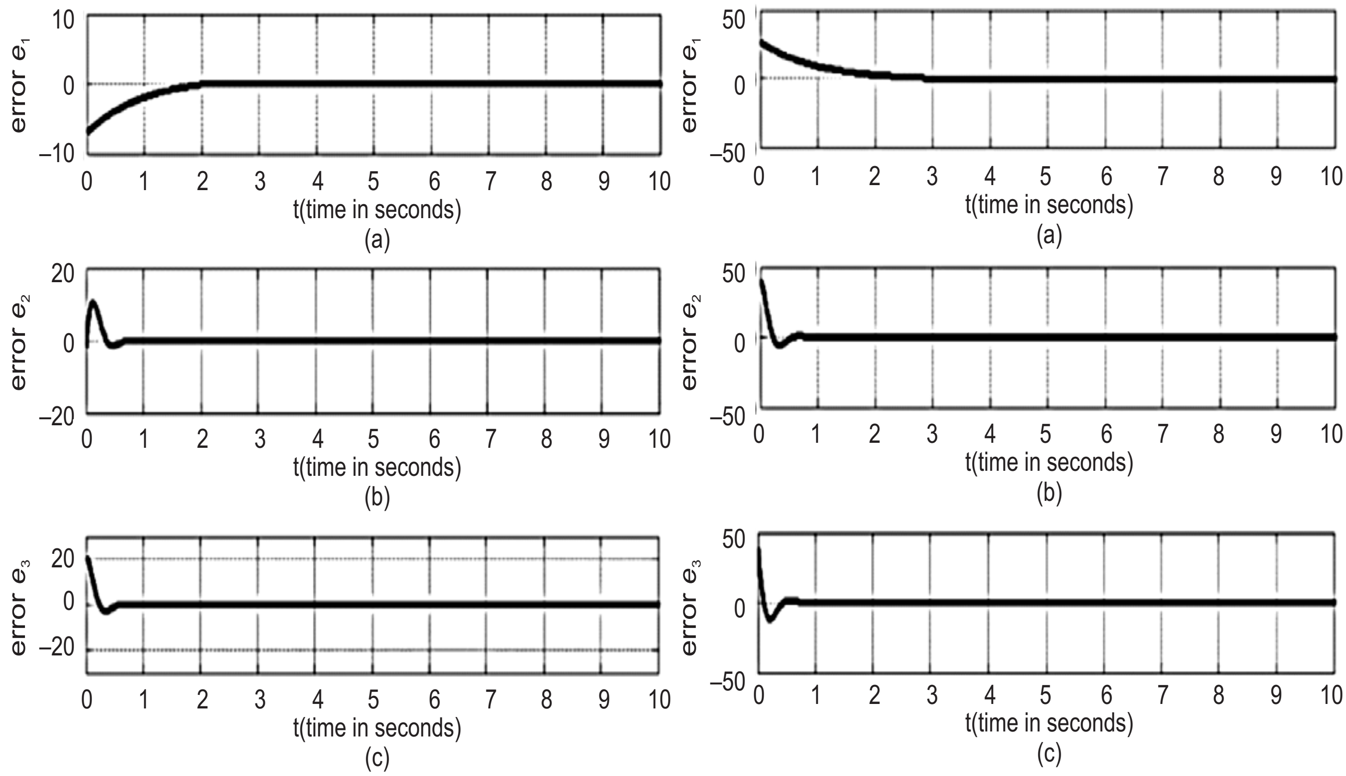
**Figure 4: Variation of control input for synchronization**




I. Switching surface stabilization for synchronization. (a) surface $s_1$ with respect to time, and (b) surface $s_2$ with respect to time.

II. Switching surface stabilization for anti-synchronization. (a) surface $s_1$ with respect to time, and (b) surface $s_2$ with respect to time.

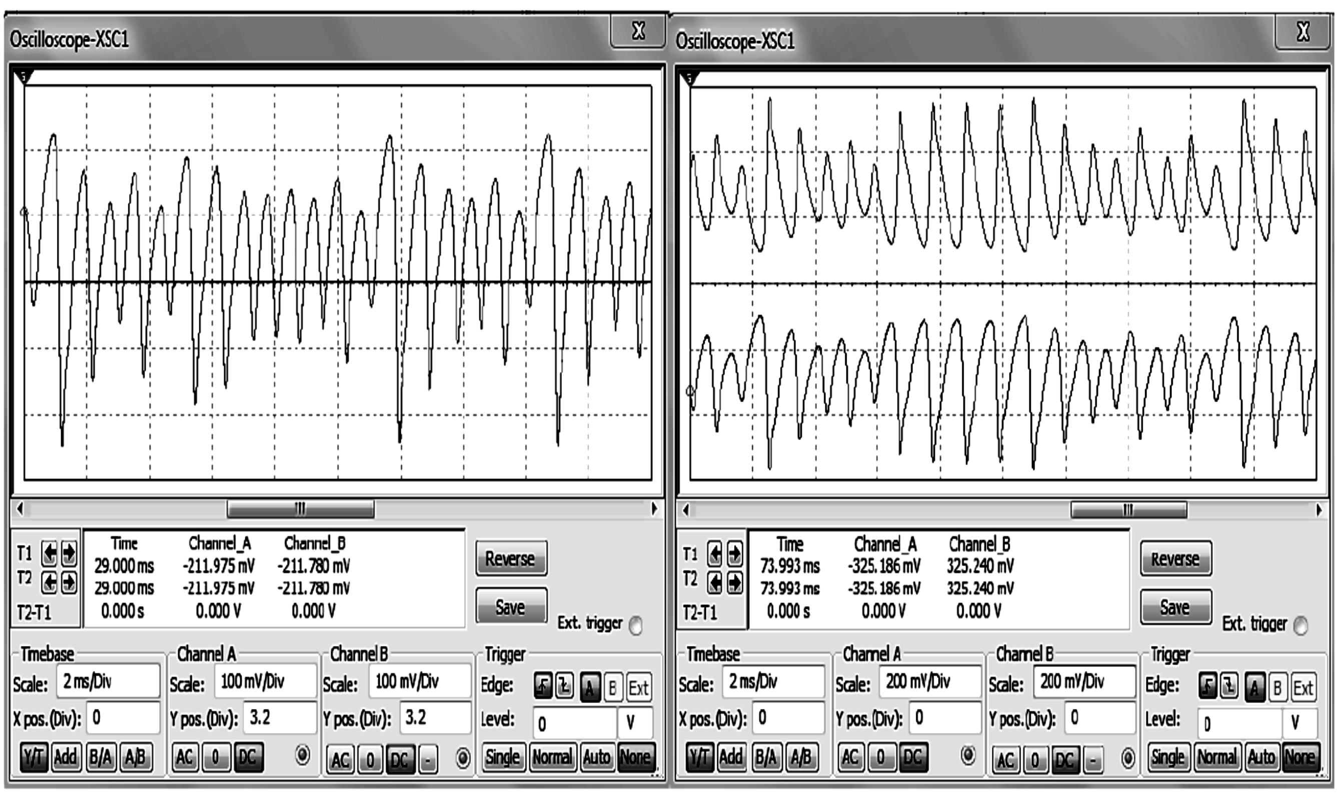
**Figure 5: Switching surfaces stabilization for synchronization and anti-synchronization**



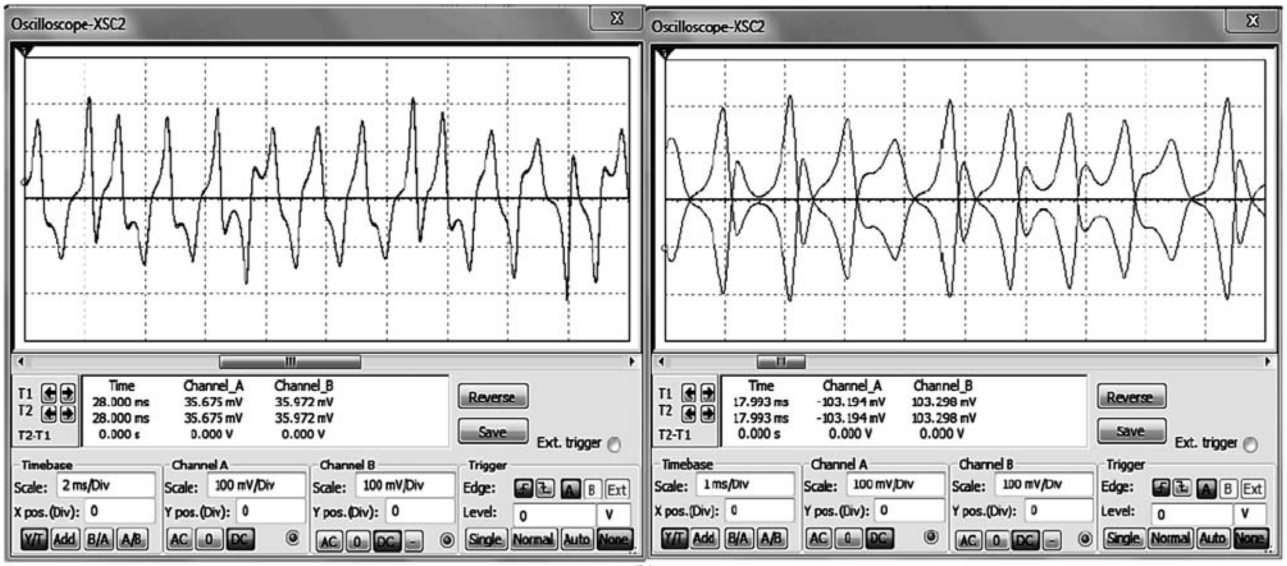

I. Synchronized error response between states of Master and Slave systems with respect to time. (a) error $e_1$ between first state, and (b) errro $e_2$ between second state, (c) error $e_3$

II. Anti-synchronized error response between states of Master and Slave systems with respect to time. (a) error $e_1$ between first state, and (b) error $e_2$ between second state, (c) error $e_3$ between third state.

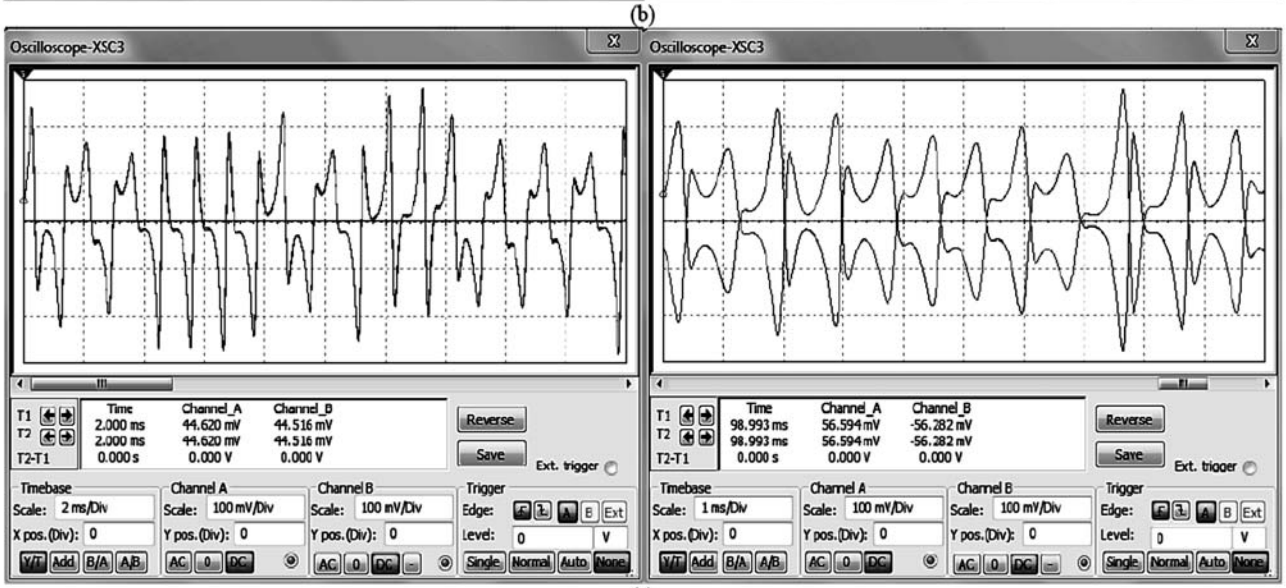
**Figure 6: Dynamic error for synchronization in I, and anti-synchronization in II**




(a)

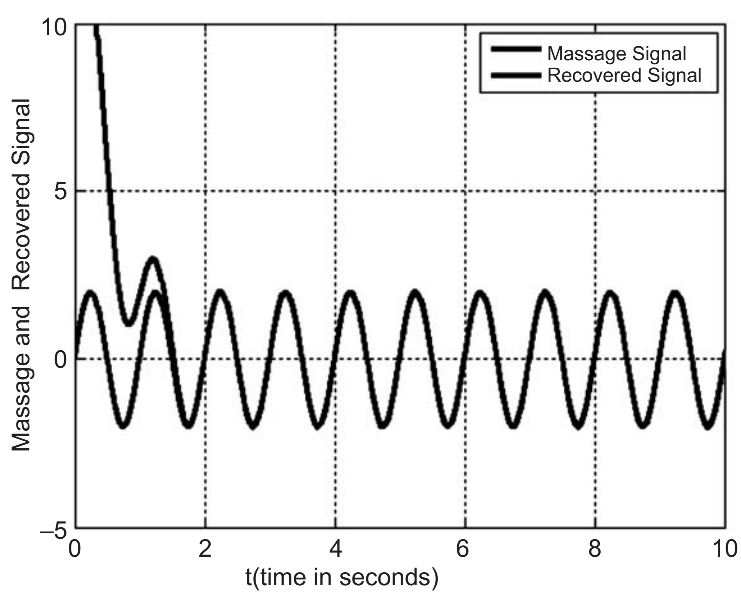



(b)




(c)

**Figure 7: Synchronized (in LHS) and Anti-synchronized (in RHS) states: first, second and the third states of master and slave systems in (*a*), (*b*) and (*c*), respectively**



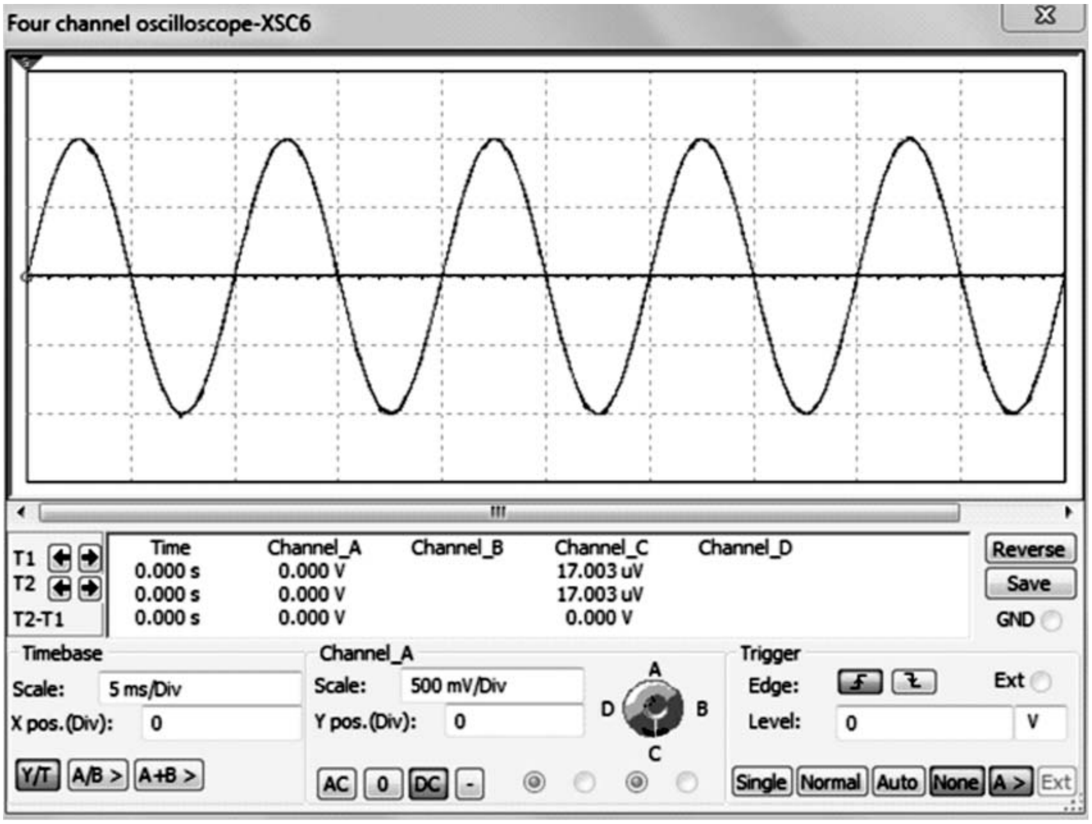



**Figure 8: Masked Message signal (red line) at the transmitter end and recovered signal (green line) at the receiver end**

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