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An Efficient Genration of Oscillation Signals By Fault Detection and Test Generation Method in Combinational Circuits

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ABSTRACT

Testing is one of the crucial problems to be solved in digital circuits. Since they are interconnected with gates and their behavior, controllability and observability of internal signals become significantly more costly than in other circuits. A novel approach is presented for automatic test pattern generation and oscillation ring test methodology for combinational circuits. The techniques used for this purpose is used to detect faults and generate the test pattern for the design circuit. The fault model being used is the input stuck-at model. Two algorithms are proposed namely oscillation test pattern generation algorithm and D-algorithm for fault detection and to generate test pattern. Experimental results show that generation of test vectors for the combinational circuits with high fault coverage.

Index Terms: Oscillation test, delay fault, stuck-at faults, test generation, ATPG.

I. INTRODUCTION

The Test Generation patterns are applied in digital circuits to check the circuits are good ones from faulty ones. The test patterns are applied at the inputs of the circuit called primary inputs. The effects of the test are observed at the outputs of the circuits called primary outputs. Thus, test pattern is also called as test set and it cause all faulty circuits to exhibit different behavior from good circuits at the primary outputs. Delay defect can be found in the circuits in which decreasing and increasing of feature sizes clock speeds and these are combined to alter the delay defect effects. Recent evidence indicates that delay defects can no longer be ignored. The detection of delay faults requires at-speed test techniques, which creates signal transitions to be captured at normal speed it is explained in the Scan-based test techniques [1]. For stuck-at faults the slow scan-based tests are used to delay test and a desirable test methodology is built for the at-speed test and it must be cost-effective method. Due to the lack of controllability and observability in internal storage elements, the sequential testing is difficult and it is explained in the Sequential automatic test pattern generation (ATPG) [2], and it may not be able to achieve high fault coverage with sequential testing. The sequential circuits can be tested using the design for testability (DFT) technique, scan tests are usually carried out in lower speed. An oscillation ring is a closed loop with an odd number of signal inversions. The circuit under test (CUT) is fault-free, if the oscillation signal appears on the ring otherwise the CUT is seemed faulty. An efficient and effective method to detect faults is the oscillation-based test and is explained in [5]by testing analog circuits, digital circuits, and system-level interconnects.

II. OVERVIEW

The oscillation test method forms a ring through a feedback path which is provided from circuit output to circuit input. This test has been proposed for digital circuits testing. As long as there are odd inversions

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along this ring, an oscillation signal is generated. To obtain oscillation test in asynchronous design is difficult, because of occurrence of the race problems. In this brief, a different way to carry out the oscillation test in digital circuits is proposed. The synchronous designs are made by using system clocks to control the feedback paths. The idea is to force a circuit moving back and forth between two states in consecutive cycles with ûxed primary inputs. Then the oscillation signal is observed at its output when its primary output whose value changes in the two states. An example is demonstrated in which implements the FSM given in Fig. 1. With primary input X = 1, the next state (NS) is f if the present state (PS) is e, and vice versa. Note that output Z is 0 when PS is e with X =1, and output Z becomes 1 when PS is f with X =1. Thus, if the circuit is initialized to either state e or f with X = 1, the FSM changes back and forth between these two states. The goal is to find the fault detection and to apply the test generation algorithm [3]-[4]. The fault detection scheme and the test generation algorithm are presented in this section.

III. PROPOSED SYSTEM

Fault Detection Scheme

The inputs of the combinational logic consist of the primary input (PI) part and the PS part, whereas the outputs are divided into the primary output (PO) part and the NS part. Oscillation tests are sensitized the signal paths from PS to both PO and NS, transition test are sensitized the paths from PI to PO and NS. For each input-output pair, the proposed method generates tests such that if a transition (0 ’! 1 or 1’!0) is applied to the input, a signal transition appears at the output. In other words, a path between the input-output pair is sensitized.

To Detect Delay Faults

The modified state register (MSR) is designed to facilitate the function of test generation. An example of FSM given in fig.1 shows state transition, output of the FSM model and the test pattern generation from an FSM model. The oscillation signals are determined through the output table.

Present State(PS)	*Next State(NS)*		*Output(Z)*	
	X=0	*X=1*	*X=0*	*X=1*
a 000	a 000	c 010	1	0
b 001	d 011	b 001	1	0
c 010	f 101	d 011	1	1
d 011	c 010	a 000	0	1
e 100	e 100	f 101	0	0
f 101	b 001	e 100	1	1

Figure 1: State transition of an FSM

An oscillation signals can also be generated without MSR cells but it is achieved when both the next states and outputs of a state pair are alternating. Unfortunately, other states doesn’t have this condition that wont satisfy the oscillation condition. So, MSR is used to change the state pairs only if their corresponding outputs are different. Delay faults can be derived in two patterns one is associated with primary inputs to either PO or NS and another one is from the FSM model by checking the outputs corresponding to the same PS. In order to produce the oscillation signals MSR cells are used by changing the state of some of the selected next state functions in the test mode. A modified state transition table is shown in Fig. 2.

Present	*Next State(NS)*		*Output(Z)*	
State(PS)	*X=0*	*X=1*	*X=0*	*X=1*
a 000	a 000	c 010	1	0
b 001	e100	b 001	1	0
c 010	f 101	d 011	1	1
d 011	c 010	a 000	0	1
e 100	b 001	f 101	0	0
f 101	b 001	e 100	1	1

Figure 2: Modified State transition of an FSM

The oscillation signals can be generated in the state pairs b and e in the Fig. 1, because the outputs of the state pair b and eat X = 0 can be modified to the next states of (b, e) from (d, e) to (e, b) when X = 0 in the test mode, shown in Fig. 2. The truth table of state bit transition is shown in fig no. 3, and the operations of MSR cell state can be explained briefly.

BIT TRANSITION	*OPERATIONAL VALUE*
0 —> 0	LOW
0 —> 1	RISE
1 —> 0	FALL
1 —> 1	HIGH

Figure 3: Truth table of state bit

The truth table indicates the change of bit in the states that is change of bits in the current and next state of the same. Then the four operations of MSR is deûned: 1) LOW state - when both the current and next states are “0”; 2) RISE state –changes from “0” to “1” on both the current and next states; 3) FALL state - changed from “1” to “0” of both the current and next states; 4) HIGH state - when both the current and next states are “1”. For example, consider state f (=101) with input X = 1 in Fig.1. Since the next state is e(=100), the OP values are (H, L, F) for the three state bits.

TO DETECT STRUCK-AT-FAULTS

Automatic Test Pattern Generation (ATPG): To automate the current circuit, we use an automatic test pattern generation or ATPG algorithm, a test to find all the possible stuck-at faults in the fault set of interest. The sequence of operations in the algorithm is like: to pick a fault that has not been detected and then to construct the search graph for the circuit with the chosen fault. Then the search space is searched until a test is found or the space is exhausted.

The test is recorded along with the expected output and the target fault if the algorithm terminates at 3a. And no test exists if it terminates at 3b, and then the fault cannot be detected; that is, it is undetectable, or redundant. The circuit graph determines the graph of the circuit and search graph is the graph of the search space. The search graph might be changed by target fault and search procedures and these search graphs can be built by using the circuit graph. Backtracking is the process of retracing the search graph to correct the conflicts between node values.R

Backtrack is applied when the ATPG experience a conflict. An example of a fan-out point is shown in Figure 4, in this example node M is the fan-out point. Node T and Node S are the branches of the Fan-out stem M. A reconvergence is point in which the successor nodes of the same signal come together at a subsequent node like node U such as node U shown in Figure 4. The dependencies in the values which is assigned to nodes are introduced by the reconvergent fan-out.

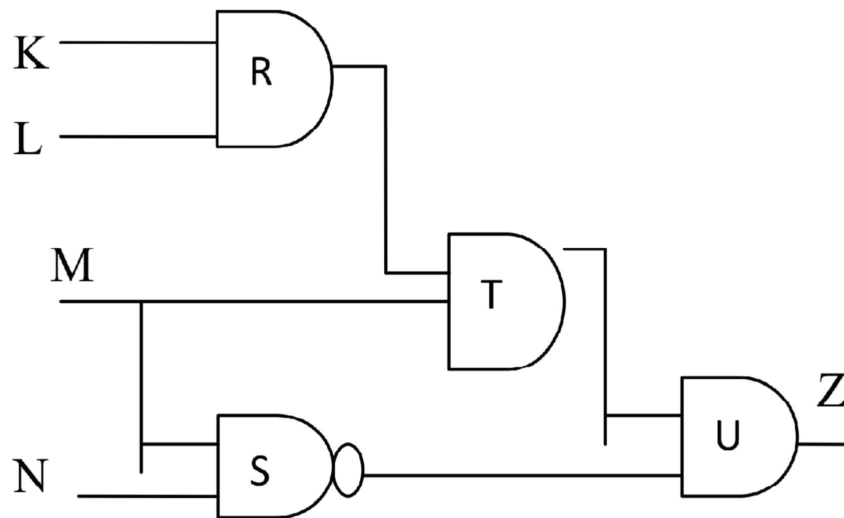

Figure 4: Circuit with reconvergence.

THE D ALGORITHM

The D algorithm is introduced to solve the conflicts for ATPG. The three new values, 1) X (unassigned), 2) D (binary values 0: if it is faulty) and 3) D (binary values 1: if it is good) are added in this D algorithm.

The stuck-at faults are explained using both FSM and circuit, here we use the simple circuit shown in Figure 4, consists of nodes K, L, M, N, R, S, T, U, and Z. The D algorithm searches this nine-node space for each fault considered and this algorithm based on the search space, in figure 4 node T value depends upon the nodes of K, L, and M, as these nodes values are assigned in the circuit and conflict is detected at this point. Suppose if it is not detected and resolved, it is impossible to deal with the subsequent assignments nodes. These are done by moving backward and frontward of the circuit. These conflicts are resolved when inconsistent values are noted in the nodes.

FAUL T SENSITIZING

The first step is to find a fault in the current circuit known as Fault Sensitizing. A fault sensitizing is the process of finding a pattern that should produces a value of 1 at the output for the good circuit. For the above circuit the output of S should produce a value of 1 but the output is stuck-at-0 (s-a-0) considered as a faulty circuit. So we need to get the output of S to 1 for that we have to set the inputs L and M to 1 and this is known as fault sensitization, since the values are different at the fault location on good and the faulty circuit. The search graph is constructed and initializes all the nodes to X, and then choose the fault node of the target circuit and assign it as D for the stuck at 0 fault or D for stuck at 1 fault. After the search begins X is replaced with either 0 or 1 or D, and then the assignments are moved backward and forward in the circuit. These methods are done until the non conflicting set occurs, then the fault has been sensitized.

FAULT PROPAGATION

The second step is the fault propagation; it is used to propagate the difference created by fault sensitizing to a primary output. As T is connected to a primary output we need to set the input from R to T to 0 and to produce a 0 we must set one of its inputs K or L to 0. Since L is already 1,then K must become 0.

In this fault propagation step it keeps checking for the list of the gates that have a D or on one or more inputs and an X on the output. This noted D nodes are drive to PO of the fault, this driving process is called fault propagation. We have to sensitize the fault before propagating it. Initially all the nodes in the circuit is denoted as X, for example take node T, a value of D is assigned to this node. The node T (=1) in the good

circuit and T(=0) in the faulty circuit, and we must make sure the node T as 1 if it is in faulty circuit and to change this M and R node must be 1. We need to make sure the non conflicts assignment and then we have to justify the value M and R.As the M value is justified already since it is a primary input, and the value R is justified as follows. The value K and L is set to 1, so the output R will be 1 and then R and T values are immediately justified. As the example circuit contains AND gate, all other inputs of the gate must be 1 to propagate the D value from T to its PO for the successful achievement of fault propagation. The PI of N is set to 0 because to assign the value 1 in S and its companion M is already set to 1.So, D and Z values are propagated to the output of U where the Primary Output is directly propositional to the value Z is directly connected to the PO; because of no more nodes there to be set the value D can be observed at PO Z.

CONCLUSION

The algorithms for fault detection and test generation are applied in the Xilinx synthesizer. And the experimental results showed that with the expected good circuit output and the target fault for which the test was generated. The test efficiency is achieved for both delay and stuck-at faults through the algorithms and in future these faults can be efficiently tested using various algorithms.

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