I J C T A, 10(5) 2017, pp. 561-567

Modified Single Phase H-Bridge Multilevel Inverter Topology with Reduced Number of Switches and DC Sources

D. Ramachandrarao[*] and O. Chandrashaker[**]

Abstract: The multilevel electrical converter utilization has been raised since the last ten years. These new variety of inverters are appropriate in various high voltage & high power application because of their ability to create waveforms with better harmonic spectrum and devoted output. This paper presents a construction electrical converter configuration that is meant by insertion of a bi-directional switch between electrical phenomenon voltage sources and a traditional H-bridge module. The changed electrical converter will manufacture a more robust sinusoidal waveform by growing the number of output voltage levels. By serial association of 3 modified H-bridge modules, it's possible to provide 11 output voltage levels as well as zero. Multi carrier phase-shifted pulse-width modulation methodology is employed to come up with control signals. The analysis of the output voltage harmonics is allotted. From the results, the proposed inverter provides higher output quality with comparatively lower power loss as compared to the other typical inverters with constant output quality.

Keywords: Cascaded H-bridge multilevel inverter (CHB), In phase Opposition modulation technique, carrier based pulse-width modulation, total harmonic distortion (THD).

1. INTRODUCTION

Over the past twenty years, multilevel inverters have attracted wide interest each within the scientific community and within the trade. The explanation for the magnified interest is that the multilevel inverters are a viable technology to implement controlled motion movement in high-power applications. [1] multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of that generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, that reach high voltage at the output, while the power semiconductors should stand up to solely reduced voltages. Structure converters have lots of benefits to supply in medium- to high-voltage range of applications. These include variable speed motor drives and grid applications. Multilevel converters will synthesize waveforms using more than 2 voltage levels, little filter elements are needed and generally they will be ignored altogether. Disadvantages of multilevel topologies include: high number of semiconductor devices, complex control as a results of the big range of controlled devices, large number of gate drive circuits, many DC voltage sources are needed, need to balance voltages across capacitors used in potential divider circuits. There are differing kinds of multilevel circuits concerned.

The primary topology introduced was the series H-bridge design. This was followed by the diode clamped convertor, which used a bank of series capacitors. A later invention elaborate the flying capacitor style in which the capacitors were floating instead of series-connected. Another structure style involves parallel association of electrical converter phases through inter-phase reactors. In this style, the semiconductors block the complete dc voltage, however share the load current. Many combinational styles have additionally emerged some involving cascading the basic topologies.[2] These styles will produce higher power quality for a given range of semiconductor devices than the basic topologies alone as a result of a multiplying

[*] M.Tech Student, K.L. University, Vaddaswaram, Andhrapradesh, India. *Email: doggaram@gmail.com*

[**] Prof (Hod in EEE), K.L. University, Vaddaswaram, Andhrapradesh, India. *Email: Sekhar.obbu@gmail.com*

result of the quantity of levels. The multilevel inverters are in the main classified as diode clamped, Flying capacitor electrical converter and cascaded multilevel electrical converter.[12] The cascaded multilevel management methodology is incredibly simple once compare to different multilevel electrical converter as a result of it doesn't need any clamping diode and flying condenser. During this paper, we have a tendency to are employing a new topology of cascaded H-bridge multilevel electrical converter for producing 11 output voltage levels and for that we have a tendency to are using multicarrier modulation technique. This paper is organized as follows: the inverter's configuration is conferred in Section II, the PWM modulation strategy in Section III, the MATLAB implementation in Section IV and Section V is that the conclusion.[2]

2. PROPOSED TOPOLOGY

Cascaded multilevel inverter has the advantage of most reliable and to realize the best fault tolerance due to its modularity; a feature that allows the inverter to continue operational at lower power levels once cell failure. Modularity additionally permits the cascaded multilevel inverter to be stacked simply for high power and high voltage applications.[2-2] The cascaded multilevel inverter generally contains many identical single phase H-bridge cells cascaded in series at its output side. This configuration is usually cited as a cascaded H-bridge (CHB), which may be classified as symmetrical if the dc bus voltages are equal altogether the series power Bridges, or as asymmetrical if otherwise. The most disadvantage of the traditional cascaded H-bridge is that when the voltage level will increase, the quantity of semiconductor switches will increase and additionally the supply needed will increase. So as to overcome this introduced a new topology of cascaded H-bridge. The most advantage of this topology is that the quantity of switches needed is reduced and additionally the quantity of sources. Figure 2.1 shows the new Basic cascaded 5 levels H-bridge multilevel inverter. It's further one two-way switch connected between the primary leg of the H-bridge and also the capacitor midpoint, enabling 5 output voltage levels.[2-3]

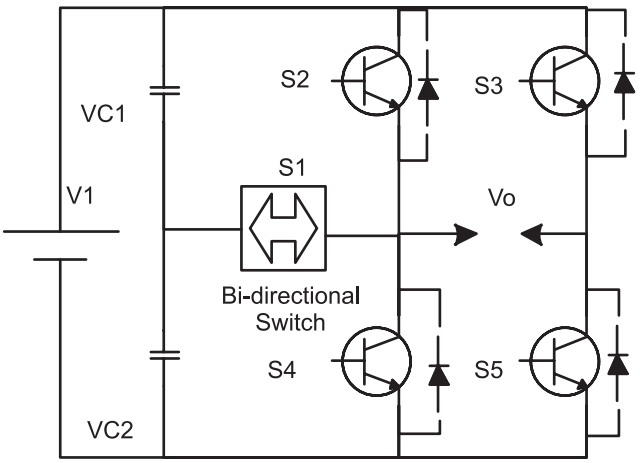

Figure 2.1: General Topology for Five level Output

It has five output voltage levels i.e. V_{dc}, $V_{dc}/2$, 0, $-V_{dc}/2$, $-V_{dc}$. For getting the output voltage V_{dc}, the switches S1, S4 need to be turned on. Similarly for output voltage $V_{dc}/2$ switches S5, S4 need to be turned on, for 0 either S3, S4 or S1, S2 need to be turned on; for $-V_{dc}/2$ switches S5,S2 need to be turned on; for $-V_{dc}$ switches S3, S2 need to be turned on.

In the circuit shown in Figure 1, single H-bridge module is capable of producing five level output voltage. Each inverter module is capable of producing 2E, E, 0, –E, –2E. That means by using two bridges 9 level output voltage is produced. The total output voltage is sum of the outputs of the inverter modules and the nine voltage levels are 4E, 3E, 2E, E, 0, E, –2E, –3E, –4E.

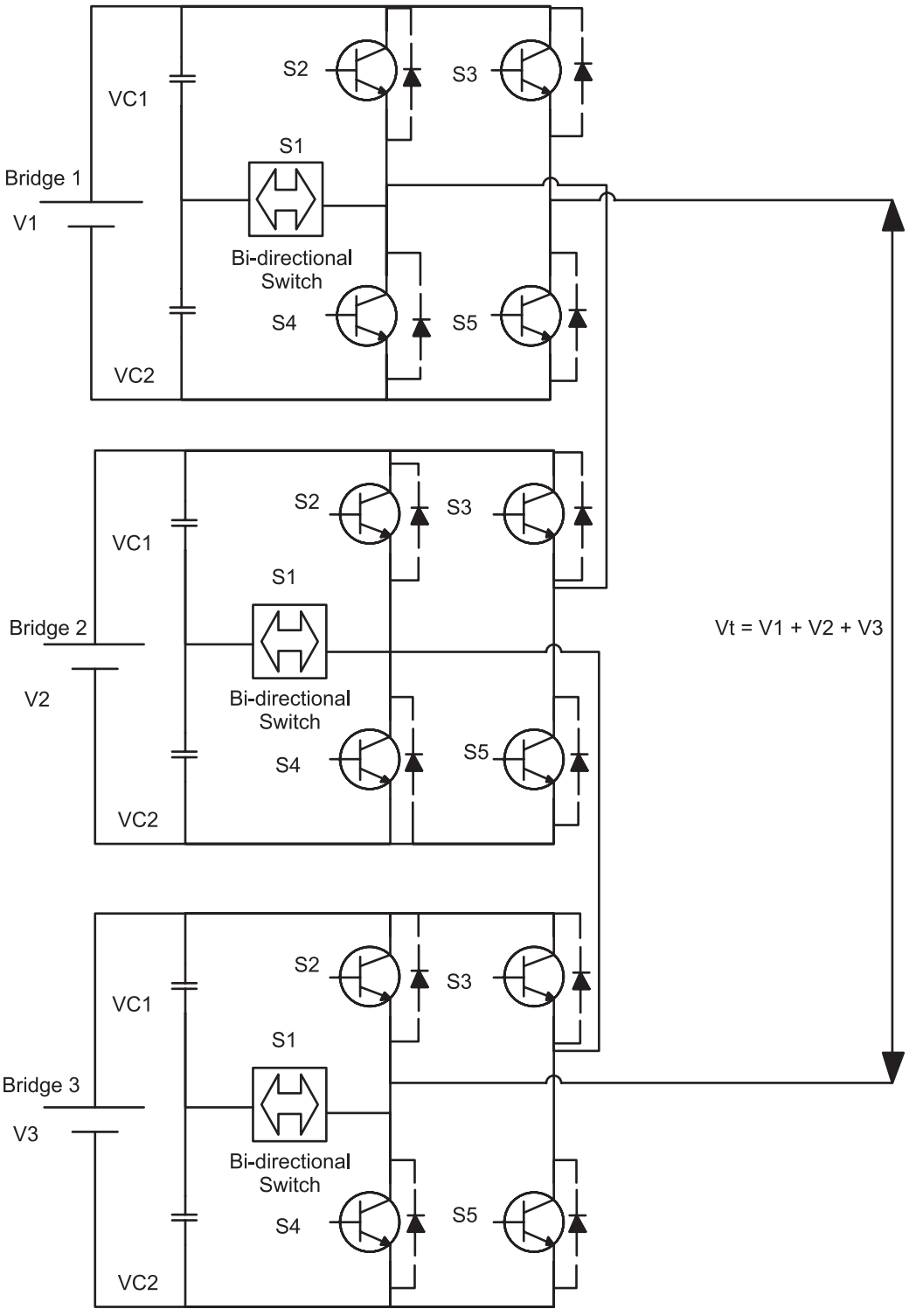

Figure 1.2: Eleven level H-bridge Multilevel Inverter

For three Bridges we develop a 11 level output voltage As show in Figure 2.2.

The advantages of this proposed circuit is number of switches are reduced. The cost and complexity is less in this circuit. To synthesize nine output voltage levels, it employs two independent dc voltage sources of 2E which are divided into two input sources E in order to secure an additional dc voltage source of E.[11] The inverter module having a bidirectional switch produces 5-levels of output voltage (–2E, –E, 0, E, 2E) by controlling of the switches. Since every output terminal of the inverter module is connected in

series, the output voltage becomes the sum of the terminal voltages of each inverter. The circuit for nine level cascaded H-bridges is shown in Figure 3.1, the gating signals for the inverter is generated by using multicarrier modulation.

3. PWM MODULATION

In this inverter, the sinusoidal pulse width modulation is going to use. In the Sinusoidal pulse width modulation scheme, as the switch is turned on and off several times during each half-cycle, the width of the pulses is varied to change the output voltage. Lower order harmonics can be eliminated or reduced by selecting the type of modulation for the pulse widths and the number of pulses per half-cycle.[9] Higher order harmonics may increase, but these are of concern because they can be eliminated easily by filters. The SPWM aims at generating a sinusoidal inverter output voltage without low-order harmonics. This is possible if the sampling frequency is high compared to the fundamental output frequency of the inverter.[4]

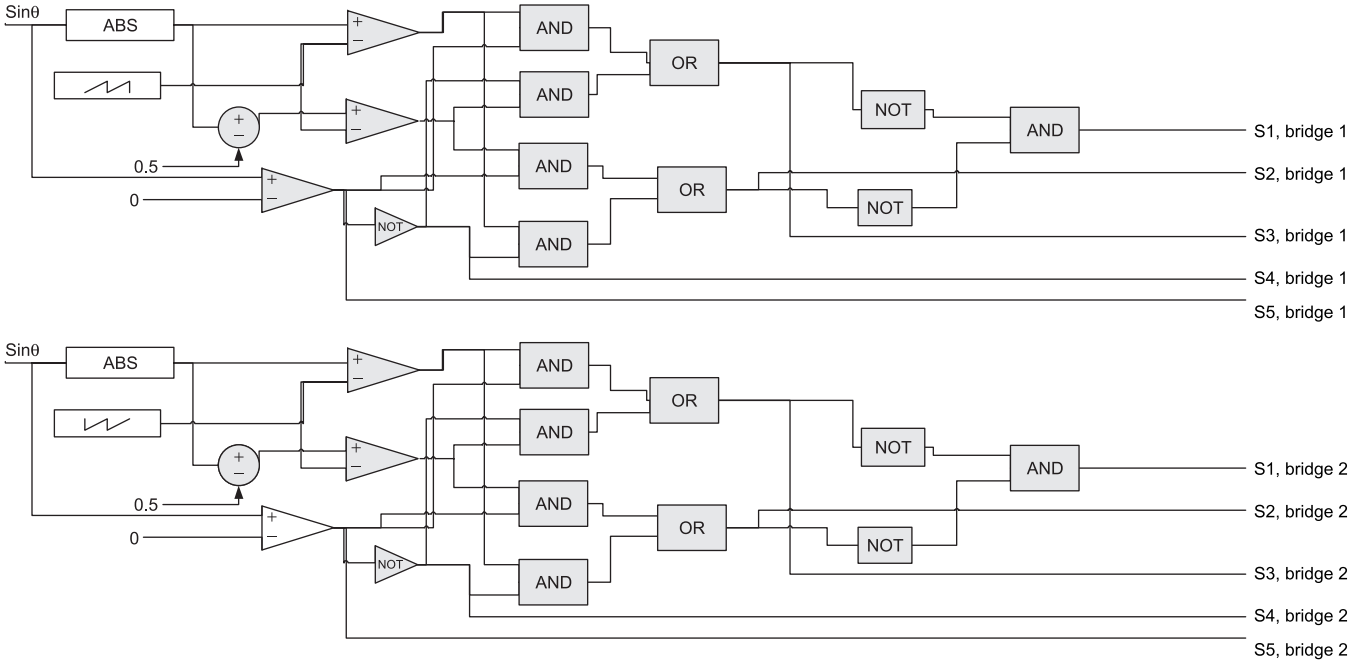

Figure 3.1: Multi carrier Sine PWM Technique

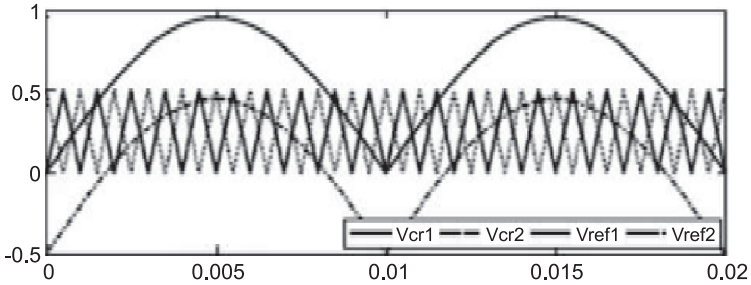

Figure 3.2: In phase opposition technique

The modulation index, M of the proposed multilevel inverter is defined by,

$$M = \frac{1}{2}(V_{ref}/V_{car}) \quad (1)$$

Where V_{ref} is the amplitude of the voltage reference and V_{cr} is the amplitude of the carrier signal. Multicarrier phaseshifted PWM (CPS-PWM) modulation is used to generate the PWM signals.[10] The

amplitude and frequency of all triangular carriers are the same as well as the phase shifts between adjacent carriers. Depending on the number of bridges, the carrier phase shift for each H-Bridge, $\theta_{cr,\,n}$ can be obtained from,

$$\theta_{cr,\,n} = \frac{2\pi(n-1)}{\mathrm{Nc}},\ n = 1, 2, \ldots \mathrm{Nc} \tag{2}$$

For signal generation in each cell, two voltage references and one carrier signal are used. V_{ref} is defined by

$$V_{ref} = M \sin \omega t \tag{3}$$

$$V_{ref\,1} = V_{ref} \tag{4}$$

$$V_{ref\,2} = (V_{ref} - 1/2) \tag{5}$$

Both references are identical but displaced by an offset equal to the carrier's amplitude which is ½. When the voltage reference is between $0 < V_{ref} \leq ½$, $V_{ref\,1}$ is compared with the triangular carrier and alternately switches S1 and S3 while maintaining S5 in the ON state to produce either $½V_{dc}$ or 0. Whereas, when the reference is between $½ < V_{ref} \leq 1$, $V_{ref\,2}$ is used and alternately switches S1 and S2 while maintaining S5 in the ON state to produce either ½ V_{dc} or V_{dc}. As for the reference between $-½ < V_{ref} \leq 0$, $V_{ref\,1}$ is used for comparison which alternately switches S1 and S2 while maintaining S4 in the ON state to produce either $-½\ V_{dc}$ or 0. For a voltage reference between $-1 < V_{ref} \leq -½$, $V_{ref\,2}$ is compared with the carrier to produce either $-½V_{dc}$ or $-V_{dc}$ alternately switches S1 and S3, maintaining S4 in the ON state. It is noted that two switches, S4 and S5, only operate in each reference half cycle. This implies that both switches operate at the fundamental frequency while the others operate close to the carrier frequency. This allows the dc voltage to be switched at a low frequency so as to reduce the switching losses. Figure 3.2 shows the modulation scheme used for the proposed Three Bridge configuration and Figure 3.1 shows a detail block diagram for generating the PWM signals.[5]

4. SIMULATION RESULT

The simulation model was designed using MATLAB/Simulink Software. The gating signals for the inverter are generated by using multicarrier pulse width modulation technique. The circuit was simulated with R L load. Figure 2.1 shows the circuit arrangement with multicarrier modulation.[6]

The output voltage and Current wave farms show in bellow Figures 4.1 to 4.6.

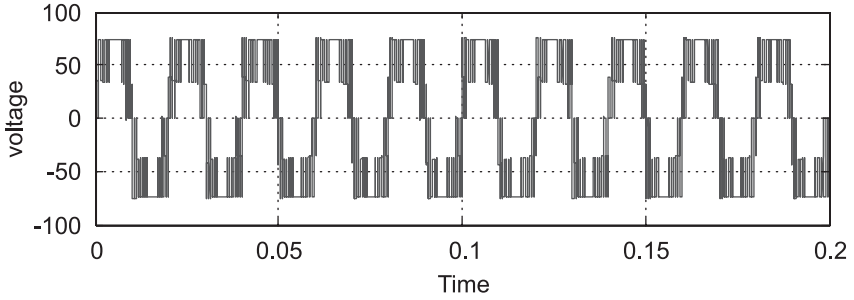

Figure 4.1: Five level level output voltage

5. CONCLUSION

Multilevel inverters have become an effective and practical solution for increasing power and reducing harmonics of ac waveforms. This project deals with the design and implementation of single-phase eleven-level

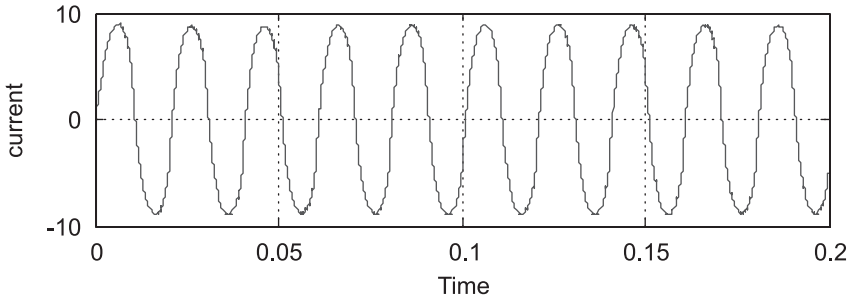

Figure 4.2: Five level output current

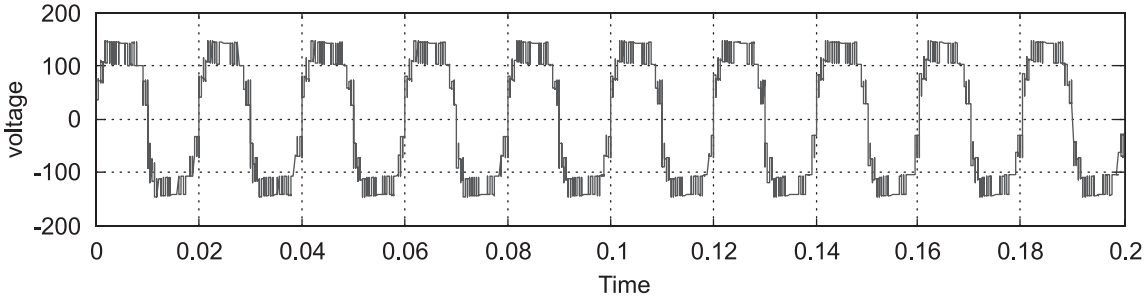

Figure 4.3: Nine level output voltage

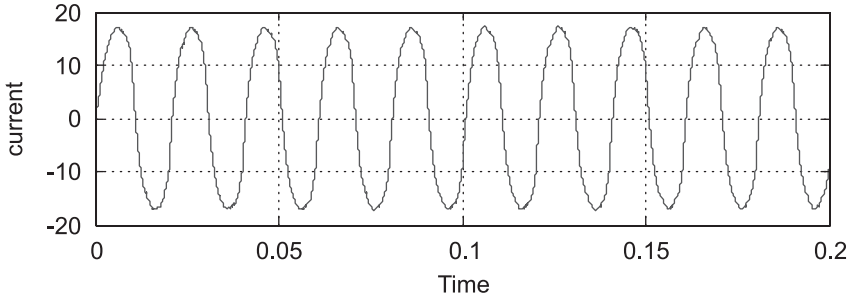

Figure 4.4: Nine level Output Current

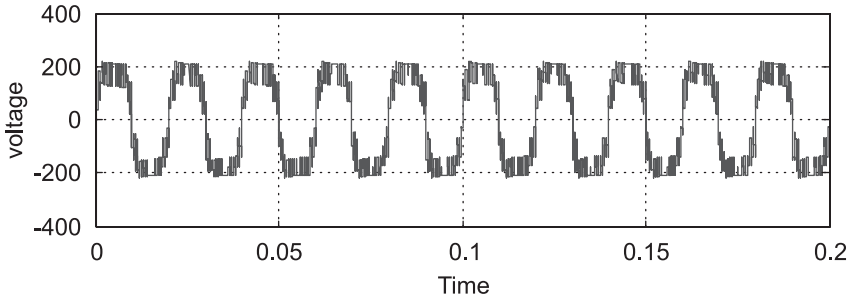

Figure 4.5: Eleven level output voltage

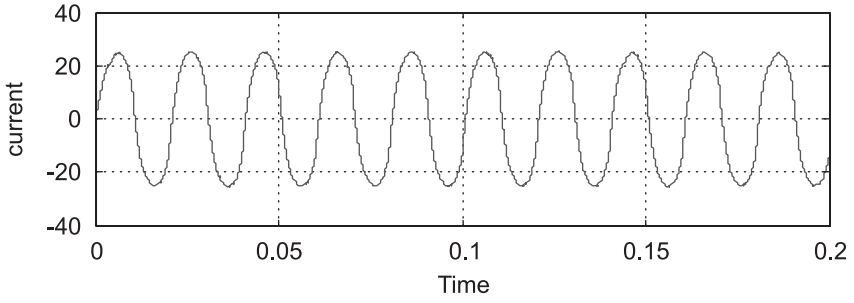

Figure 4.6: Eleven level output current

Cascaded H-bridge multilevel inverter for high power applications with multicarrier phase-shifted PWM modulation method.[7] The simulation implementation of 11-level cascaded H-bridge was made. Along with it, its harmonic analysis was done. The simulation results shows that the developed eleven-level Cascaded H-bridge Multilevel inverter has many merits such as reduce number of switches, lower EMI, less harmonic distortion and the THD obtained is 11.15%. The study of this topology can also be extended to three phase induction motor and also to reduce the number of switches. It Is Further plan to hardware implementation.[8]

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