I J C T A, 9(6), 2016, pp. 2767-2775 ISSN: 0974-5572

A Novel VLSI Based Pipelined Radix-4 Single-Path Delay Commutator (R4SDC) FFT

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ABSTRACT

Fast Fourier Transform (FFT) is one of the important operations in field of digital signal, image processing and FFT. FFT processor is a critical block in all multicarrier systems used in the mobile environment. FFT is a systematic implementation of the Discrete Fourier Transform (DFT). In this paper, a novel high speed low complexity Radix-4 Single-path Delay Commutator (R4SDC) FFT processor has been proposed. The radix-4 Single-Path Delay Commutator (SDC) FFT architecture provides a higher throughput rate and low hardware complexity. The proposed architecture is based on Radix-4 algorithm. The design of high speed R4SDC FFT processor with pipelined architecture which is efficient in terms of latency, speed, utilization area, frequency, LUTs. The new Radix-4SDC pipelined FFT processor simplies its data flow and it is easy to control, and the complexity of the resulting hardware is lower than that of existing structures. The performance evaluation of proposed architecture has been determined through Very Large Scale Integration (VLSI) System design environment. High speed, less area hardware utilization, and low power consumption are the main parameters in VLSI design environment. In general, R4SDC FFT is to reduce the hardware utilization than R4SDF FFT. Proposed Novel R4SDC FFT structure offers 4.54% reduction in Slices, 8.78% reduction in LUTs, 40.83% reduction in delay and 18.18% reduction in power consumption than traditional R2SDF FFT structure.

Keywords: Fast Fourier Transform (FFT), Discrete Fourier Transform (DFT), Radix-4 Single-Path Delay Commutator (R4SDC), Radix-4 Single-path Delay Feedback (R4SDF), Very Large Scale Integration (VLSI) design.

1. INTRODUCTION

Fast Fourier Transform (FFT) has an important role in digital signal processing field, mainly in the advanced communication systems, such as Orthogonal Frequency Division Multiplexing (OFDM) and asymmetric digital subscriber line. All these system require that the FFT computation must be high throughput and low latency. In particular, the pipelined FFT architectures have been mainly adopted to address the difficulties due to their properties, such as small chip area, high throughput and low power consumption. Two types of pipelined FFT architectures are Delay Feedback (DF) and Delay Commutator (DC). According to the number of input data stream paths, they can be classified into Multiple-Path or Single-Path architectures.

Radix-4 Single Path Delay Commutator (R4SDC) architecture consists of Commutator, butterfly elements and complex multiplier with shift registers to provide delays. Radix-2 algorithm has the multiplicative complexity as radix4 and retaining the butterfly structure of radix2. R4SDC architecture has higher computational efficiency in addition. In R4SDC, improves the utilization of butterfly elements by modifying the butterfly elements. However, it increases the memory requirement.

Fortunately, the improved R4SDC architecture can produce the addition and the corresponding subtraction results of a butterfly operation in consecutive two cycles. The addition part is directly passed to another stage, while the subtraction part needs to execute complex multiplication before passing to the next stage. Therefore, the R4SDC architecture is ideal for our efficient pipelined radix-4 FFT architecture. In this

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paper, proposed Radix-4 Single Path Delay Commutator (R4SDC) FFT architecture is to reduce the two stages in a single stage. R4SDC is very efficient when compared to R4SDF. In R4SDC have a many number of paths to make a single stage. R4SDC provides high throughput rate and low hardware complexity.

2. RELATED WORK

A parallel structure for VLSI implementation of FFT processor has been explained in [Yongjun Peng, 2003]. In this paper, they propose an implementation method with high throughput for a single-chip 4096 complex point FFT. To increase the transformation speed, a parallel FFT architecture has been designed. The area and power efficient pipeline FFT algorithm has been explained in [Jung-yeol oh and Myoung-Seob Lim, 2005]. In this paper, the proposed radix-2^4 and the radix-4^2 algorithm and their pipeline FFT architecture has to reduce the area and power consumption of the multiplication. The proposed pipeline approaches have the characteristic that can replace one half of whole programmable multipliers with the novel Canonic Signed Digit (CSD) constant multipliers.

High performance VLSI FFT architecture has been described by [K.Babionitakis, et al. 2006].The hard real-time constraints at low silicon area and low power compared to CPU-based solutions. It reduces latency and memory requirements to one third compared to fully unfolded radix-4 architecture. VLSI design of radix with mixed FFT processor for MIMO OFDM in wireless communication has been explained in [N Kirubanandasarathy, et al. 2010]. In this paper present a pipelined Fast Fourier Transform (FFT) or Inverse Fast Fourier Transform (IFFT) processor for the applications in a OFDM based IEEE 802.11n Wireless Local Area Network baseband processor is presented. To achieve high throughput, reduction of memory, low power and complex multiplier reduction by using higher mixed radix FFT in MIMO-OFDM.

New parallel MDC FFT processor with efficient scheduling scheme has been described in [Moon Gi Kim, et al. 2014]. The proposed processor can provide a low hardware complexity and an efficient scheduling scheme, which is to reduce the number of complex multipliers from 8 to 6 without increasing delay and computation cycles. Low power and high throughput radix-4 FFT architecture has been explained in [Soumak Mookherjee, et al. 2014]. In this paper, architecture for 2546-point FFT processor is proposed which is suitable for both high performance and low area and power applications. The proposed architecture is based on radix-4 algorithm.

High speed FFT processor design using pipelined architecture has been explained in [Swapnil Badar and D.R. Dandekar, 2015]. The pipelined architecture of high speed FFT processor which is efficient in terms of latency, with using fastest processing element. Floating-point FFT of butterfly architectures based on multi-operand adders has been briefly explained in [Amir Kaivani and Seok-Bum Ko, 2015]. The proposed design consumes the lowest area. The butterfly architecture based on multi operand adders. As a future work, one could modify the proposed design to include a dual-path FP architecture which would be expected to have lower latency but at the cost of more area.

3. RADIX-2 FFT ARCHITECTURE

The Radix indicates the size of FFT decomposition. Radix is 2 which is single-radix FFT. For single radix FFTs, transform size must be select according to the power of radix. The Radix-2 decimation-in-time FFT (DIF-FFT) is applied to the two points N/2 DFT's. To calculate the number of butterfly stages required to compute N length, sequence can be M = log2N and N/2 butterfly operations are calculated to produce 32 point FFT. Discrete Fourier Transformation (DFT) has been designed for calculating the frequency representation of digital signals. In general, DFT of N-point discrete time signal is represented as follows,

$$X_k = \sum_{n=0}^{N-1} x_n W_N^{nk}, \; 0 \le k \le N-1 \tag{1}$$

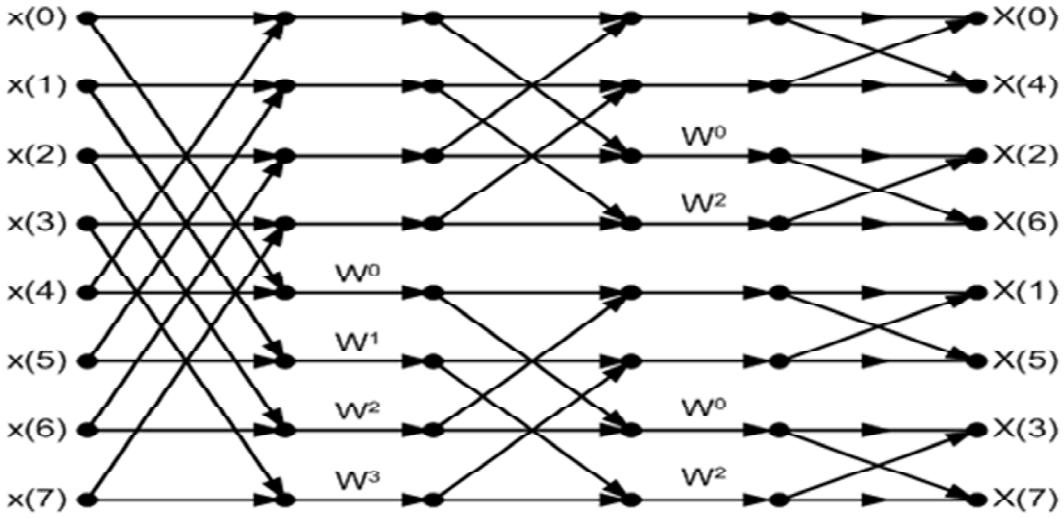

Figure 1: Signal Flow Graph (SFG) of 8point Radix-2 FFT

Where, X_k is the DFT (frequency) representation of discrete signal X_n. W_N^{nk} represents the twiddle factor and N represents the number of points. The average worst case performance of radix-2 DFT processor has been denoted as $O(n^2)$. In DIT-FFT the given input sequence is in shuffled order and the output sequence is in natural order. The Radix-2 decimation in time FFT is the basic form of Cooley-Turkey implementation algorithms.

Radix-2 FFT calculates the DFT of even index inputs and odd index inputs and then combines the two results to produce the entire DFT sequence. The basic block of FFT is butterfly structure, in which the two inputs are combined to give two outputs. The Signal Flow Graph (SFG) of 8-point Radix-2 FFT has been illustrated in fig. 1.

4. RADIX-4 FFT ALGORITHM

The radix-4 FFT is an advanced technique for performing Fourier transformation of input discrete signals. The radix-4 decimation in time and decimation in frequency fast Fourier transforms (FFTs) gain their speed by reusing the results of smaller, intermediate computations to compute multiple DFT frequency outputs.

The radix-4 FFT requires only 75% as many complex multiplies as the radix-2[9] FFTs, al uses the same number of complex addition and subtraction. These additional savings make it a widely-used FFT algorithm. Radix-4 decimation-in-frequency FFT can be equated similarly to the radix-2 DIF FFT, by separately calculating all four groups of every 4th output frequency sample. The DIF radix-4 FFT is a flow-graph reversal of the DIT radix-4 FFT, with the same operation twiddle factors and counts in the reversed order. The output ends up in digit-reversed order for an in-place DIF algorithm.

When compared to Radix-2 FFT, Radix-4 FFT takes advantages in following symmetries:

$$W_N^{nk+N/4} = -W_N^{nk+3N/4} = -jW_N^{nk} \tag{2}$$

This equation leads to a reduction of the number of multipliers. For 4 point radix-4 DIF FFT, four point output obtained as follows

$$X[4m] = \sum_{n=0}^{N/2-1} \left(x[n] + x[n+N/4] + x[n+N/2] + x[n+3N/4]\right) W_{N/4}^{mn}$$

$$X\left[4m+1\right]=\sum_{n=0}^{N/2-1}\left(x\left[n\right]-jx\left[n+N/4\right]-x\left[n+N/2\right]+jx\left[n+3N/4\right]\right)W_{N/4}^{mn}W_{N}^{n}$$

$$X\left[4m+2\right]=\sum_{n=0}^{N/2-1}\left(x\left[n\right]-x\left[n+N/4\right]+x\left[n+N/2\right]-x\left[n+3N/4\right]\right)W_{N/4}^{mn}W_{N}^{2n}$$

$$X\left[4m+3\right]=\sum_{n=0}^{N/2-1}\left(x\left[n\right]+jx\left[n+N/4\right]-x\left[n+N/2\right]-jx\left[n+3N/4\right]\right)W_{N/4}^{mn}W_{N}^{3n}$$

When $x[4m]$, $X[4m + 1]$, $X[4m + 3]$ are the Fourier transformation of input $X[n]$. The structure of 4 point Radix-4 FFT is illustrated in fig. 2.

Similarly, 16 point Radix-4 DIF FFT has two stages for performing FFT computation. It has only nine twiddle factor multiplication in first stage of FFT computation. The structure of 16 point Radix-4 FFT is illustrated in fig. 3.

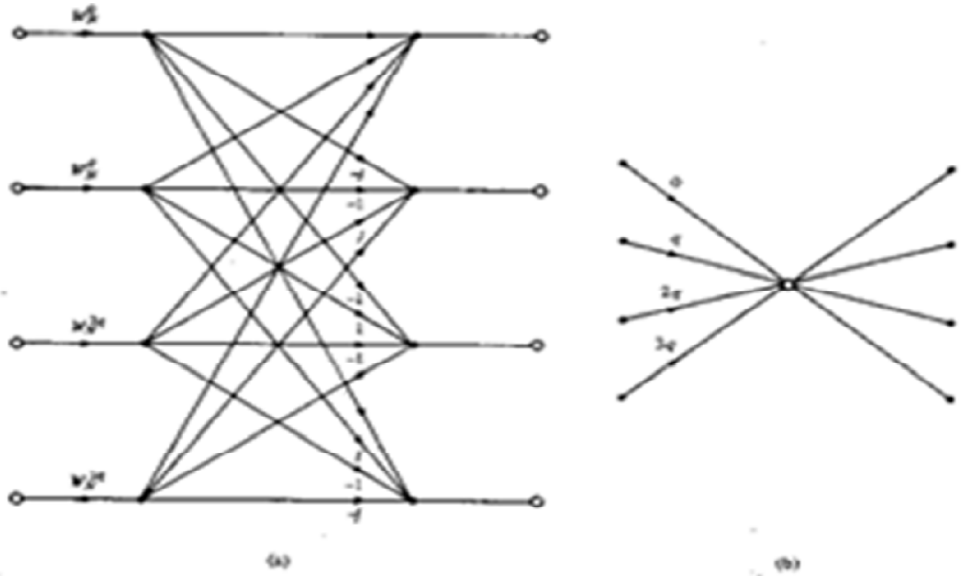

Figure 2: Structure of 4 point Radix-4 DIF FFT

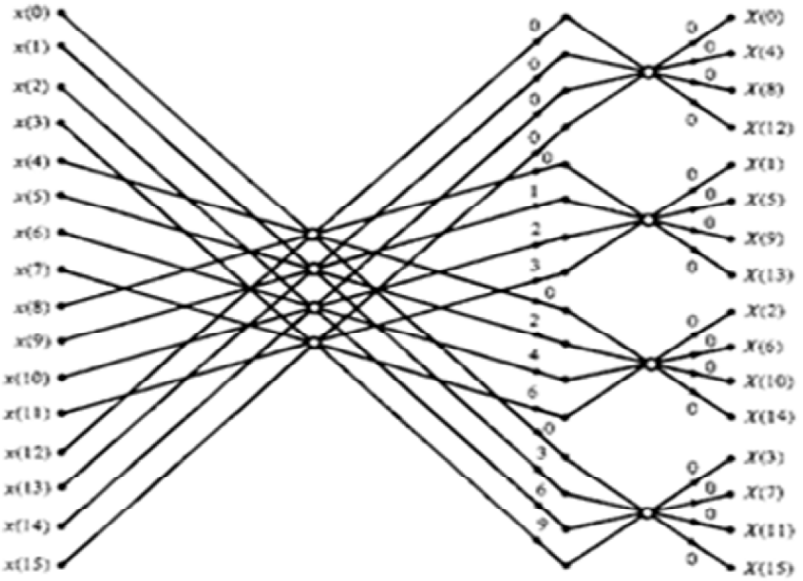

Figure 3: Structure of 16 point Radix-4 DIF FFT

5. RADIX-4 SINGLE-PATH DELAY FEEDBACK FFT ARCHITECTURE

Radix-4 Single-path delay feedback (R4SDF) FFT is a radix-4 version of R2SDF.R2SDF is an efficient architecture in terms of utilization of memory and multipliers increases from 50% to 75% at a cost of only 25%utilization of the butterfly element. The latency for each stage is 3N/4, 3N/16…. The memory requirement for this architecture is N-1. Radix-4 Single-path delay feedback uses the registers to store the one output of each butterfly in feedback shift registers.

Radix-4 single path delay feedback (R2SDF) FFT is a serial FFT processor which provides high speed operation. In R4SDF FFT, inputs are given into serial manner. Radix-4 Single path delay feedback FFT which is to increases the speed but it does not reduce the hardware utilization, power consumption and frequency. To overcome this problem, we proposed Radix-4 Single path delay Commutator. Each and every stage can be connected with Commutator instead of feedback, because it is very effective to reduce the area, delay, power consumption and increase the frequency. The structure of pipelined Radix-4 Single-path delay feedback (R4SDF) for 16-point FFT is illustrated in fig. 4.

6. PROPOSED RADIX 4 SINGLE PATH DELAY COMMUTATOR (R4SDF) FFT

In this paper, architecture of Radix-4 single-path delay Commutator (R4SDC) is preferred to reduce the hardware utilization, power consumption and to improve the speed of the processor.R4SDC improves the utilization of the butterfly elements by modifying the butterfly elements. However, this increases the requirement of memory. The number of words, which are necessary to be stored in 3N/2, 3N/8….. In the proposed technique, R4SDC architecture is presented for improving the architectural performances in terms of VLSI main concerns.

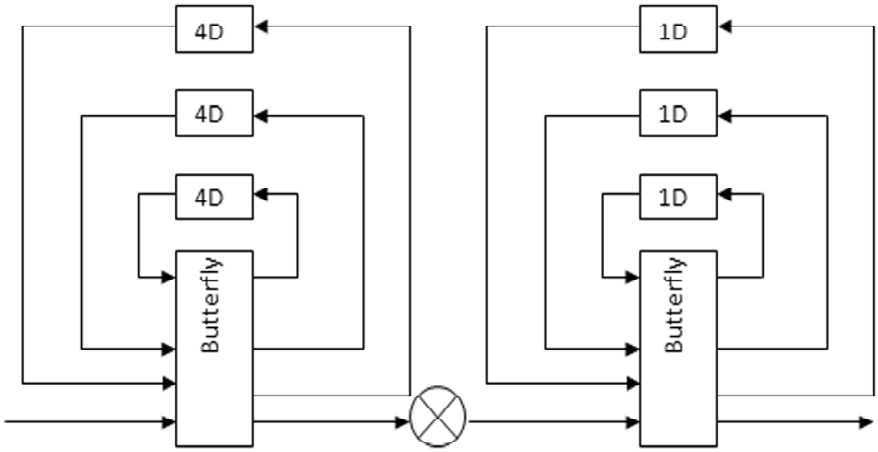

Figure 4: Pipelined Radix-4 single-path delay feedback (R4SDF) for 16 point FFT

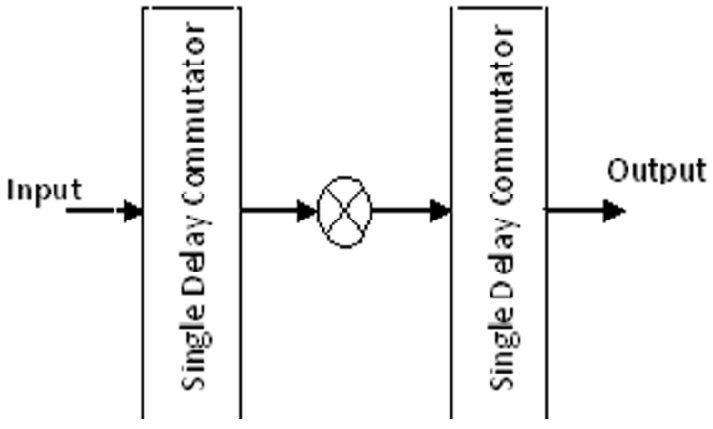

Figure 5: Architecture of proposed 16-point Radix-4 Single-path Delay Commutator

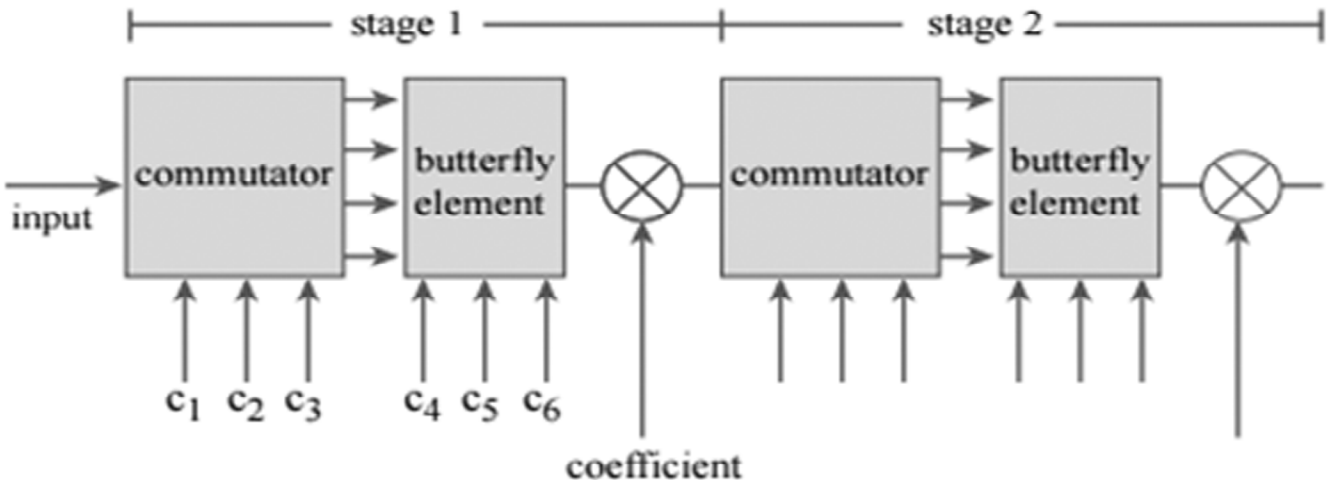

Figure 6: Internal structure of R4SDC

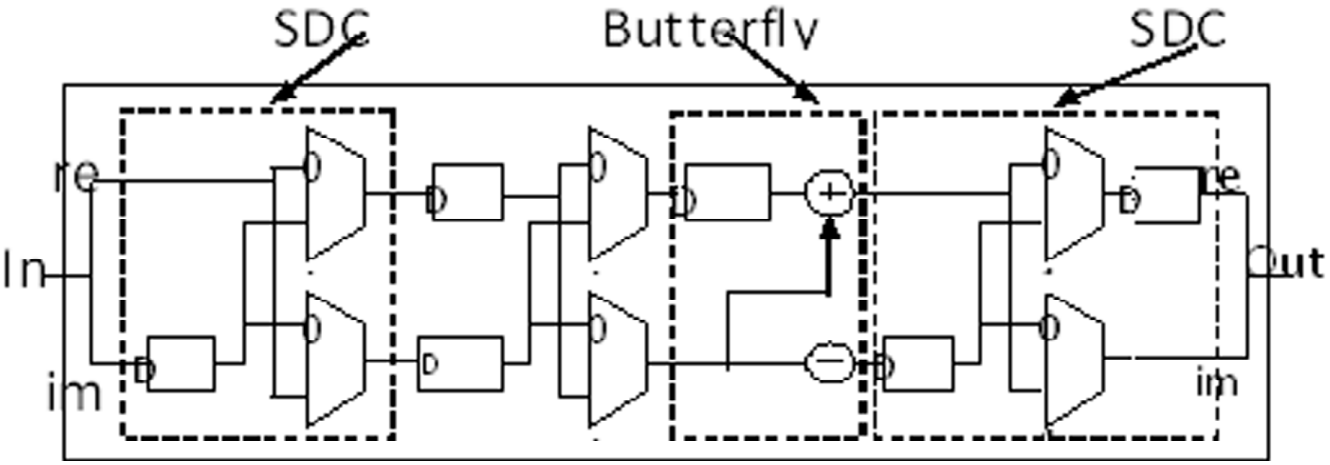

Figure 7: Data Flow of Single Path Delay Commutator

When compared to R4SDF structure, R4SDC architecture has less computational paths to perform FFT function. The R4SDC FFT architecture provides high throughput rate and low hardware complexity. The architecture of proposed 16-point Radix-4 Single-Path Delay Commutator FFT architecture is shown in fig. 5.

The internal structure of R4SDC has been illustrated in fig.6.The logic flow of single path delay Commutator has been illustrated in Fig.7.In Radix-4 single delay commutator architecture consists of processing elements, Commutator and delay. The operation of addition and subtraction has been done in processing element. The commutator, which is used to convert one form of signal to another form of signal. Twiddle factor, which is used to reduce the shifter and adder values. Multiplexer is used to control the signals.

7. RESULTS AND DISCUSSION

The design of Radix-4 Single-Path Delay Commutator (R4SDC) FFT architecture has been made by using Verilog Hardware Description Language (Verilog HDL). The simulation results has been evaluated by using ModelSim 6.3C and Synthesis performances are evaluated by using Xilinx 12.4i (Package: pq208, Family: Spartan-3, Device: Xc3s200) design tool. The simulation result of existing Radix-4 Single-Path Delay Feedback (R4SDF) FFT is illustrated in fig.8. Similarly, the simulation result of proposed Radix-4 Single-Path Delay Commutator (R4SDC) FFT is illustrated in fig. 9.

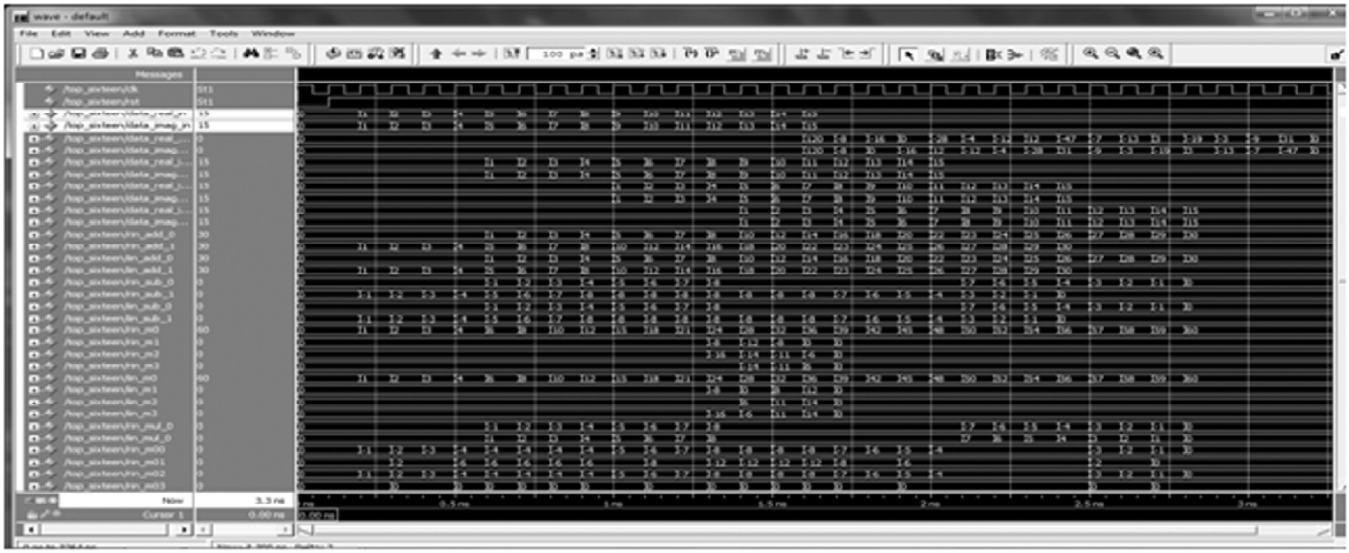

Figure 8: Simulation result of existing Radix-4 Single-Path Delay Feedback (R4SDF) FFT.

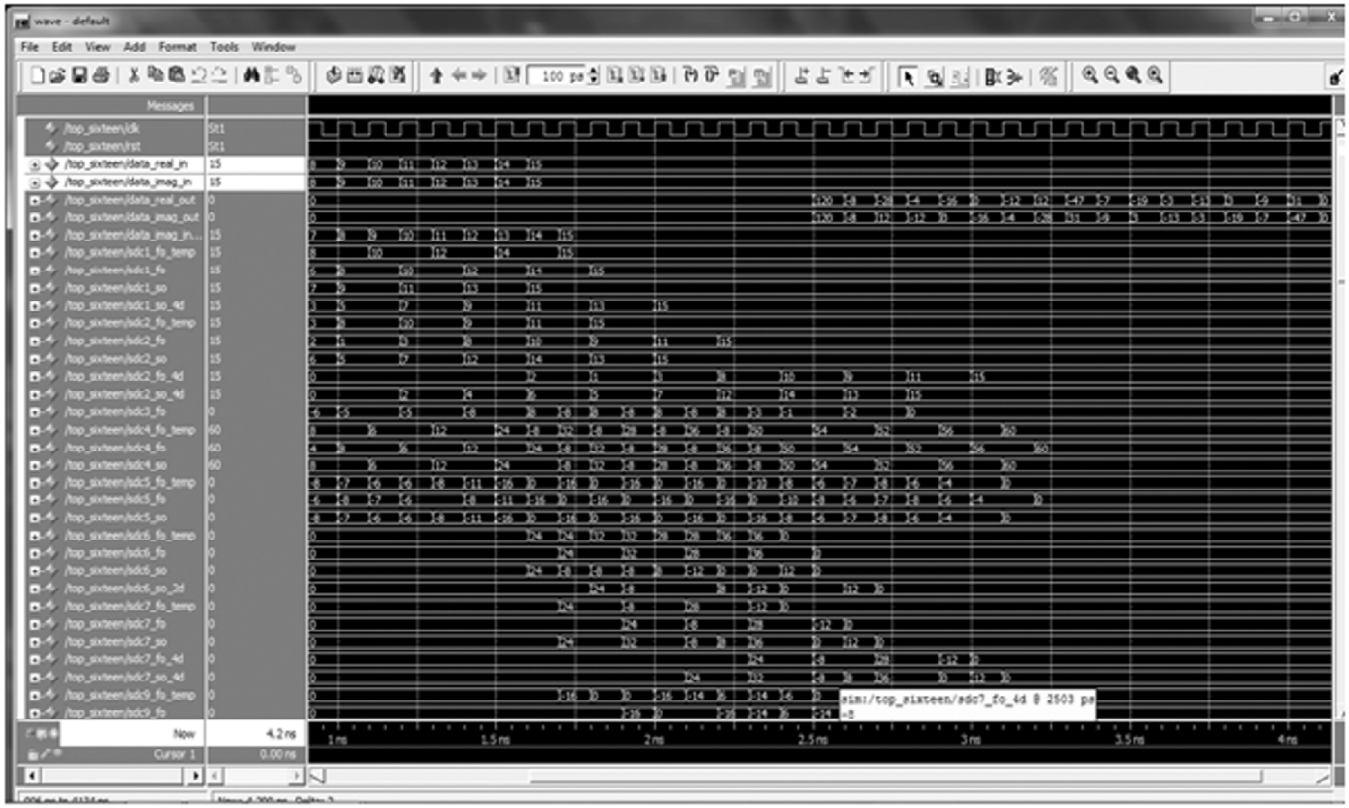

Figure 9: Simulation result of proposed Radix-4 Single-Path Delay Commutator (R4SDC) FFT

Table 1
Comparison of existing Radix-4 Single path delay feedback (R4SDF) and proposed Radix-4 Single path delay Commutator (R4SDC) FFT

Types/VLSI concerns	*Number of Occupied Slices*	*Total Number of LUTs*	*Delay (ns)*	*Power (mW)*
Existing R4SDF FFT	903	1640	23.295	957
Proposed R4SDCFFT	862	1496	13.782	783
Percentage Reduction	4.54%	8.78%	40.83%	18.18%

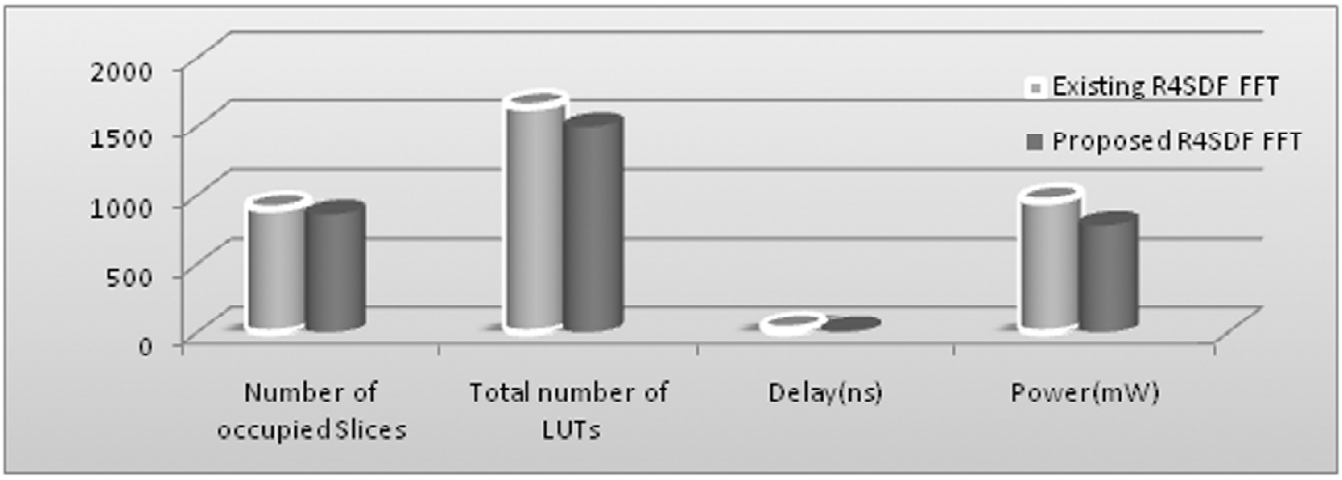

Figure 10: Performance evaluation of both existing R4SDF and proposed R4SDC FFT

When compared to R4SDF, the R4SDC has been improved in terms of less silicon area utilization and power consumption. The performance evaluation of existing R4SDF and proposed R4SDC are analyzed and compared in table 1. From table 1, it is clear that proposed Radix-4 Single-Path Delay Commutator (R4SDC) FFT offers 4.54% reduction in hardware slices, 8.78% reduction in number of LUTs, 40.83% reduction in delay and 18.18% reduction in power consumption than existing R4SDF FFT. Performance evaluation of both existing R4SDF and proposed R4SDC FFT as shown in Fig.10.when compared to existing Radix-4 single path delay Feedback(R4SDF) FFT, Radix-4 Single path delay Commutator provides better performance.

8. CONCLUSION

In this paper, the new architecture "Radix-4 Single-Path Delay Commutator (R4SDC) FFT" has been designed through Very Large Scale Integration (VLSI) system design environment. The aim of this research work is to reduce the hardware utilization and power consumption of FFT processor and also increasing the throughput rate, low hardware complexity. Proposed R4SDC provides better performance than the existing R4SDF FFT structure. Proposed pipelined R4SDC FFT offers 4.54% of reduction in hardware slices, 8.78% of reduction in number of LUTs, 40.83% of reduction in latency and 18.18% of reduction in power consumption than existing R4SDF FFT. In future, the proposed architecture will be absolutely useful in OFDM based digital communication to perform the function of frequency transformation and to analyze the spectrum characteristics of digital inputs.

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