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Enhanced 1.2-V Flash ADC with integrated Low power Sub threshold CMOS Voltage Reference methodology

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ABSTRACT

The objective of the work is to design low power CMOS logic for a flash type ADC, typically 4-bit. The modeled ADC is driven with the proposed subthreshold CMOS voltage reference circuit to meet the objective of low power design by replacing conventional voltage reference with low voltage comparator, charge pump circuit, and a digital control unit. This proposed reference voltage design works at 274.51mV reference voltage at 374.39mVsupply voltage and achieves 27% reduction in power consumption. The analysis was done in cadence virtuoso environment and stimulated using spectre simulator under 90nm technology. The results for the proposed ADC design shows that the power dissipation is7mW approximately for a four-bit, that constitute to 27% savings. The technique extended for higher ADC bitsthen percentage of savings would be high. The proposed design operates at 6MHz with supply of 1.2v,conversion time of 6.182ns and occupies an area of 1202.2um.

Keywords: Voltage Reference, Control circuit, Subthreshold Encoder, Low voltage Comparator

1. INTRODUCTION

The linkage between analog and digitals worlds can be implemented by using ADC (Analog to Digital Converter). It is used to produce digital output D as a function of analog input A as follows D=f (A). It can be designed by producing a set of reference voltages by using a reference voltage generator and comparing it with the provided analog input and selecting the input voltage which is closest to the reference voltage. Generally most of the ADC's prefer analog input as a voltage quantity because comparing, routing and storing operations are easier for voltages as compared to currents. In present scenario, as there is a lot of demand for low power design circuits in VLSI circuits, different enhanced low power voltage reference circuits had been implemented and integrated with ADC to create a reference voltage which can be used for comparing with provided analog input voltage.

Voltage reference circuits are having two most important criteria as Low voltage and Low power operation .A parasitic vertical bipolar junction transistor is generally used in designing voltage reference circuits for CMOS technology. Filanovsky and Allam studied MOSFET temperature deportment pointing out that below a certain technology dependent partialness point, the gate-source voltage of a MOSFET, inequitable with a fine-tuned drain current, decreases with temperature in a quasilinear fashion [1]. Starting from this observation, a gate to source voltage can be used in instead of a base-emitter voltage to design a voltage reference independent of temperature. The Bandgap Voltage Reference (BVR) circuits are commonly used owing to their high precision. These have been implemented in standard CMOS technologies exploiting parasitic vertical Bipolar Junction Transistors (BJT). Several BVR circuits are implemented in submicron BICMOS technology [2]. This circuit operates with a supply voltage of 1 V. Later several low voltage low

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power Voltage Reference (VR) predicated on incipient circuit topology and on subthreshold MOSFETS. It exploits the fact that the gate source voltage of MOSFET, after biasing with constant drain current decreases linearly with temperature [3]. Several techniques for sub 1-V operation has been proposed to reduce the supply voltage [4].

The other techniques are implemented by superseding the p-n junction circuit with the diode-connected NMOS transistors partial in the subthreshold region [5]. This paper proses a proposed voltage reference design which is based on conventional design .When this circuit is integrated with Flash ADC the required low voltage operation is obtained.

2. CONVENTIONALVOLTAGE REFERENCE DESIGN METHODOGY

This conventional CMOS voltage reference circuit shown in Fig. 1 where the diode connected NMOS transistors M1 and M2 in the subthreshold region replace the BJTs in the traditional bandgap reference circuits.

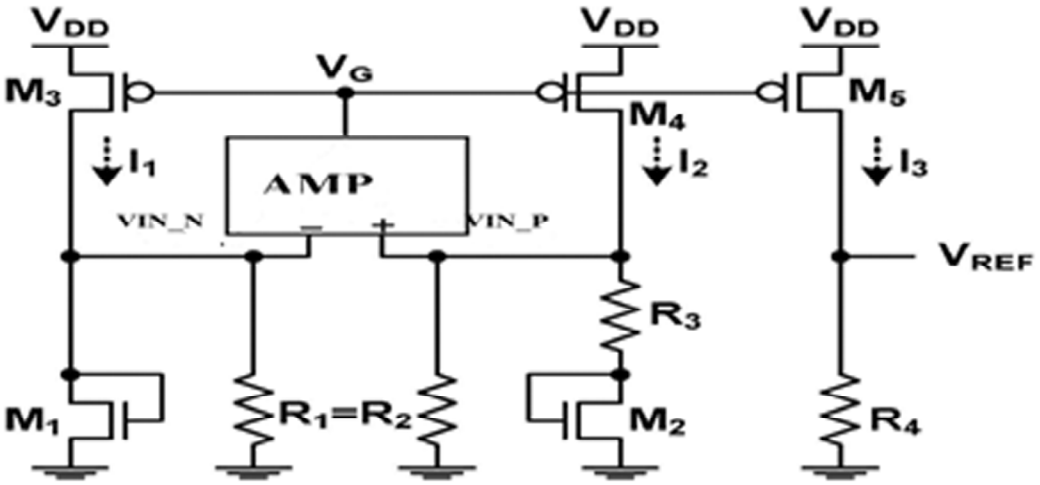

Figure 1: Conventional CMOS voltage reference Design

2.1. MOSFET in subthreshold region operation

The behavior of MOS transistor in subthreshold region when channel is weakly inveted is explained as

In sub threshold region when $V_{gs} < V_{th}$,

Where V_{gs} is the supplied Gate to Source voltage of MOSFET and V_{th} is corresponding threshold. In weak inversion source is tied to bulk and current is varied exponentially as given below:

$$I_D = I_{D0} e^{\frac{V_{gs} - V_{th}}{V_t}} \tag{1}$$

Where I_{D0} is current at $V_{gs} = V_{th}$, and $V_T = \frac{KT}{q}$ and $= a + \frac{c_D}{c_{OX}}$ C_D is capacitance of the depletion layer, c_{OX} is capacitance of the oxide layer

Equation (1) is used to derive the sub threshold current of MOSFET.

2.2. Circuit operation

Due to resistors R_1 and R_2 are equal, produced currents I_1, I_2 and I_3 are equal to $\left(nU_T \ln(N) + \frac{R_3}{R_1} V_{GS1} \right)$.

So the output reference voltage is defined as follows

$$V_{REF} = \frac{R_4}{R_3}\left(nU_T \ln(N) + \frac{R_3}{R_1} V_{GS1} \right) \quad (4)$$

Output reference voltage V_{REF} is controlled by choosing the R 4 value.

The simulation result of conventional voltage reference is shown in Fig. 2.

3. PROPOSED VOLTAGE REFRENCE DESIGN METHDOLOGY

This circuit is implemented based on the conventional design as shown in Fig. 3. It has been implemented by replacing the analog amlifier in the conventional design by a low voltage comparator and a charge pump circuit and control unit circuit.

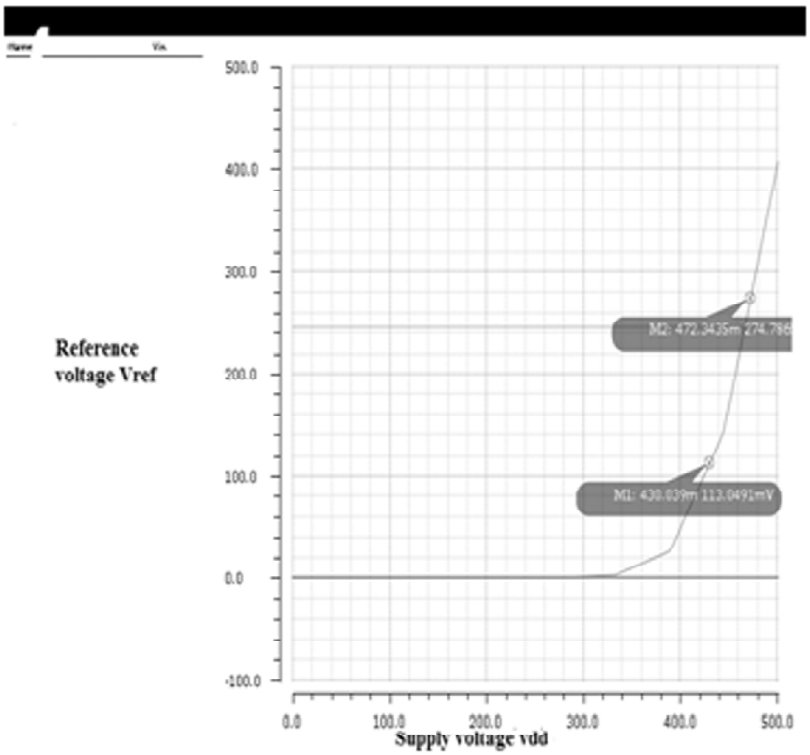

Figure 2: Variation of supply voltage vs Reference voltage in conventional design

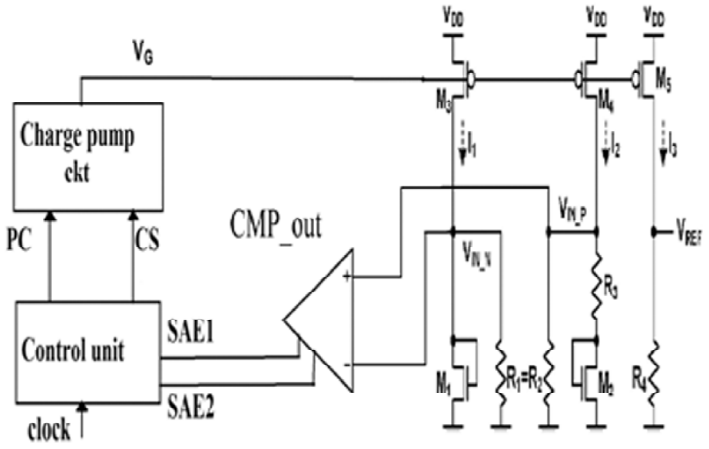

Figure 3: Proposed voltage reference circuit design

3.1. Design of Control unit

The following Cintrol signals are generated by the control circuit shown in Fig. 4.

1) SAE1 (Sense Amplifier Enable 1)
2) SAE2 (Sense Amplifier Enable 2)
3) CS (Charge Sharing)
4) PC (Pre Charge)

3.2. Design Low voltage comparator

The proposed Low voltage comparator as shown in Fig. 5 is used to detect the voltage difference between the two provided inputs $V_{IN\,N}$ and $V_{IN\,P}$. And it is going to add an auxiliary amplifier to the conventional sense amplifier type comparator. Sensing speed will be enhanced by using auxilary amplifier.

For some kind of cases like when two input voltages (i.e. $V_{IN\,N}$ *and* $V_{IN\,P}$) are low and the input voltage difference ($\Delta V_{IN} = V_{IN\,N} - V_{IN\,P}$) is small the comparator operates very slowly if it not provided by auxiliary amplifier. When V_{IN} is low, the current difference between M_1 and M_2 becomes small; hence, the voltage difference on nodes V_1 and V_2 ($\Delta V_{1,2} = V_1 - V_2$) increases very slowly. Due to the pull-down current of the cross-coupled latch is limited to the drain currents of M_3 and M_6 (i.e., I_{D1} and I_{D2}), the voltage amplification on the corresponding nodes V_1 and V_2 by the cross-coupled latch ($M_3 - M_6$) is very slow. Then, the drain currents significantly decrease proportional to VIN. In addition to that The comparator without the auxiliary amplifier does not operate at very low input voltage where the pull-down current of the cross-coupled latch is very weak. Moreover Nodes V_1 or V_2 are going to pull down during the second amplifying operation byThe auxiliary amplifier ($M_7 - M_8$).

3.3. Design of Charge Pump circuit:

The proposed charge pump circuit as shown Fig. 6. According to the comparator output value (CMP_out) adjusts the gate voltage of the transistors.

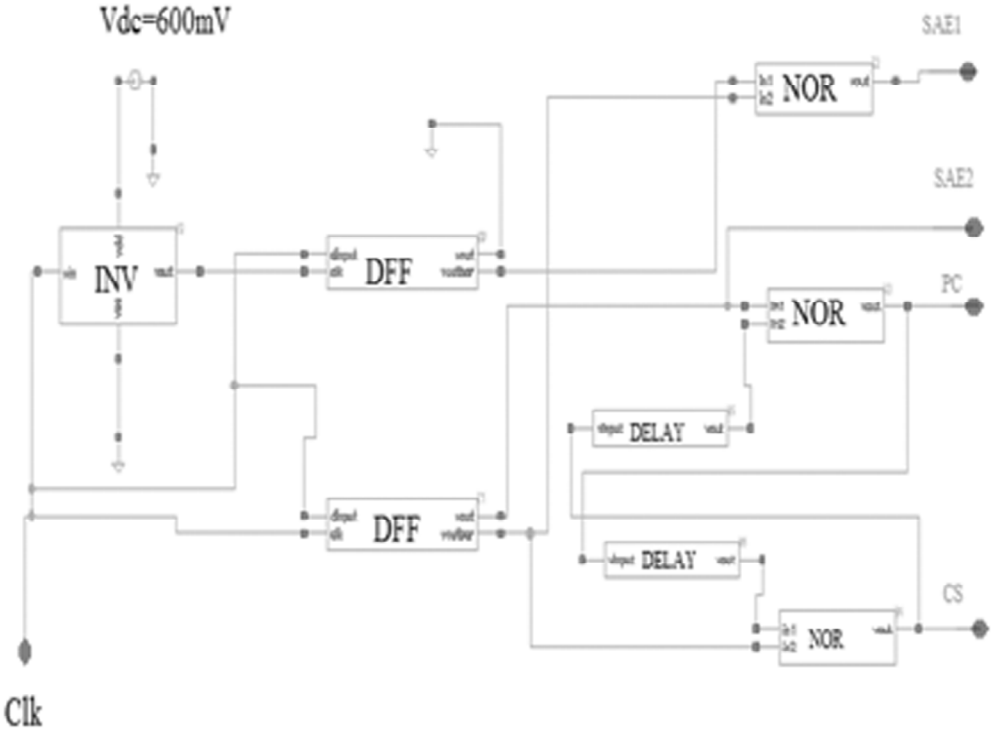

Figure 4: Digital control unit

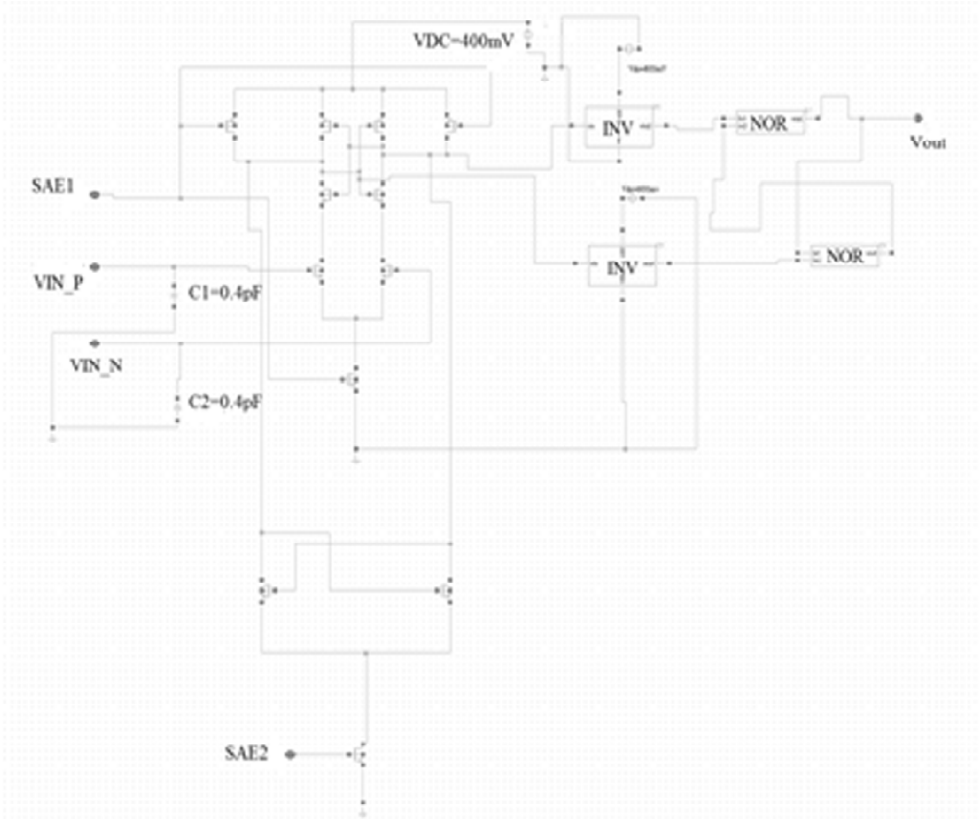

Figure 5: Low voltage comparator schematic

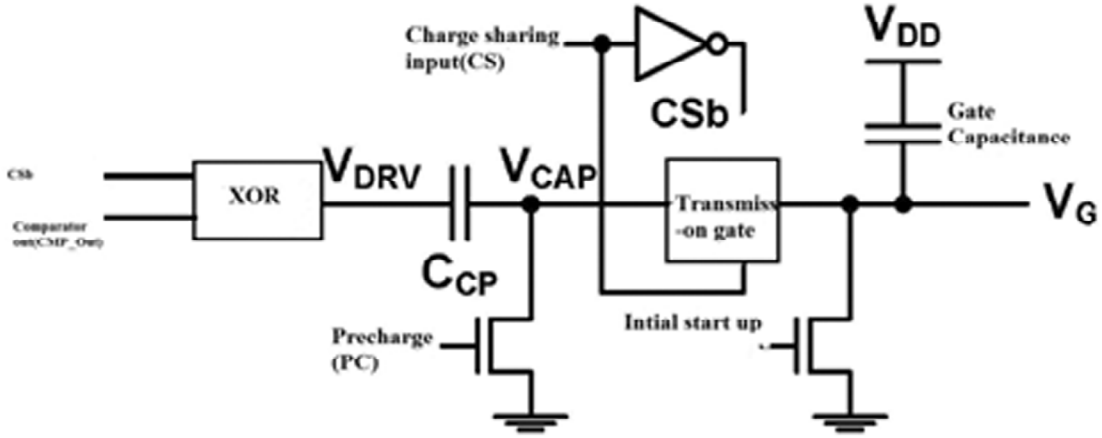

Figure 6: Charge pump circuit

Initially, V_G is discharged to the ground by a startup signal. Then corresponding currents I_1, I_2, and I_3, will be generated by Transistors M_3, M_4, and M_5 as shown in Fig. 7 respectively. Two input voltages of the comparator (i.e., $V_{IN\,N}$ and $V_{IN\,P}$) increase to near V_{DD}. At the time where start-up operation ends, for every clock cyclethe charge-pump circuit changes slightly. At the precharge (PC) phase, the PC signal is going to connect V_{CAP} to ground and according to the comparator output value node V_{DRV} is connected to the ground or V_{DD}. At charging phase by the CS signal node V_{CAP} is connected to node V_G and V_{DRV} changes from the ground to V_{DD} or from V_{DD} to the ground. And Output reference voltage V_{REF} is controlled by V_G.

Fig. 7 shows the schematic of the proposed volage reference and the simulation result is shown in Fig 8 and Fig. 9. The proposed voltage refere is given by 600mV clock pulse and it is going to generate required control signals for producing the reference voltage. This proposed method produces 274 mV reference voltage at 374 mV and it requires 250mV minimum supply voltage.

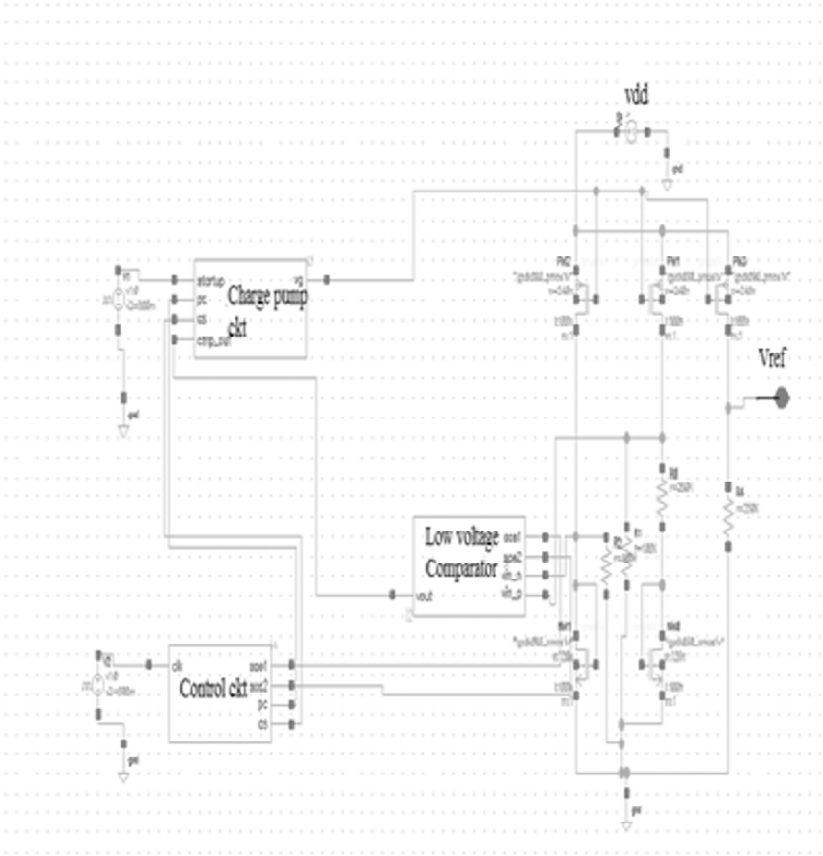

Figure 7: Proposed Voltage Reference Design

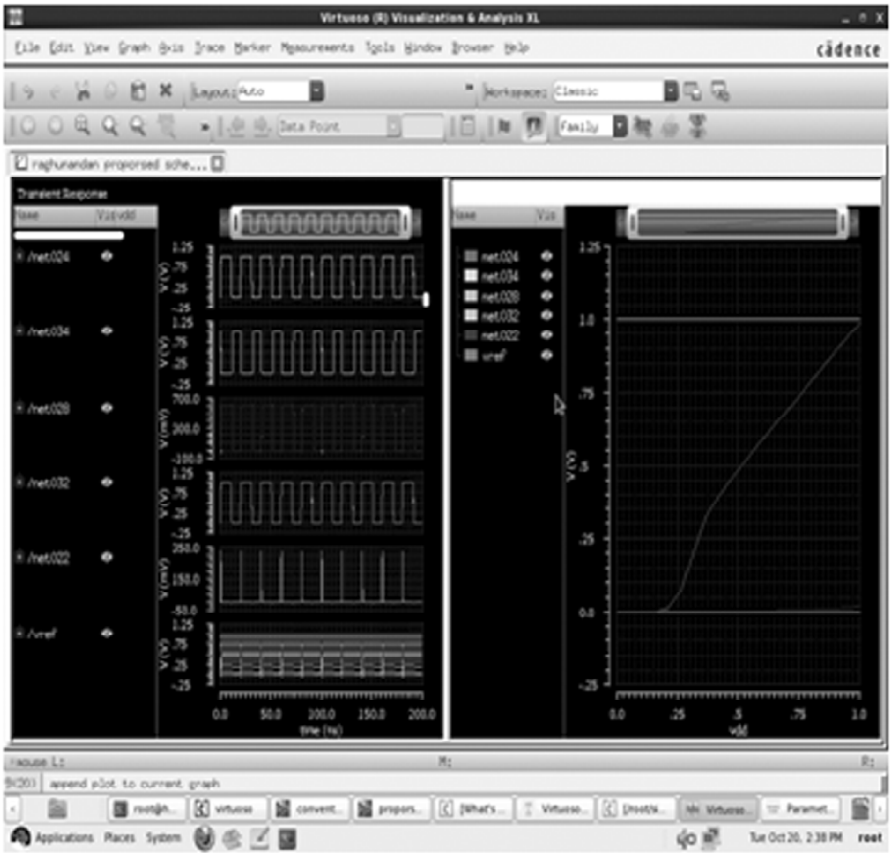

Figure 8: Transient response of proposed voltage reference

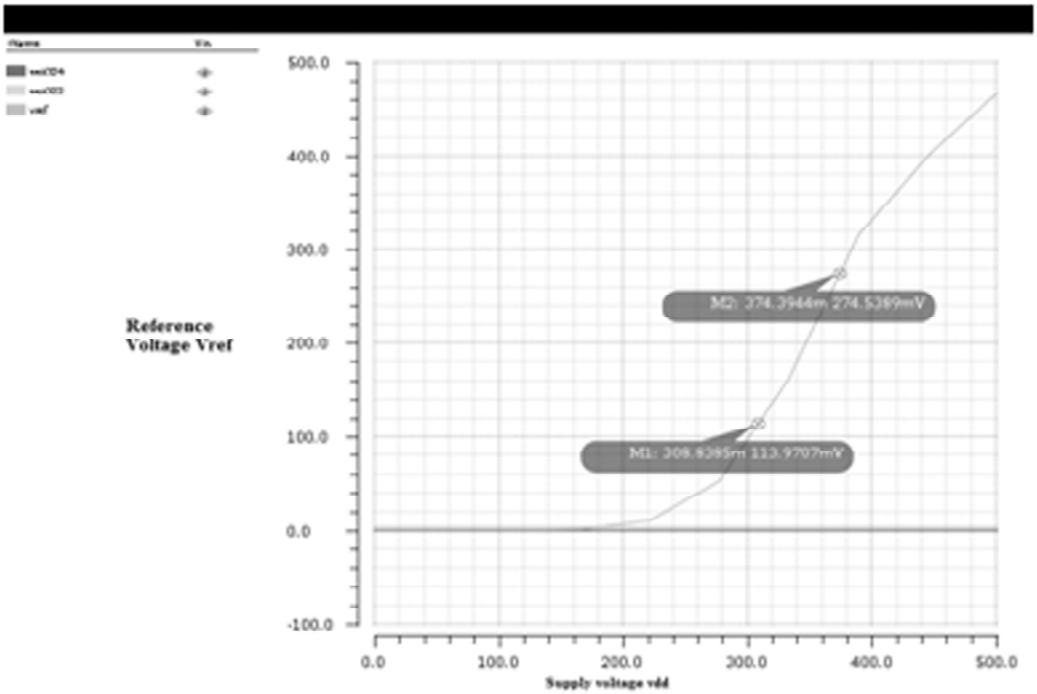

Figure 9: Variation of supply voltage vs reference voltagE

Table 1
Parameters For the Conventional and Proposed Low voltage References

Parameter	*Conventional Design*	*Proposed Design*
Process (nm)	90	90
Power (μw)	7.33	5.35
V_{DD}	472	374
V_{REF}	274	274

4. DESIGNING FLASH ADC

Flash ADCs (Known as parallel ADCs) uses large numbers of comparators and are fastest. The input signal is applied at once to all the comparators ,one comparator delay from the input appears in thermometer oupput , and the encoder N-bit output by only a few gate delays on top of that, so the process is very fast. An N-bit flash ADC consists of 2^N resistors and 2^N–1 comparators as in Figure Fig. 1. Each comparator was provided by a reference voltage. A comparison is performed between a given input voltage and reference voltage of all the comparators. If input voltage is greater than reference voltage it is going to produce "Logic 1" otherwise as "Logic 0".

4.1. Designing of Comparator

The low power comparator circuit used in the design of Flash ADC is shown in Fig. 12. This circuit uses a preamplifier and a positive feedback stage. To produce an acceptable gain the input differential pair uses NMOS transistors in the preamplification stage and the load uses PMOS transistors. Whether the input singal is larger or smaller will be decided by positive feedback stage.This information is amplified by output buffer stage and provides digital output. Schematic low voltage comparator is shown in Fig. 11.

4.2. Priority Encoder design

In this design to convert from thermometer code to binary code a priority encoder is used as shown in Fig. 12.For better accuracy multiplexers are designed by using transmission gates.

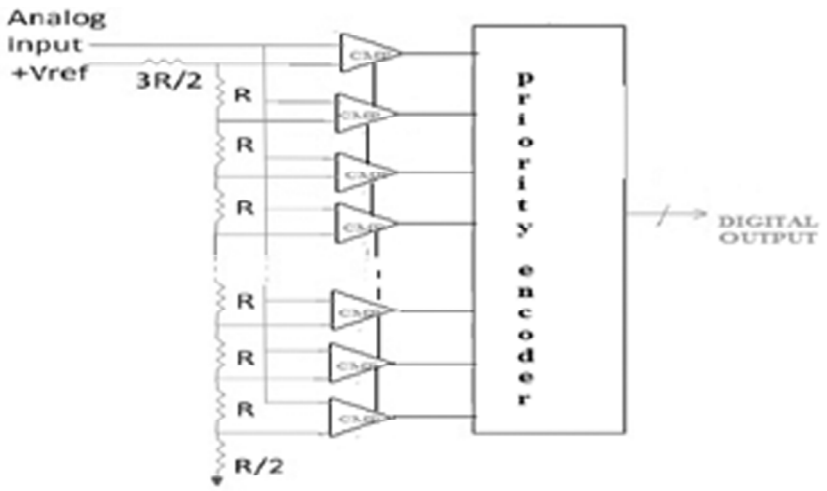

Figure 10: N-bit Flash ADC

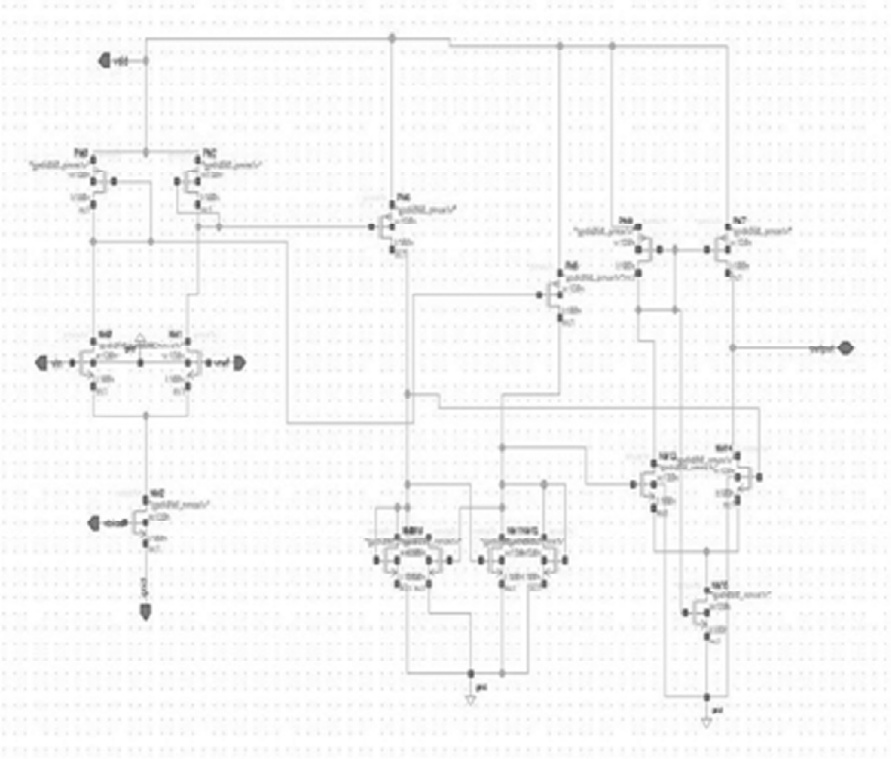

Figure 11: Schematic of Comparator

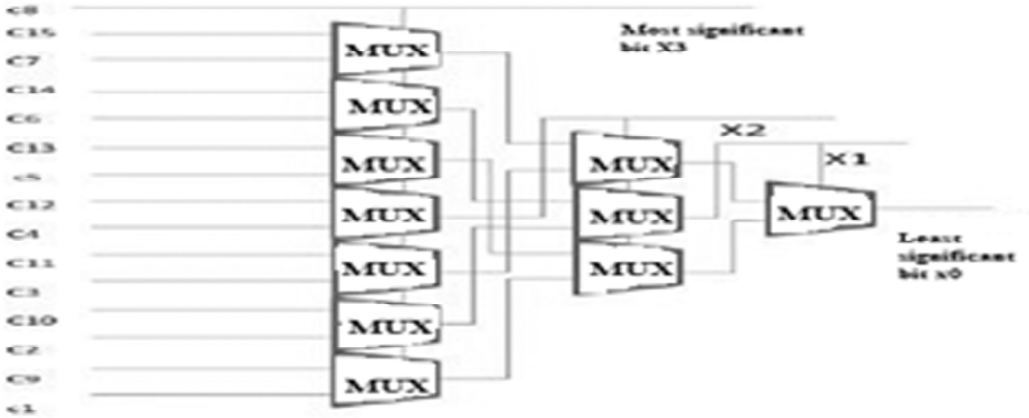

Figure 12: Design of Priority Encoder

The schematic of 4 bit Flash ADC is designed in 90nm CMOS technology by using Cadence virtuoso and it is integrated with the proposed reference voltage design. The simulation result of 4 bit Flash ADC is shown in Fig. 13 and Fig. 14 and Fig. 15.

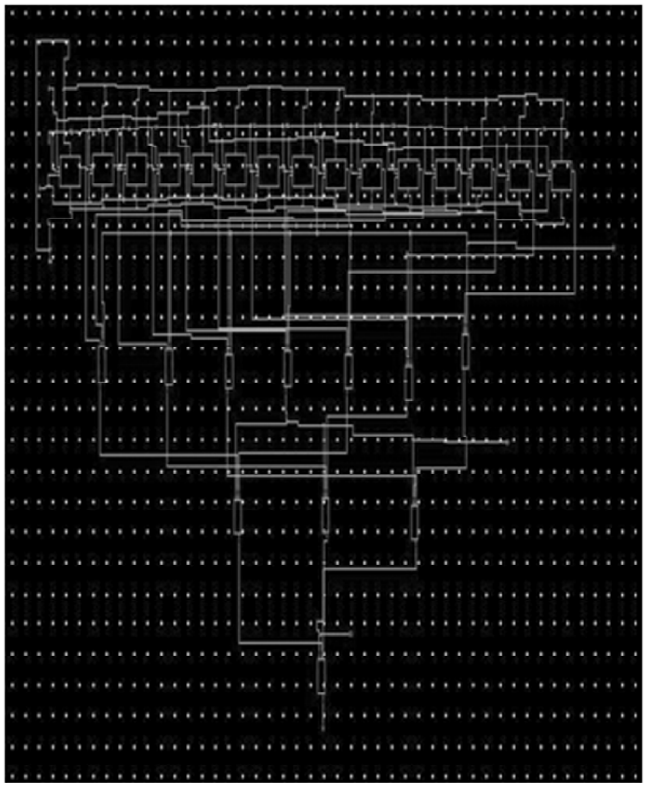

Figure 13: schematic of 4 bit Flash ADC

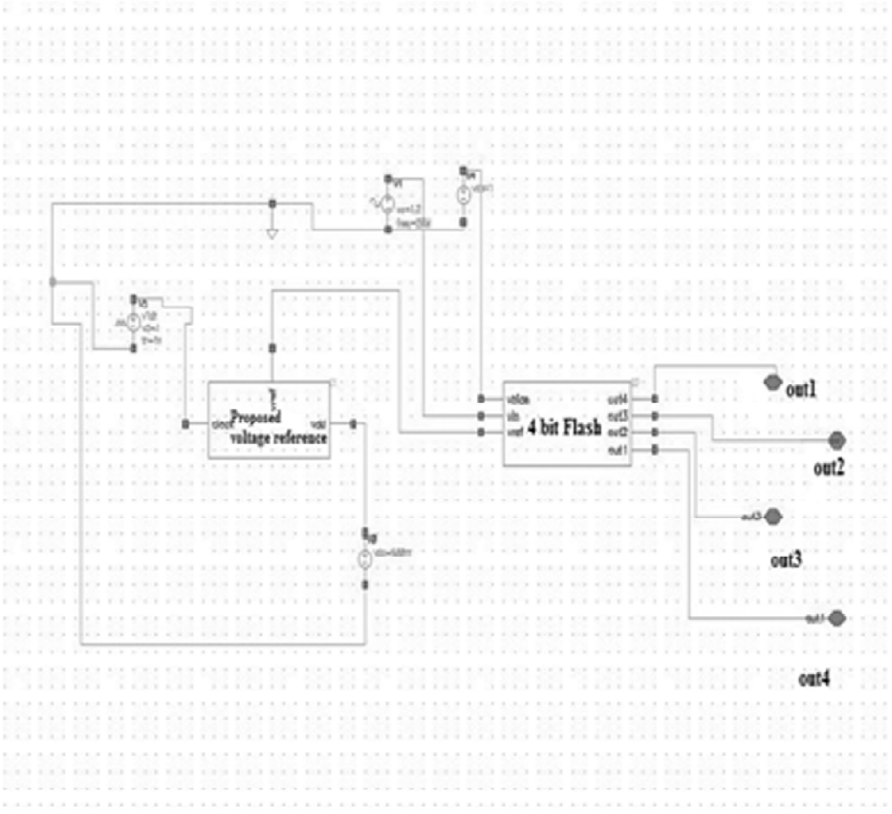

Figure 14: symbol of 4 bit Flash ADC

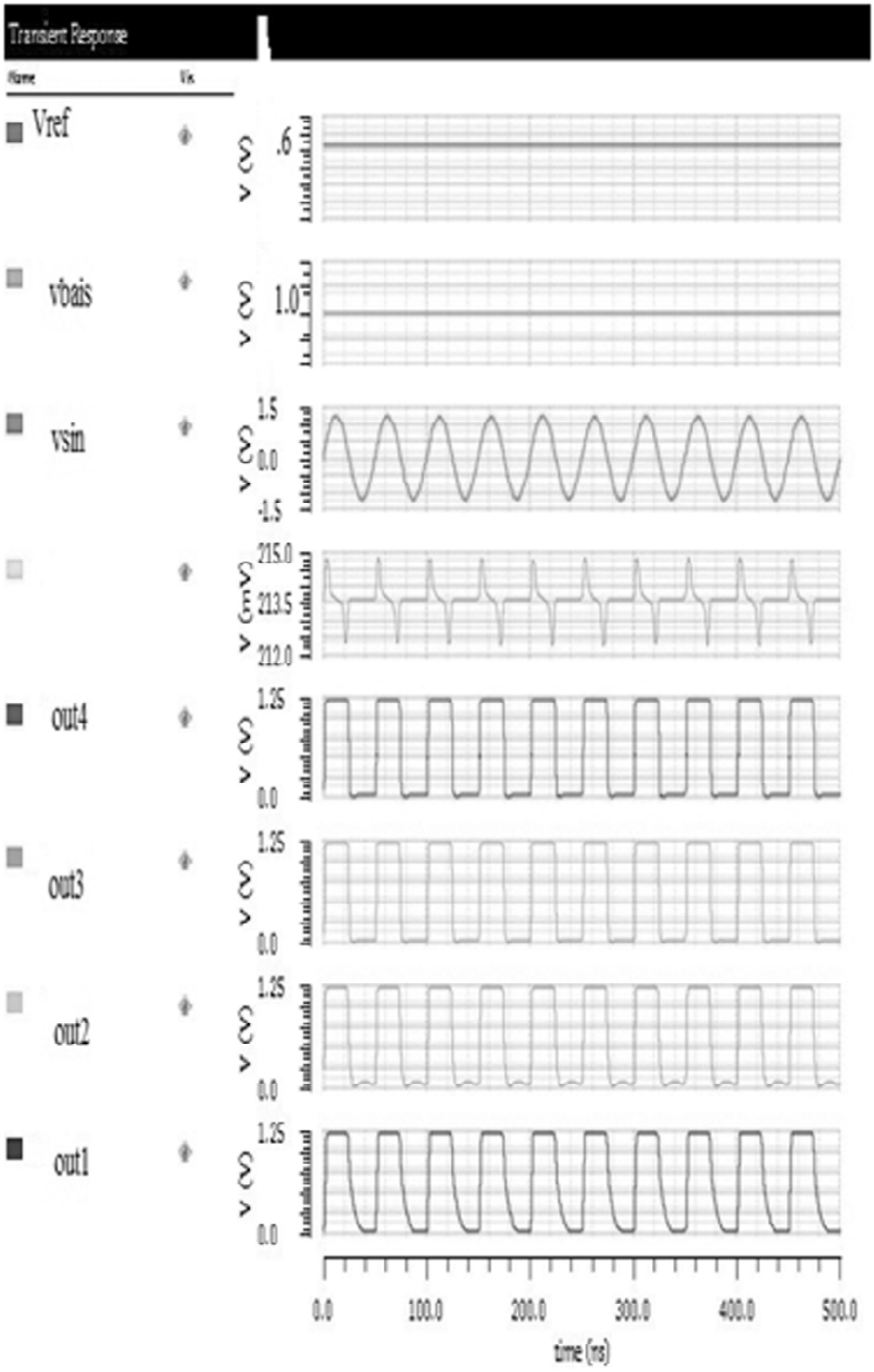

Figure 15: Simulation result of 4 bit Flash ADC

Fig. 16 is used to depict the layout daigram of 4 bit Flash ADC.

Table 2
Parameter Values of 4 BIT Flash ADC in 90 NM

Resolution	*Frequency*	*Power dissipation*	*Conversiontime*	*area*
4 bit	6 Mhz	6.943mW	6.182 nS	1202.2uM

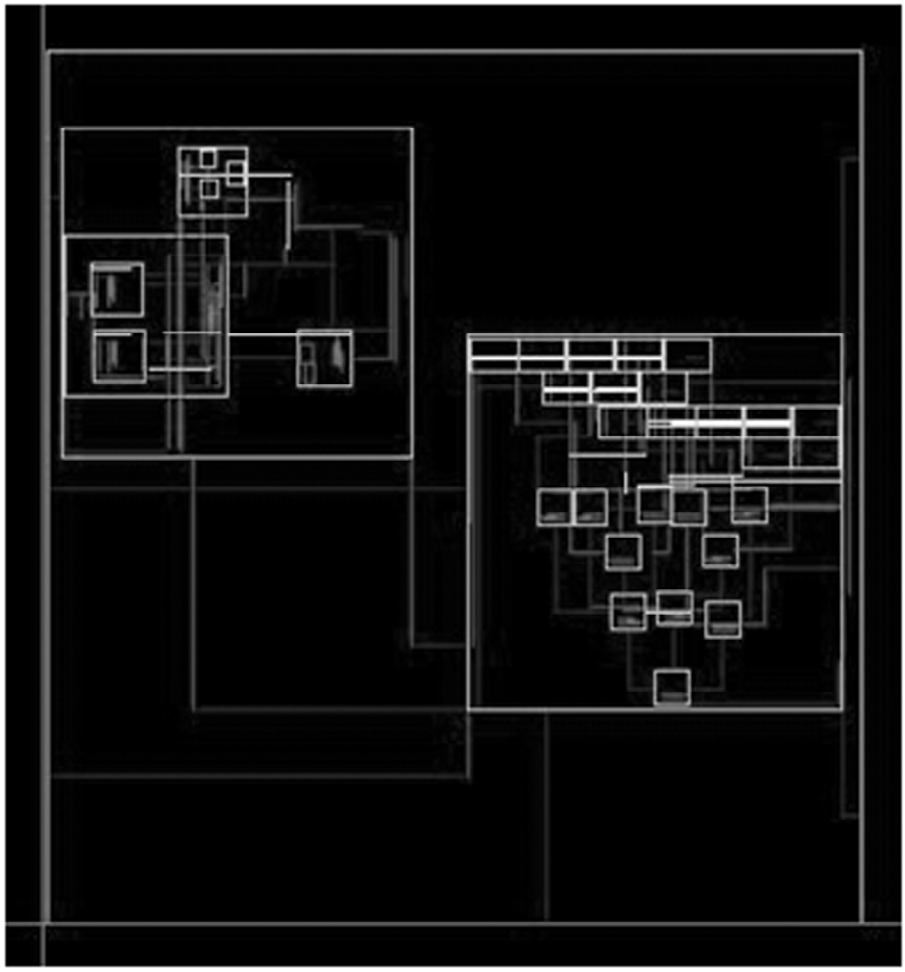

Figure 16: Layout diagram of 4 bit Flash ADC

CONCLUSION

The disadvantage associated with Flash ADC is high power dissipation due to implementing it by large no of comparators. In this regard a low power 4 bit Flash ADC is has been designed by implementing it with the subthreshold CMOS voltage referece design. The design and simulation are carried out in 90nm CMOS technology by using Cadence virtuoso. This ADC is integrated with the proposed reference voltage circuit, which requires 20% less supply voltage and consumes 27% less power as shown in Table.1.From Table.2 it can be concluded tis 4 bit Flash ADC can be used in low power and high speed applications.

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