Design of Low Power Code Converter using Energy Recovery Logic

Dinesh Kumar[1] and Manoj Kumar[2]

[1] University School of Information, Communication & Technology GGSIPU, Delhi, India, Email: dinesh4saini@gmail.com
[2] University School of Information, Communication & Technology GGSIPU, Delhi, India, Email: manojtaleja@ipu.ac.in

Abstract: In this paper, a new design of code converters have been presented using two phase adiabatic static CMOS logic (2PASCL). Energy recovery techniques are becoming a prominent solution of power reduction problem which comes due to scaling limits in integrated circuits. In this paper the proposed design of binary to gray converter shows the power delay product (PDP) of 290.6156×10^{-9}fJ as compared to 653.9846×10^{-9}fJ of conventional design. The proposed gray to binary converter shows the PDP of 237.2683×10^{-9}fJ as compared to 499.1218×10^{-9}fJ of conventional design. The performance of the proposed design has been evaluated with temperature variation and design shows improvement in the performance. In proposed design transistor count is also less than as compared existing designs reported in the literature.

Keywords: Adiabatic Logic, Code Converter, Energy recovery, Power Delay Product, Transmission Gates

1. INTRODUCTION

Low power portable electronic devices are reining today's world magnificently. The backbone of portable electronic devices is very large scale integrated circuits (VLSICs). With the introduction of integrated circuits by Jack Kilby and Robert Noyce in 1958, the amelioration in ICs has been accomplished by improving the scaling of metal oxide semiconductor field effect transistors (MOSFETS) [1]. According to Moore's law, the number of devices on chip of the same area will be doubled with in a period of 18 months. This increasing density of devices reduces the overall size with increased performance and portability of the electronics systems. However, the increased in device density results in increased power density which elevates the dissipated heat of the systems. Cooling mechanism for sinking this heat requires more power and this whole mechanism drained the battery energy at a faster rate. Therefore low power dissipation to prolong the battery life becomes a prime concern for portable devices. Power dissipation in a complementary MOSFET takes place in three components: dynamic power dissipation, short circuit power dissipation, and leakage power dissipation [2]. As the feature size of the device reduces the increase in leakage power dissipation becomes constraints for devices [3]. Other practical limitations of downscaling such as electro-migration, lithographical issues, material as well as technological issues have been discussed in [4-6]. Therefore the saturation of technology due to practical and technological constraints needs a paradigm shift towards new techniques of energy recovering or harvesting. Adiabatic logic is such a prominent technique of power reduction without downscaling further. It is an energy

recovery technique in which the stored energy at capacitive nodes recycled back to the power supply [7]. There are different adiabatic logic techniques like TSPC, 2N-2N2D, 2N- 2N2P reported in [8-12]. A FinSAL and Graphene based adiabatic logic has been discussed in [13, 14]. A 2 phase adiabatic static CMOS logic (2PASCL) has been discussed in [15]. In this paper a 2PASCL based, transmission gate X-OR [16] gate has been used for proposed circuit.

Modern communication systems, digital signal processors, portable electronic devices such as laptops, cell phones, implantable medical devices, and modern warfare equipments consist of digital logic circuits. The working of these logic circuits is based on codes such as binary, octal, hexadecimal, and gray codes. Binary and gray codes have extensive applications in digital circuits such as position encoder, genetic algorithms, Karnough maps, and in various communications systems. There are various applications which require the conversion of codes like binary to gray and gray to binary. In this paper, 4 bit binary to gray (B-G) and gray to binary (G-B) conversion circuits using 2PASCL are presented.

2. PROPOSED CIRCUIT OPERATION AND DESCRIPTION

2.1. Adiabatic Logic

The word adiabatic comes from thermodynamic which means zero loss or gain of heat during a state change. Fundamentally we know that in a CMOS inverter during charging and discharging CV_{dd}^2 energy is required from the supply. Half of this energy is dissipated by the PMOS ON state resistance during charging and half gets stored in node capacitance which discharged through NMOS to the ground. In adiabatic logic circuits, this charge recycles back to the power supply. The RC circuit for adiabatic charging and discharging is given in Figure 1. In this, the capacitor.
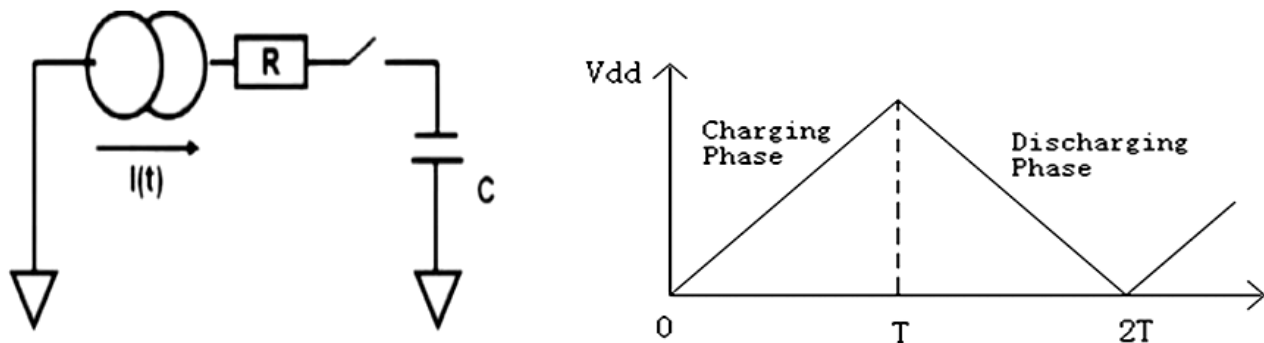

Figure 1: Adiabatic charging

C is charged via an MOS ON state equivalent resistor R through a constant current $I(t)$ as compared to a fixed voltage V_{dd} in conventional CMOS inverter[17]. If the initial charge at the capacitor is zero then the capacitor voltage $Vc(t)$ is given by the following expression.

$$V_c(t) = \frac{1}{C} i(t) * t \tag{1}$$

And
$$i(t) = C \frac{V_c(t)}{t} \tag{2}$$

As the current is constant due to constant current source hence the energy dissipation can be approximated by the following equation.

$$E_{diss} = R \int_0^T i^2(t)dt = Ri^2(t) * T = \frac{RC}{T}CV_c^2(T)$$ (3)

Where $V_c(T)$ is the voltage across the capacitor at time T. It is depicted from (3) that the energy dissipation is smaller as compared to conventional charging at V_{dd} supply voltage, when $T>2RC$. Also, the energy dissipation can be reduced by using a slowly time varying voltage supply i.e. longer T. In adiabatic charging the energy dissipation also depends on R hence reduction in R is also a possible way to reduce energy dissipation.

2.2. Binary and gray code

Binary codes consist of two digits '0' and '1', these two digits are used to represents the voltage levels generally 0 for low and 1 for high voltage. These codes are used to represents the signal for transmission and storage purpose. Gray codes are also called as reflected binary codes, in which the successive codes differ by a single digit. Gray codes are generally used for error correction due to their cyclic properties. The conversion of binary to gray and vice versa is important for many applications.

2.2.1. Binary to gray code conversion

If the four-bit binary inputs are B_1, B_2, B_3, B_4 and the corresponding output for gray codes are G_1, G_2, G_3, G_4 then gray codes are given as follows

$$G_4 = B_4$$
$$G_3 = B_4 \oplus B_3$$
$$G_2 = B_3 \oplus B_2$$
$$G_1 = B_2 \oplus B_1$$

2.2.2. Gray to binary code conversion

If the four-bit gray code inputs are G_1, G_2, G_3, G_4 and the corresponding output for binary codes are B_1, B_2, B_3, B_4 then the logical expressions for binary codes are given as follows

$$B_4 = G_4$$
$$B_3 = B_4 \oplus G_3 = G_4 \oplus G_3$$
$$B_2 = B_3 \oplus G_2 = G_4 \oplus G_3 \oplus G_2$$
$$B_1 = B_2 \oplus G_1 = G_4 \oplus G_3 \oplus G_2 \oplus G_1$$

Based on these logical expressions the gate level circuit diagrams are given in Figure 2 and 3.

2.3. 2PASCL based circuit operation

In this paper, four bit B-G and G-B converter have been proposed which is based on 2PASCL using six transistors X-OR gate. The operation of basic CMOS inverter using this logic can be explained with help of figure 4. In this two extra MOS transistors are used with complementary power supply clocks PC and $\overline{PC}$. One is 180° out of phase with the other one and the voltage magnitude of both power clock supplies is governed by (4) and (5) [15].
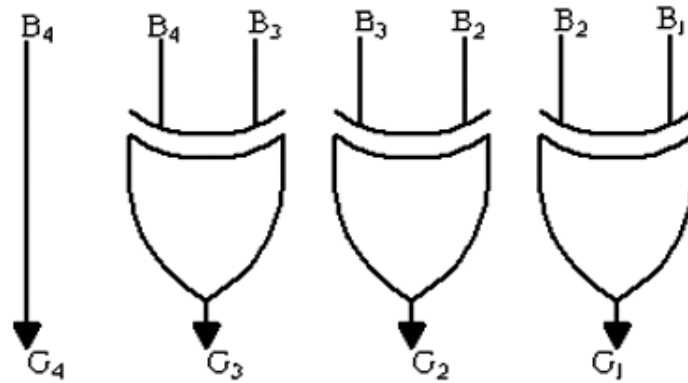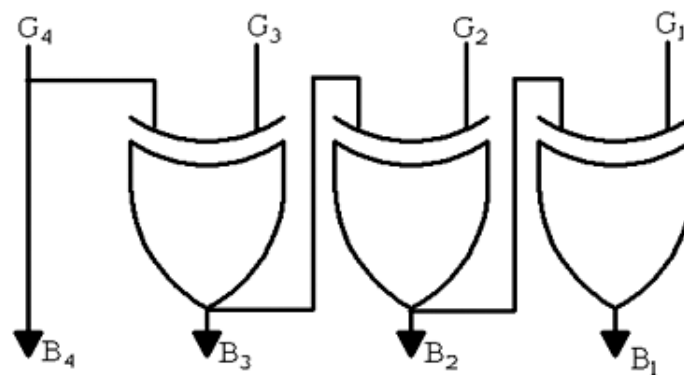
Figure 2: B-G Converter

Figure 3: G-B Converter

$$V_{PC} = \frac{V_{DD}}{4}\sin(\omega t + \theta) + \frac{3}{4}V_{DD} \tag{4}$$

$$V_{\overline{PC}} = \frac{V_{DD}}{4}\sin(\omega t + \theta) + \frac{1}{4}V_{DD} \tag{5}$$

The magnitude of V_{PC} is twice of $V_{\overline{PC}}$ to reduce the voltage difference between the electrodes which results in decreased power dissipation. In the proposed circuit split level clock supply charges/discharges the load capacitance slowly as compared to other clock pulse used in adiabatic logic. This also minimizes the energy loss. The operation of this circuit is divided into two steps, i.e. evaluation and hold.

1. During evaluation when output is low and pull-up network turns ON, the load capacitance C_L charged through PMOS and output goes HIGH. When the output is high and pull-down network turns ON discharging of load capacitance takes place via NMOS and D_2.

2. *In hold step if no transition takes place at input side the output will be held by the load capacitance consequently, reduces switching activity and results in decreased energy loss.*

3. EXPERIMENT AND RESULTS

In this report, all the circuits have been simulated in 0.18μm CMOS technology. The simulated results of conventional X-OR based design and proposed designs of B-G and G-B have been obtained with varying
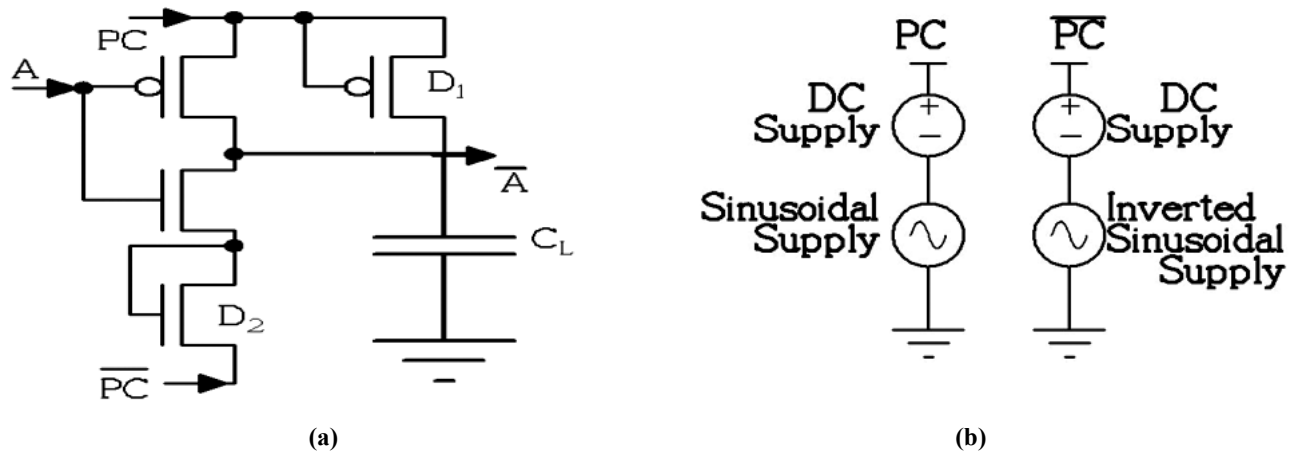
(a)   (b)
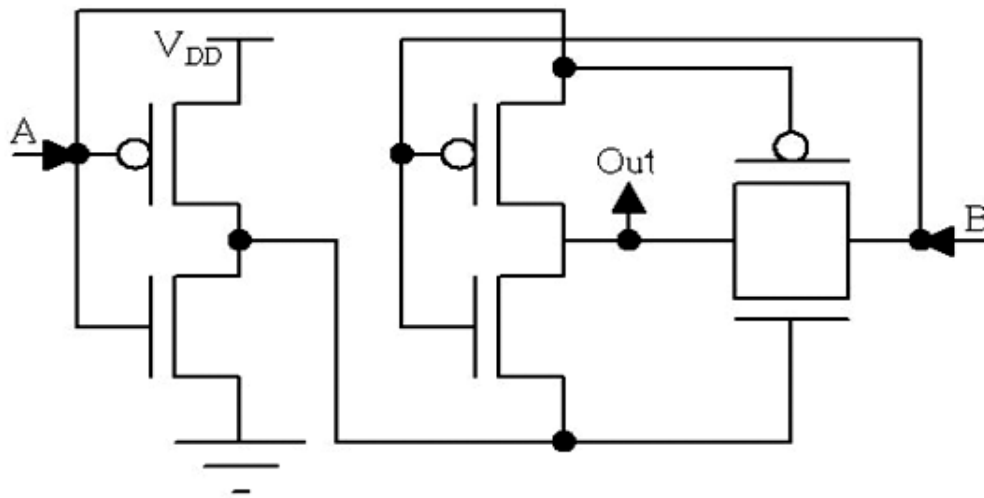
Figure 4: (a) 2PASCL based inverter (b) Power clock supplies

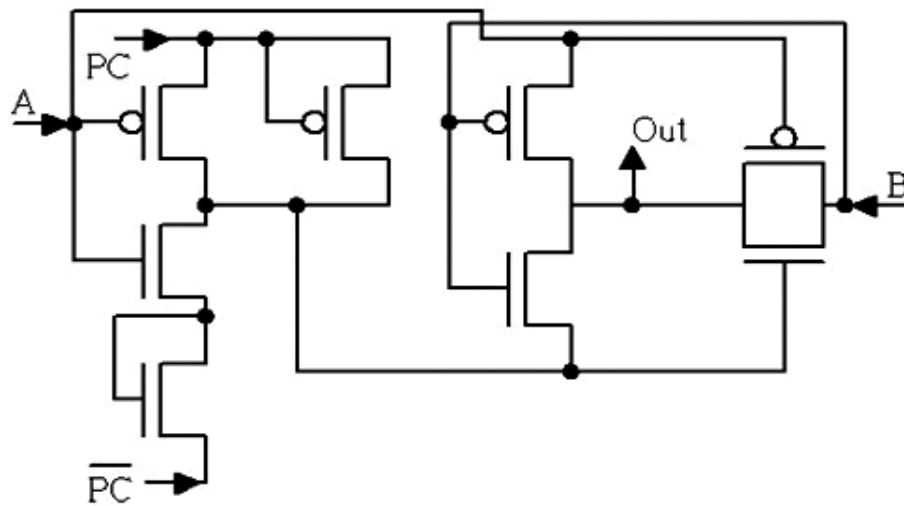**Figure 5: Conventional TG based X-OR gate**

Figure 6: 2PASCl based X-OR gate

supply voltage and temperature. The conventional TG and proposed X-OR used for converters has been shown in figure 5 and 6 respectively. The simulation results are compared with the help of tables and graphs. The conventional and proposed designs have been simulated with temperature 15°C to 50°C and the power supply has been varied from 1.1V to 2.4V. The magnitude of the sinusoidal source has been varied according to the supply voltage. Tables 1-8 shows the power dissipation, delay, and PDP of conventional and proposed B-G and G-B converter designs with varying voltage and temperature conditions. Here one X-OR gate delay has been considered in both conversions. The PDP results have been compared with the help of graphs as shown in figure 7-10.

Table 1
Power and Delay Results of B-G Converter with Voltage 1.2V to 2.4V

Supply Voltage (V)	Power (pW) Conventional	Power (pW) Proposed	Delay (ps) Conventional	Delay (ps) Proposed
1.2	141.58	50.94	2.56	3.51
1.3	167.60	59.69	2.44	3.45
1.4	196.55	69.23	2.33	3.38
1.5	228.61	79.62	2.22	3.02
1.6	264.00	90.88	2.11	2.69
1.7	302.94	103.05	1.99	2.59
1.8	345.67	116.19	1.89	2.50
1.9	392.44	130.34	1.79	2.41
2.0	443.51	145.56	1.72	2.40
2.1	499.17	161.89	1.63	2.38
2.2	559.72	179.39	1.56	2.29
2.3	625.48	198.10	1.50	2.17
2.4	696.78	218.04	1.44	2.06

Table 2
PDP of B-G Converter with Voltage 1.2V to 2.4V

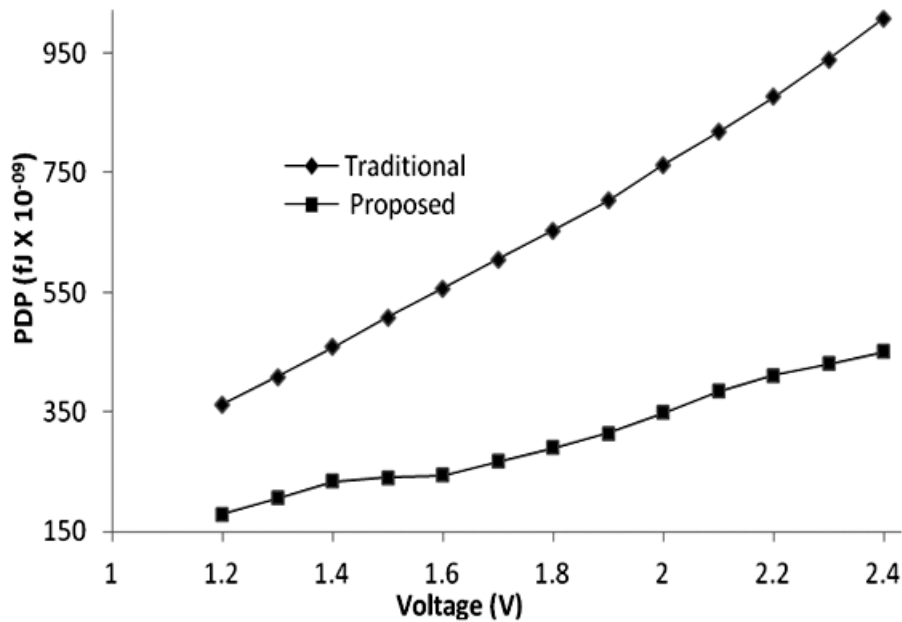| Supply Voltage (V)	PDP(fJ) $\times 10^{-9}$ Traditional	PDP(fJ) $\times 10^{-9}$ Proposed
1.2	363.15	179.01
1.3	409.33	206.11
1.4	458.43	234.13
1.5	508.30	240.83
1.6	557.16	245.04
1.7	605.35	267.37
1.8	653.98	290.61
1.9	703.84	314.90
2.0	763.64	349.63
2.1	817.80	385.31
2.2	876.25	411.42
2.3	939.66	431.08
2.4	1008.59	450.87

Figure 7: PDP comparison of B-G Converter with voltage 1.2V to 2.4V

Table 3
Power and Delay Results of B-G Converter with Temperature 15ºC to 50ºC at 1.8V Supply

Temperature in ºC	Power (pW) Traditional	Power (pW) Proposed	Delay (ps) Traditional	Delay (ps) Proposed
15	302.24	101.22	1.82	2.75
20	320.29	107.35	1.85	2.80
25	338.38	113.61	1.88	2.84
30	356.76	120.16	1.90	2.88
35	376.08	127.29	1.93	2.93
40	397.75	135.71	1.96	2.97
45	424.45	146.67	1.98	3.01
50	460.51	162.37	2.01	3.05

Table 4
PDP of B-G Converter with Temperature 15ºC to 50ºC at 1.8V Supply

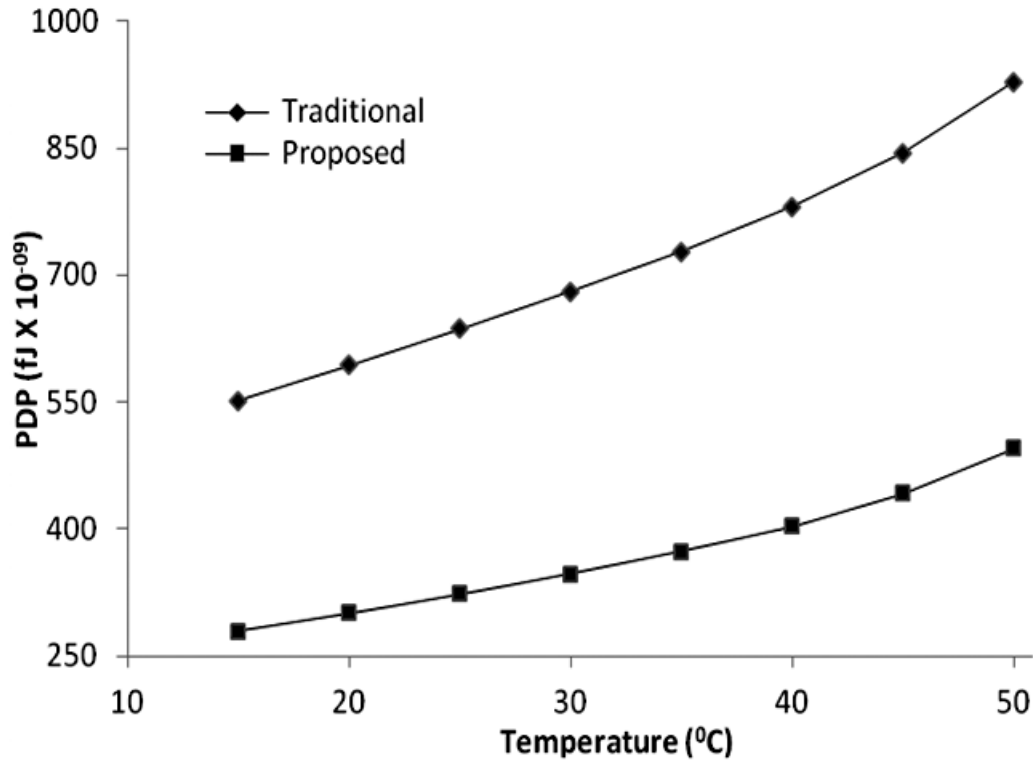| Temperature in ºC	PDP(fJ) $\times 10^9$ Traditional	PDP(fJ) $\times 10^9$ Proposed
15	551.31	279.28
20	593.53	300.87
25	636.50	323.38
30	680.81	347.17
35	727.94	373.22
40	780.63	403.54
45	844.36	442.05
50	928.06	495.60

Figure 8: PDP comparison of B-G with Temperature 15ºC to 50ºC at voltage 1.8V.

Figure 8 explained graphically the improvement in performance of proposed design as compared to traditional design of B-G converter with varying temperature in terms of PDP.

Table 5
Power and Delay Results of G-B Converter with Voltage 1.2V to 2.4V

Supply Voltage (V)	Power (pW) Traditional	Power (pW) Proposed	Delay (ps) Traditional	Delay (ps) Proposed
1.2	141.57	50.93	1.76	2.51
1.3	167.60	59.67	1.74	2.46
1.4	196.55	69.23	1.69	2.39
1.5	228.61	79.62	1.63	2.31
1.6	264.00	90.88	1.56	2.22
1.7	302.94	103.05	1.50	2.13
1.8	345.67	116.19	1.44	2.04
1.9	392.44	130.34	1.38	1.94
2.0	443.51	145.56	1.26	1.86
2.1	499.17	161.89	1.21	1.77
2.2	559.72	179.39	1.17	1.69
2.3	625.48	198.10	1.13	1.62
2.4	696.78	218.04	1.10	1.55

Table 6
PDP of G-B Converter with Voltage 1.2V to 2.4V

Supply Voltage (V)	PDP(fJ) $\times 10^{-9}$ Traditional	PDP(fJ) $\times 10^{-9}$ Proposed
1.2	250.25	128.09
1.3	292.01	146.96
1.4	332.31	165.82
1.5	373.01	184.38
1.6	414.09	202.50
1.7	455.99	220.09
1.8	499.12	237.26
1.9	543.80	254.11
2.0	559.14	270.85
2.1	604.90	287.56
2.2	654.88	304.37
2.3	708.86	322.15
2.4	767.22	338.86

It is evident from figure 9 that the proposed design for G-B converter shows better performance in terms of power efficiency with varying supply voltage.
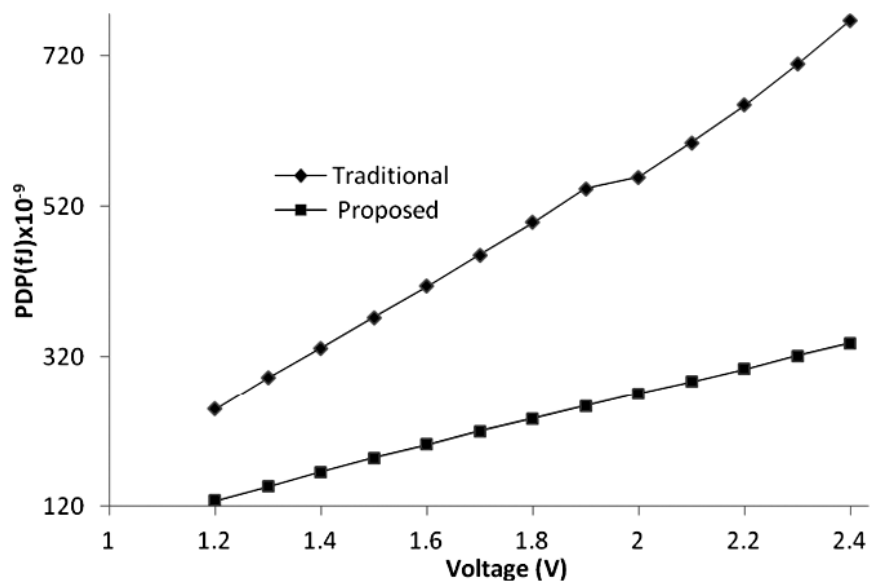

Figure 9: PDP comparison of G-B Converter with voltage 1.2V to 2.4V

Table 7
Power and Delay Results of G-B Converter with Temperature 15ºC to 50ºC at 1.8V Supply

Temperature in ºC	Power (pW) Traditional	Power (pW) Proposed	Delay (ps) Traditional	Delay (ps) Proposed
15	302.23	101.22	1.39	1.99
20	320.29	107.35	1.41	2.01
25	338.39	113.61	1.43	2.03
30	356.77	120.16	1.45	2.05
35	376.08	127.29	1.47	2.06
40	397.76	135.71	1.48	2.08
45	424.45	146.67	1.50	2.09
50	460.51	162.37	1.51	2.11

Table 8
PDP of G-B Converter with Temperature 15ºC to 50ºC at 1.8V Supply

| Temperature in ºC	PDP(fJ) × 10⁻⁹ Traditional	PDP(fJ) × 10⁻⁹ Proposed
15	421.10	202.02
20	453.25	216.33
25	485.86	231.11
30	519.31	246.58
35	554.05	263.31
40	591.98	282.79
45	637.44	307.74
50	697.58	342.87
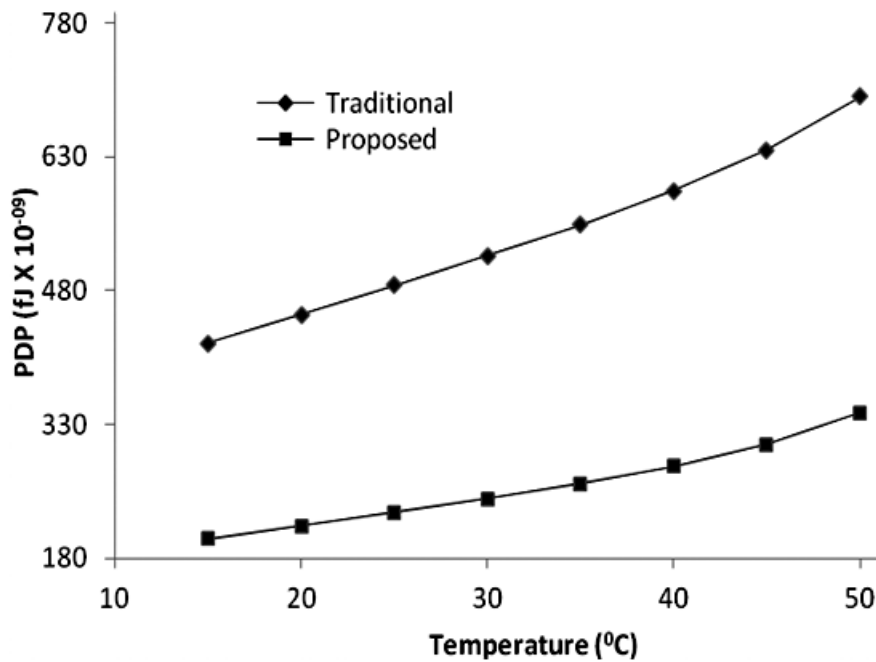
Figure 10: PDP comparison of G-B Converter with Temperature 15ºC to 50ºC at voltage 1.8V

Table-9 shows the comparison of proposed designs with existing designs reported in the literature in terms of power dissipation and transistor counts. Figure 11 shows the simulated waveform of code converters.

Table 9
**Comparisons of proposed designs with existing designs reported in literature**

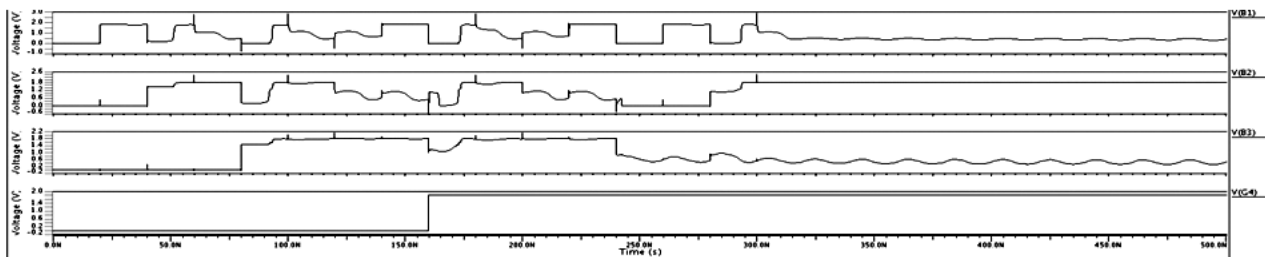| 9(a) For B-G Converter			9(b) For G-B Converter		
Transistor count	Power Dissipation	Logic Designs	Transistor count	Power Dissipation	Logic Designs
26	1.656 (µW)	Static[18]	26	1.656 (µW)	Static[18]
34	0.782 (µW)	2PASCL [18]	34	0.782 (µW)	2PASCL [18]
26	0.413(µW)	Power efficient[18]	26	0.413(µW)	Power efficient[18]
24	116.199(pW)	Proposed	24	116.199(pW)	Proposed
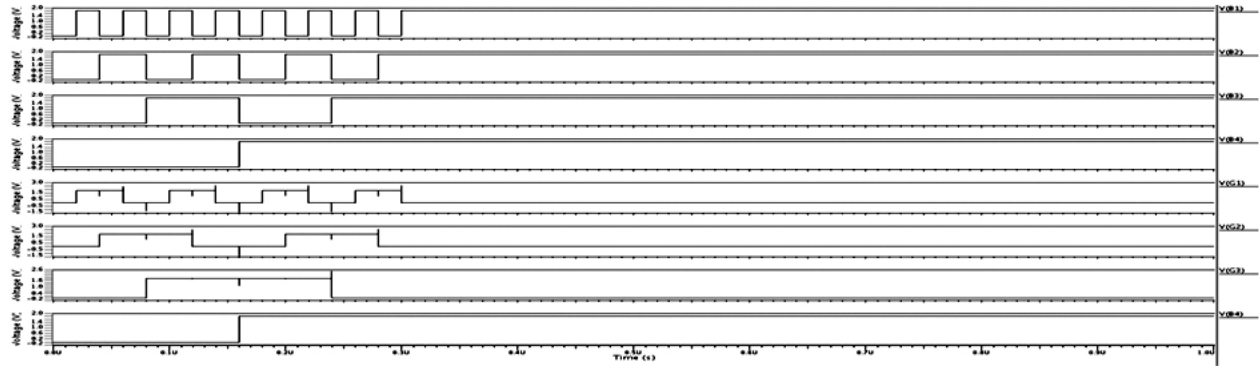
(a)
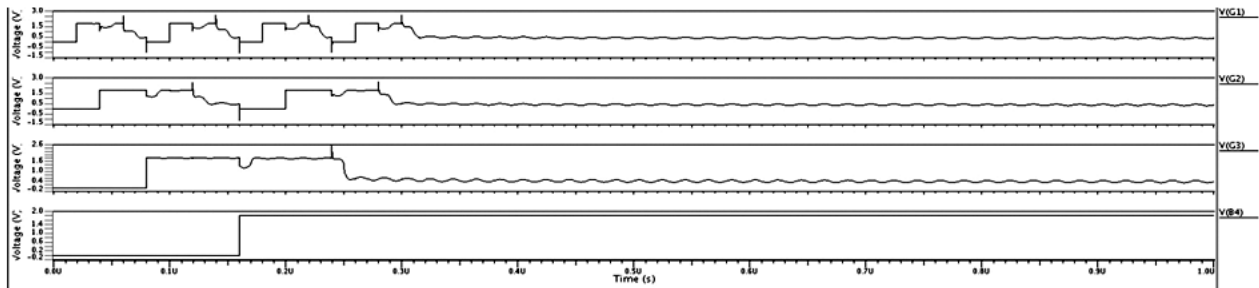
(b)
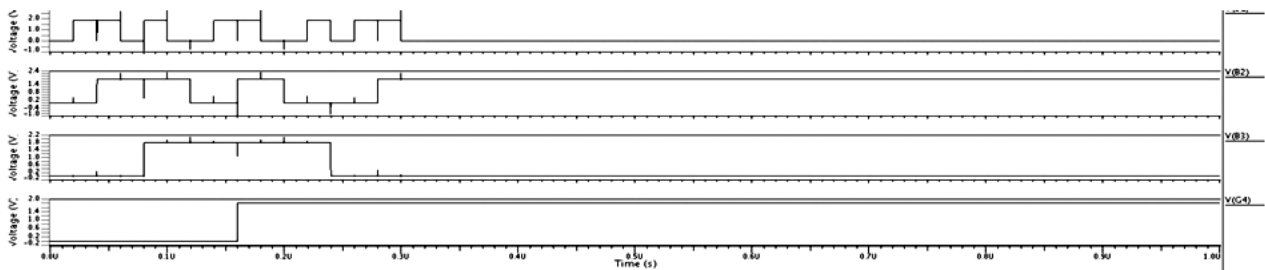
(c)

(d)

**Figure 11: Waveforms of (a) 4 bit input combinations and traditional B-G converter,
(b) B-G Converter for proposed design, (c) G-B Converter for traditional design,
(d) G-B Converter for proposed design**

4. CONCLUSION

In this paper, new deign of code converters have been proposed and results have been obtained in 0.18μm CMOS technology. The proposed design of binary to gray converter shows the reduction of 55.56% in terms of PDP as

compared to conventional design. The proposed design of gray to binary converter shows the performance improvement in PDP by reduction of 52.46% as compared to conventional designs. The proposed designs also show better performance with varying temperature conditions. Comparison with earlier work has been done in terms of power, delay and PDP, which shows that the proposed circuit approach is advantageous over previous ones.

REFERENCES

[1] S-M. Kang, Y. Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", 3rd edn.Tata McGraw-Hill, New York 2003, ch.1, sec 1.1, pp 2-3.

[2] K. Roy and S. Prasad," Low Power CMOS VLSI Design", In Low power 'CMOS VLSI Circuit Design, Ist Ed. USA, Wiley-Interscience, 2000, ch. 1,sec.1.2, pp. 2-3.

[3] K. Roy, S. Mukhopadhyay and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," in *Proceedings of the IEEE*, vol. 91, no. 2, pp. 305-327, Feb 2003. doi: 10.1109/ JPROC.2002.808156

[4] H. Iwai, "CMOS scaling for sub-90 nm to sub-10 nm", *17th International Conference on VLSI Design Proceedings,* 2004, pp.30-35 doi: 10.1109/ICVD.2004.1260899.

[5] V. V. Zhirnov, R. K. Cavin, J. A. Hutchby and G. I. Bourianoff, "Limits to binary logic switch scaling - a Gedanken model", in *Proceedings of the IEEE*, vol .91, no. 11, pp.1934-1939, Nov 2003. doi: 10.1109/JPROC.2003.818324.

[6] T. Skotnicki, J. A. Hutchby, Tsu-Jae King, H. S. P. Wong and F. Boeuf, "The end of CMOS scaling: toward the introduction of new materials and structural changes to improve MOSFET performance", in *IEEE Circuits and Devices Magazine*, vol. 21, no. 1, pp. 16-26, Jan.-Feb. 2005. doi: 10.1109/MCD.2005.1388765

[7] P.Ajit, " Adiabatic logic circuits", in Low Power VLSI Circuits and systems, Springer New Delhi Heidelberg New York Dordrecht London, Springer India 2015, ch10, sec 10.2, pp.304-306.

[8] Bai-Sun Kong, Young-Hyun Jun and K. Lee, "A True Single-Phase Clocking Scheme for Low-Power and High-Speed VLSI", *Circuits and Systems, 1997. ISCAS '97., Proceedings of 1997 IEEE International Symposium on*, 1997, pp. 1904-1907 vol.3. doi: 10.1109/ISCAS.1997.621522

[9] D. J. Frank, "Comparison of high-speed voltage-scaled conventional and adiabatic circuits", *Proceedings of 1996 International Symposium on Low Power Electronics and Design*, Monterey, CA, 1996, pp. 377-380.

doi: 10.1109/LPE.1996.54754

[10] M. Kumar, S. K. Arya, and S. Pandey, "An Energy-Efficient Full Adder Design Based on Energy Recovery Gates and Multiplexer Architecture", *The IUP J. Electrical & Electronics Engg.* Jan. 2011 vol. 4, no. 1, pp. 21-30.

[11] A. Kramer, J. S. Denker, S. C. Avery, A. G. Dickinson and T. R. Wik, "Adiabatic Computing with the 2n-2n2d Logic Family", *VLSI Circuits, 1994. Digest of Technical Papers., 1994 Symposium on*, Honolulu, HI, USA, 1994, pp. 25-26. doi: 10.1109/VLSIC.1994.586194

[12] A. Kramer, J. S. Denker, B. Flower, and J. Moroney, "2nd Order Adiabatic Computation with 2N-2P and 2N-2N2P Logic Circuits", *Proceedings of the International Symposium on Low Power Design*, 1995, pp. 191–196. doi: 10.1145/224081.224115

[13] S. D. Kumar, H. Thapliyal and A. Mohammad, "FinSAL: A novel FinFET based Secure Adiabatic Logic for energy-efficient and DPA resistant IoT devices," *2016 IEEE International Conference on Rebooting Computing (ICRC)*, San Diego, CA, 2016, pp. 1-8. doi: 10.1109/ICRC.2016.7738710

[14] S. Miryala, A. Calimera, E. Macii and M. Poncino, "Ultra Low-Power Computation via Graphene-Based Adiabatic Logic Gates," *2014 17th Euromicro Conference on Digital System Design*, Verona,2014, pp.365-371. doi: 10.1109/DSD.2014.49

[15] N.Anuar, Y. Takahashi, T. Sekine, "Low power 4x4 bit array two phase clocked adiabatic static CMOS logic multiplier", in Proceedings of the ITCCSCC 2010, 2009, pp. 296-299.

[16] S-M. Kang, Y. Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", 3rd edn.Tata McGraw-Hill, New York 2003, ch.7, sec 7..5, pp 295-300.

[17]   P. Teichmann, Adiabatic Logic: Future Trend and System Level Perspective. New York: Springer, 2011.

[18]   S. Konwar, T. B. Singha and S. Roy, "Power Efficient Code Converters Using Adiabatic Array Logic", *2014 Fourth International Conference on Emerging Applications of Information Technology,* Kolkata, 2014, pp. 167-172. doi: 10.1109/ EAIT.2014.5