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Performance Analysis of Array Multiplier Using SPL and Control Input Technique Based Adder Cells for Neural Networks

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Abstract: In this article presents the investigation of array multipliers using SPL and control input technique based adder cells. The proposed SPL based adder cell consumes low power, small silicon area and low delay compared to control input technique based adder cell. The proposed circuit is tested with 4 bit array multiplier in terms of power, delay for 45 and 180 nm technology nodes. The array multiplier shows 20 % improvement in power consumption and 18% improvement in transistor count and these parameters are analyzed using cadence virtuoso software.

Keywords: SPL logic, Control input technique, Array Multiplier, Low Power

1. INTRODUCTION

The ultimate goal of VLSI system is to reduce the energy consumption and silicon area of the systems. The switching power component is called as dynamic power dissipation and it is the major source of power dissipation in systems [11]. The mathematical model of neurons involves the components of arithmetic sub systems in neural architecture. The power optimization of neural network architecture is achieved by low power adder and multiplier cell with minimum footprint of the system [10, 3]. The improvement in neural network is obtained by using SPL based adder cell. The major advantage of single phase logic it requires small silicon area compared to all other designs. The SPL adder is designed by using factoring technique with small sub circuits.

The DPL gate consists of complementary inputs and outputs and is thus dual rail logic like CPL. The main idea of double pass transistor logic is both PMOS and NMOS networks are used in parallel. The signal degradation is avoided by using double pass transistor logic. There is no level restoration required in double pass transistor logic [2].

Markovic [5] has discussed several pass transistor logic families like CPL, DPL, and DVL. Complementary pass transistor logic consists of complementary inputs and outputs, a NMOS network. In CPL swing restoration is achieved by use of weak PMOS transistor. The main drawback of DPL logic is its transistor count. To overcome the problem of transistor count, a new logic family is derived named as DVL. The DVL is mainly used to eliminate redundant branches in double pass transistor logic. Kosonocky [4] proposed a concept called multi threshold techniques to minimize leakage current in the active mode of operation. The performance is improved by properly selecting low Vth devices and high Vth devices. The new hybrid style full adder circuit was analyzed by the various CMOS logic styles like C-CMOS, CPL, TFA, TGA [6]. Ivakhnenko [7] works on identifying and analyzing systems based on the theory of self organization have been actively pursued in the field of engineering and technology. The MCIT based adder cell decomposition logic is applied for sum expression and pass transistor logic applied for carry expression

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[1, 12]. A threshold is specified at each level to determine if the outputs of the elements in a layer are giving acceptable results [9].The basic idea of group method of data handling, which is a tool for modeling complex input-output relationships by building hierarchical polynomial regression networks, was used [7,8].

2. ADDER ARCHITECTURES

The model of neurons consists of adder and multiplier blocks in shown in figure 1.

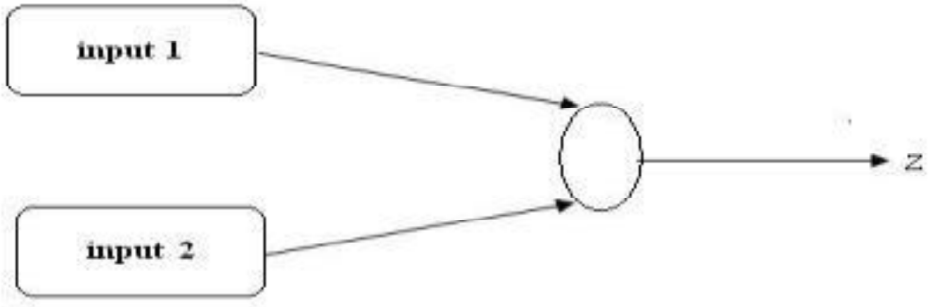

Figure 1: Neuron Hardware Structure

2.1. Control input method based adder cell for neural network

The CIT method is obtained by using mapping techniques for sub system in addition operation using factoring technique [1].

The Boolean expressions for sum and carry are given as in (1) and (2) respectively:

$$CARRY = AB + AC + BC \tag{1}$$

$$SUM = A'B'C + A'BC' + AB'C' + ABC \tag{2}$$

By using expressions (1) and (2), the pass transistor functions can be implemented.

The equation 2 is modified as equation 3.The multiplexing control input based adder cell using is shown in figure 2.

$$SUM = (A \oplus B).C' + (A \odot B).C \tag{3}$$

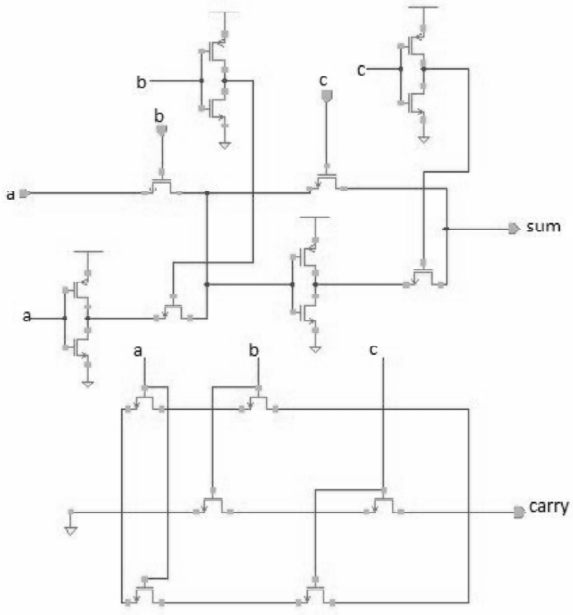

Figure 2: Existing area efficient adder cell using CIT

2.2. SPL based adder cell for neural network

The demerits of control input method based adder for neural architecture is transistor count. The SPL Shannon based adder cell consists of small silicon area and is designed using the concept of decomposition logic [10]. The proposed full adders have the modified expressions for the sum and carry as:

$$SUM = (A \oplus B).C' + (A \odot B).C \tag{4}$$

$$CARRY = (A \oplus B).C + (A \odot B).B \tag{5}$$

The SPL Shannon based adder cell is shown in figure 3.

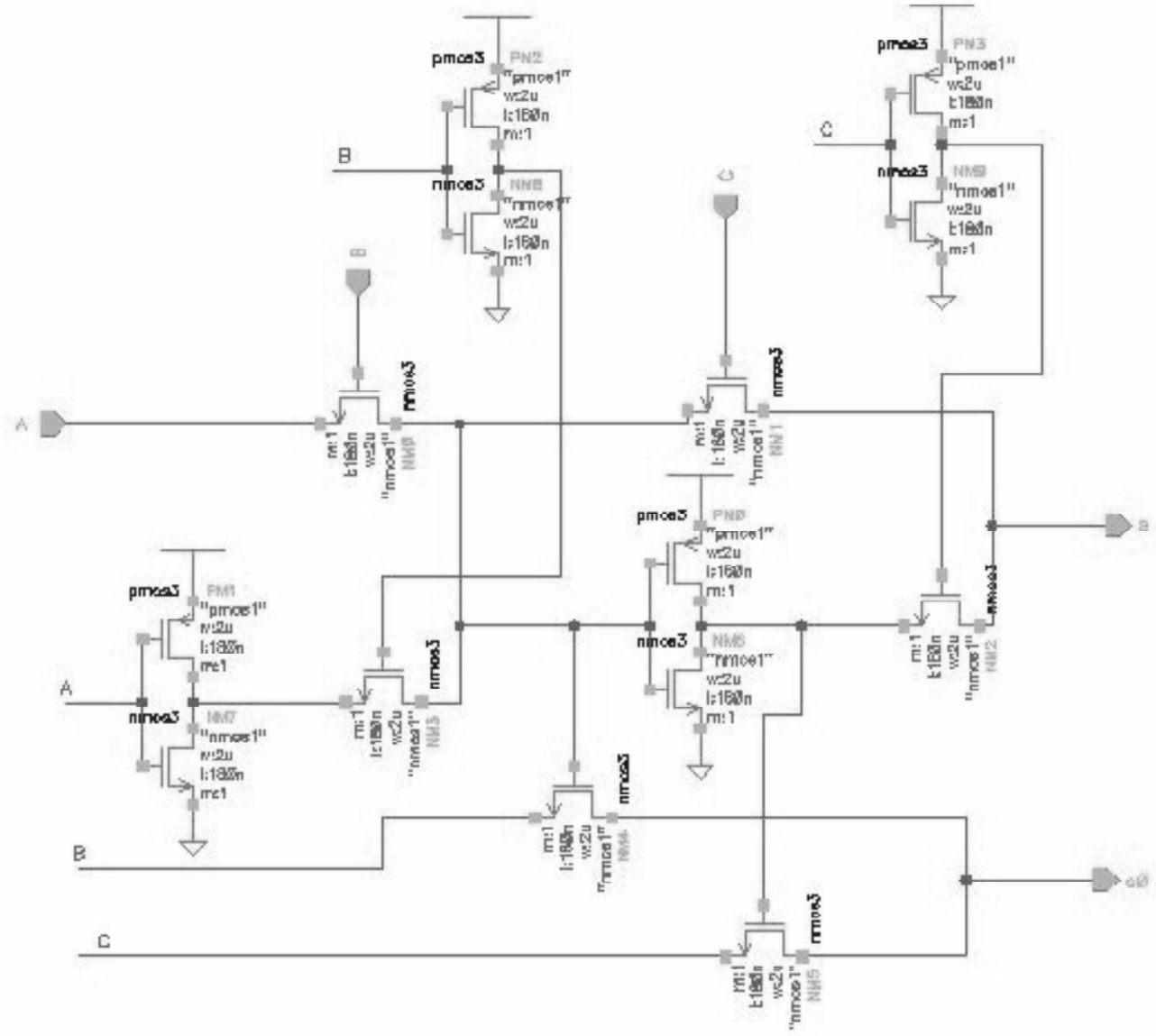

Figure 3: Proposed area and energy efficient SPL based adder cell

3. DESIGN OF ARRAY MULTIPLIERS

The 4 bit array multiplier is designed by using SPL based adder cell and control input technique based adder cells. The simulation is done with cadence virtuoso software. The schematic and simulations results of existing and proposed array multipliers are shown in figure 4 and 5 respectively.

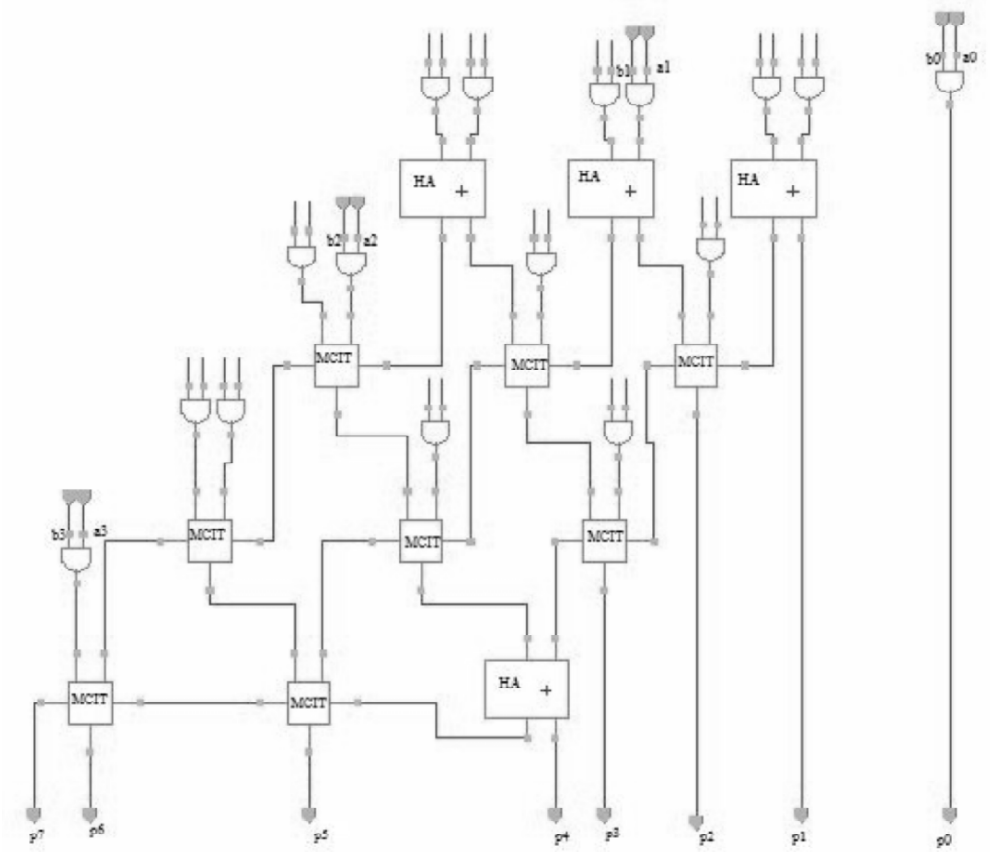

Figure 4: Existing 4 bit array multiplier using MCIT based adder cells

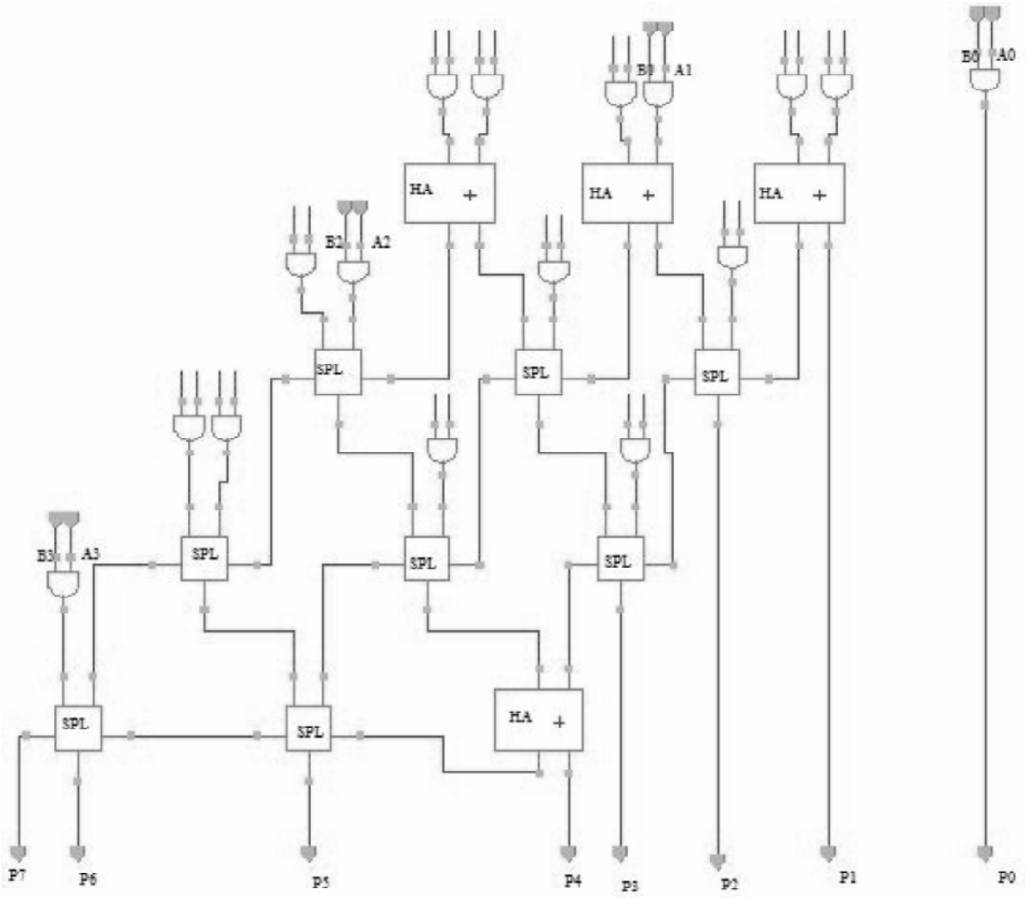

Figure 5: Proposed 4 bit array multiplier using SPL based based adder cells

4. SIMULATION RESULTS

Table 1
Power and delay calculation of proposed and existing adder cell designs

Type of Adder Cells	180nm-Power (W)	180nm-Delay(S)	45nm-Power(W)	45nm-Delay(S)
Existing area efficient adder cell using control input technique	21.9×10^{-6}	9.345×10^{-9}	88.5×10^{-9}	10.17×10^{-9}
Proposed area and energy efficient adder cell using single phase logic	11.32×10^{-6}	2.494×10^{-12}	78.41×10^{-9}	9.923×10^{-9}

Table 2
Power and delay calculation of 4 bit multipliers using MCIT and SPL based adder cells

Type of Array Multiplier Cells	180nm-Power (W)	180nm-Delay(S)	45nm-Power(W)	45nm-Delay(S)
Existing 4 bit array multiplier using control input based adder cell	1.147×10^{-3}	9.345×10^{-9}	4.056×10^{-6}	7.4×10^{-9}
Proposed 4 bit array multiplier using SPL based adder cell	1.087×10^{-3}	2.494×10^{-12}	3.162×10^{-6}	43.72×10^{-12}

The table 1 and 2 shows the performance of adder and multiplier cells are tested by applying the input patterns in cadence software. The performance is measured with the help of virtuoso in 45 and 180 nm technologies. The proposed adder and multiplier cells show better improvement in terms of power and delay.

5. CONCLUSIONS

In this power optimization technique, the SPL based adder cell is designed using XOR module as sub component. The proposed SPL adder cell is found to attain low power and minimum area when compared with the existing adder cell. This design can be verified using cadence virtuoso software. The area and energy efficient 4 bit low power multiplier cell can be designed with the help of this SPL based low power adder cell.

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