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FPGA BASED WIRELESS UNIVERSAL DIGITAL AUTOMATED TEST EQUIPMENT

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Abstract: Test & measurement accuracies decide & truly indicate any Country's Technological Progress. In electronics design and manufacturing industry, to ensure maximum quality and reliability of the product sold by all good companies design effort (time) : testing effort (time) is 1 : 6. This means testing is most important than design for quality assurance to product end users. In testing, ATE has a key role to play in the various levels of Electronics Product design life cycle & development. Thus the design and development of proposed low cost "FPGA based Scalable Universal Wireless Digital ATE" is used to test all kinds of Combinational Circuits, Sequential Circuits, Processors, SOC, PCB and motherboard physically.

Key Words: *Digital Pattern Generator, Digital logic analyzer, Device Under Test (DUT)/Circuit Under Test (CUT), ATE Controller*

I. INTRODUCTION

Advances in Fabrication technology has enabled VLSI engineers to go to sub-micron technology allowing them to pack millions of transistors in a single chip. All Technological advancements can be successfully proven only by best Testing of validation methods. Electronics is gaining maximum popularity and has become part and way of life of every human being. All Electronics designs, products and appliances can be successful only if they are tested completely before it is released into market.

In Today's Electronics world, 90% of electronic components sold in market is digital, so the need for Digital test equipment is very relevant. The IC tester available in the market tests only limited series of IC's, which is not desirable or affordable. It is necessary to test functionalities of all Sequential, Combinational circuits, Processors, SOC, PCB and Motherboard using unique device in lesser time and Automated Test Equipment (ATE) serves the above requirements.

ATE's popular Applications:

- ATE is widely used in the electronic manufacturing industry to test electronic components and systems
  (Combinational, Sequential circuits, Processors, Memories, SOC's and PCB's) after being fabricated.
- ATE is also used to test avionics and the electronic modules in automobiles.
- Military applications like radar and wireless communication

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1.1 Related Work

The disadvantages with VLSI Circuit testing are more number of discrete test equipments, slow speed, manual recording of results and use of general purpose software like EXCEL to compare the recorded data with those expected data(provided by design specifications) [6]. To overcome these draw backs industries started using very high hand test equipment called Automated Test Equipment (ATE) which had all standard discrete test equipments interfaced and controlled by a central control unit [6][1].

ATE control has evolved from dedicated sequencers to mini-computers and now to personal computers [5]. Teradyne, HP, Tektronix, Rico Scientific Industries, Theta Controls, Info Systems and Testo India Pvt Ltd. are the few major ATE manufacturing and supplying companies.

ATE is very large, vendor specific, non-scalable and expensive equipment, costs several millions of dollars and takes several months to build due to the need for custom made, complex circuitry and computing components [2] [3]
[4].ATE is used to test Integrated Circuits (IC's) by applying test patterns stored in ATE memory to the IC under test and comparing chip response with the expected response [4][1]. These test patterns typically involve waveform and timing generation via an Application Specific IC's (ASIC). Using FPGA Technology significantly reduce the cost of ATE by eliminating the huge non-recoverable development cost typically associated with ASIC designs and also provides enhanced functionality, flexibility to reprogram [4].

Now a days with the availability of computer controlled test equipments and test automation software like Lab view, Agilent VEE, Xilinx etc [6], lower cost/ higher speed ATEs can be designed.

1.2 Functional Overview of ATE

In general, there are two kinds of ATEs, one is dedicated and other is Universal. In Dedicated ATE, all input-output patterns are compacted, stored in a data base and compared with the expected outputs [1] and Working/Not Working Condition of the Circuits can be indicated by LEDs or 7-Segment Display.

The Problem associated with this kind of ATEs is no manual control over the circuits and it is Non-Scalable and this Problem can be solved by using Universal ATEs. In Universal ATE, additional Controller Circuit can be used to Scale up/down and Control the I/O Channels and frequency. Output of the Universal ATEs can be observed on PC Scope or Chip Scope.

Like Dedicated and Universal ATEs, there are two more types of ATEs namely: External and Embedded ATEs. In External ATEs, readily available ICs can be tested outside the ATE using bread board. Embedded ATEs consists of Built in Self-Test [EBIST] along with Pattern Generator and Logic Analyzer; all these Components can be built inside the ATE and additional circuits can also be tested using this kind of ATEs.

1.3 Need for Digital SOC ATEs

- The VLSI circuit manufacturer cannot guarantee the defect free integrated circuits(IC's). This makes necessary to evolve a fast accurate means of testing such circuits. ATEs used to test all such electronic components.

- 90% of all electronic components sold in market is digital. So, Digital ATE is very relevant. Today's quality requirement will require minimum one in a million failure rates.
- Development or design time spent is 30%, Time or resources spent on test are 70% in total Product development life cycle.
- Hardware & On-board Testing procedure or Emulation methods are expensive and exclusive to any particular CUT/DUT.
- The main problem associated with the ATEs is requirement of large investment. In a Small-Scale Industry/Test Lab, it may not be feasible to invest large sums of money on complex IC testers hence the main aim of "FPGA based Scalable Universal Digital ATE" RESEARCH is to reduce the overall investment on such equipment considerably.

1.4 Challenges in ATE design

1. Ever increasing bus width
2. Ever increasing speed
3. Accuracy and confirmative to standards
4. Power consumption
5. Size and mobility
6. Scalability & field Up gradation
7. Component absoluteness
8. Making it universal
9. Remote testing
10. Wireless testing
11. Flexibility
12. Up-gradation

II. TEST METHODOLOGY

In Proposed Universal Digital ATE, the Digital Test pattern generator is used to supply excitation to Circuit under test (CUT) in the form of pulses with different frequencies and corresponding response can be obtained by Digital Logic Analyzer. The Circuit under test (CUT) output can be stored in the Logic analyzer & user need to check the functionality of the devices based on their input and output results.

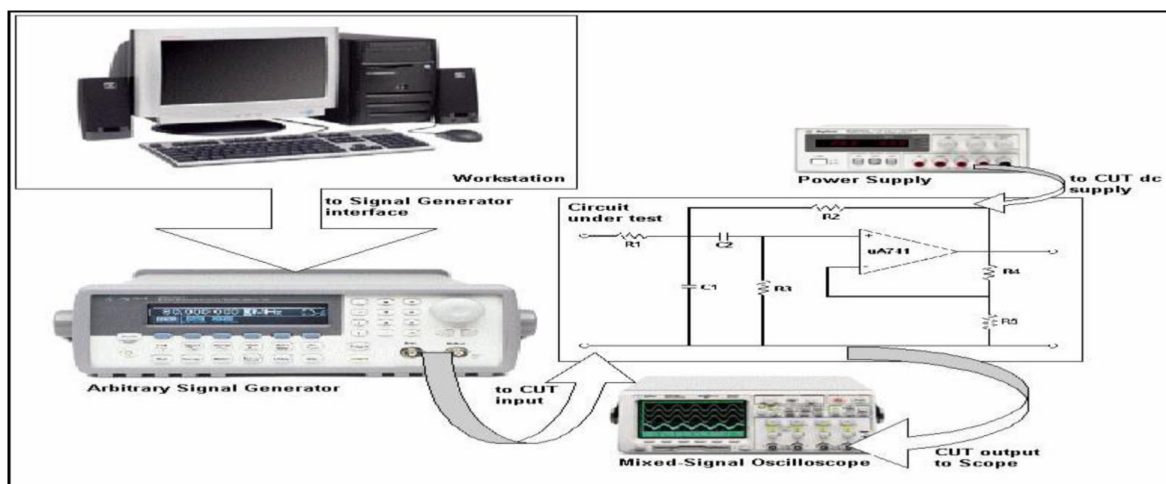


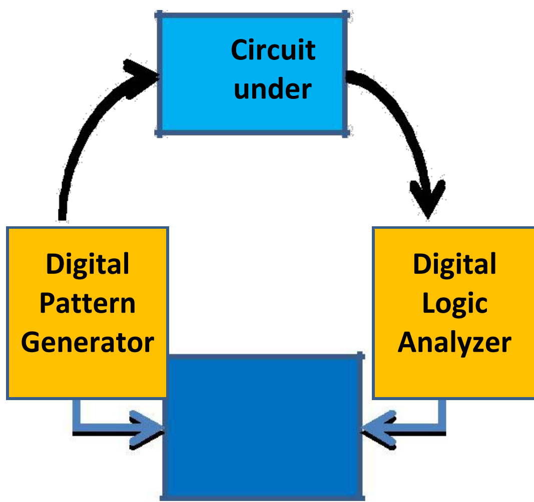
Figure 1. Broad view of Automatic test equipment

III. FPGA BASED ATE DESIGN

The main components associated with ATEs are Test Pattern Generator and Logic Analyzer. But the ATEs, Logic Analyzers and Pattern Generators are very expensive for everybody involved in Electronics Design to afford, as they run into Lakhs of Rupees (more expensive than the Design cost itself).

There is a very strong need to evolve some low cost, indigenous and accurate PC based equipment, which can perform the Test Vector Generation and which can provide Synchronous or Asynchronous Signals over 8/16/32/64 channels or bus widths, required to test ICs or Circuits or PCBs.

Circuit under



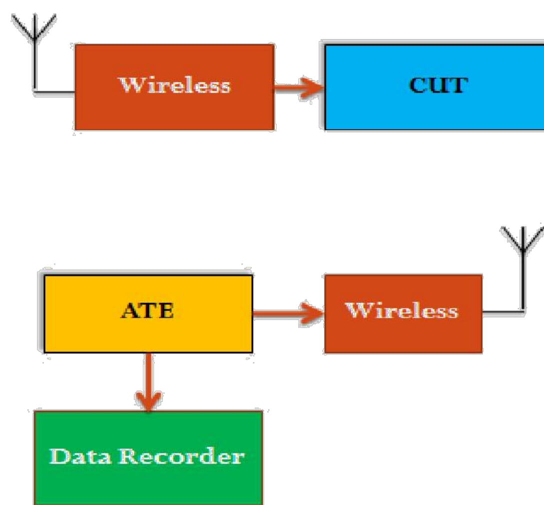


Figure 2. Wired Digital ATE **Figure 3. Wireless Digital ATE**

Digital Pattern Generator is useful for functional testing, debug of new designs and failure analysis of existing designs. Pattern Registers are usually used to store the different patterns of waveforms, the signals with different frequencies can be supplied by synthesizer. A switch matrix is used to route high frequency signals between the device under test (DUT/CUT) & measurement equipment; Input signals can be controlled by control signals (command).

Circuit under test (CUT) is nothing but any electronic assembly (Circuit/PCB) under test.

Digital logic analyzer is an electronic instrument which displays the signals of a Digital Circuit under test and used to check and analyze the test outputs. A logic analyzer may convert the captured data into timing diagrams, protocol decodes, state machine traces, assembly language, or correlate assembly with source-level software [15].

Dual port RAM (DPRAM) allows the simultaneous multiple read-write operations. High speed buffer is used to store the each bit used for transmission without miss, UART/RS232 used for

transmission-reception of the bits in serial/parallel manner. Working/Not working condition of the components can be realized by checking these bits.

IV. POSSIBLE OUTCOMES

The Digital ATE proposed to be implemented in FPGA shall have 32 channels, operated between 1 to 10MHZ, which can be scaled up to 256 channels, 100MHZ without difficulty.

The design is implemented on Xilinx Spartan 6 family based FPGA board, using Verilog HDL on Xilinx latest version software. The main features Wireless Digital Automated Test Equipments are fully programmable, Scalable, high speed data acquisition and high speed buffering methods used to test Digital Circuits/ICs.

Simulation, implementation and demo of Universal wired and wireless Digital SOC ATE can be used to test the functionality of

- Processor
- Motherboard
- Digital system
- Combinational (gates/encoders)
- Sequential (counters)
- Memory (RAM)

Proposed Cost:

- Reduce the cost of ATEs
- Prototype cost – less than 1,00,000 INR [Hardware & Software together]
- Product cost – less than 50,000 INR

Good Testing leads to:

- better quality products
- good brand value for company
- Testing leads to total Customer satisfaction
- Improves yield in manufacturing
- Repeat & referral business

V. CONCLUSION

This paper is part of my Research work, I have covered the aspects like – need for ATEs, types of ATEs available in the market a Products, Applications of ATEs, Key issues & challenges in the Design of Digital ATEs, Key performance parameters like Testing time taken, speed of operation, cost, Power etc. I have indigenously designed and proposed a novel architecture for Wired & Wireless Digital ATE that I plan to implement on FPGA. The Universal Digital ATE is designed for low cost and high performance applications used in electronic manufacturing industries to test electronic components and systems.

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