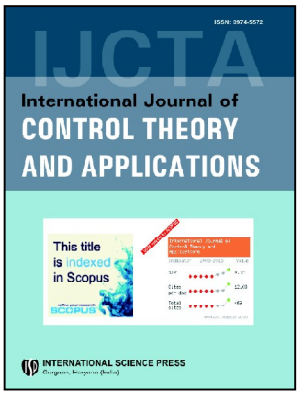

International Journal of Control Theory and Applications

ISSN : 0974-5572

Volume 10 • Number 29 • 2017

QCA Based High Speed Arithmetic and Logical Computational Unit in Microprocessor

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Abstract: Quantum dot Cellular Automata is another innovation in nanometer range i.e. 2 to 18nm, to maintain nanotechnology. QCA is particularly convincing similarly as high space thickness and will accept an essential part in the change of the Quantum Personal Computers (PC) by small power use. This paper describes the design and layout of a 4-bit Arithmetic and Logical Unit based on quantum-dot cellular automata using the QCA Designer design tool. This design depends on combinational circuits which decreases the required hard-product multifaceted nature and takes into consideration sensible pastime. The paper intends to give confirm that QCA has possible applications in future Quantum Computers, gave that the unseen modernization is made practical and plan is also compared with CMOS technology. The QCA layout for 4-bit ALU is implemented and further this layout will be helpful for fabrication. Additionally, simulation and computational analysis for same 4-bit ALU has been done by using CMOS technology and it has been observed that area efficiency (0.789um^2) and processing time is improved in QCA technology.

Keywords: Arithmetic and Logical Unit, Nano-technology, Quantum Dot Cellular Automata

1. INTRODUCTION

Quantum dot Cellular Automata is another innovation in nanometer range i.e. 2 to 18nm, to maintain nanotechnology. QCA is particularly convincing similarly as high space thickness and will accept an essential part in the change of the Quantum Personal Computers (PC) by small power use. This paper describes the design and layout of a 4-bit Arithmetic and Logical Unit based on quantum-dot cellular automata using the QCA Designer design tool. This design depends on combinational circuits which decreases the required hard-product multifaceted nature and takes into consideration sensible pastime. The paper intends to give confirm that QCA has possible applications in future Quantum Computers, gave that the unseen modernization is made practical and plan is also compared with CMOS technology. The QCA layout for 4-bit ALU is implemented and further this layout will be helpful for fabrication. Additionally, simulation and computational analysis for same 4-bit

ALU has been done by using CMOS technology and it has been observed that area efficiency (0.789um^2) and processing time is improved in QCA technology.

(A) Quantum Cell

Quantum Dot Cellular Automata relies on upon the coordinated effort of bi-stable QCA cells created from four quantum-dots. An anomalous state graph of two enchanted QCA cells is shown in Fig. 1.

Each cell is produced from four quantum dots [2] arranged in a square plan. The cell is blamed for two electrons, which are allowed to tunnel between bordering dots. These electrons have a tendency to have antipodal goals as a delayed consequence of their mutual electrostatic revolution.

Varieties of QCA-cells are able to be masterminded to play out every rationale capacities. It is expected to the Columbic co operations, that impacts the polarization of neighboring cells. QCA structure has been proposed with possible obstructions amid the dots that can be controlled and used to clock QCA circuits.

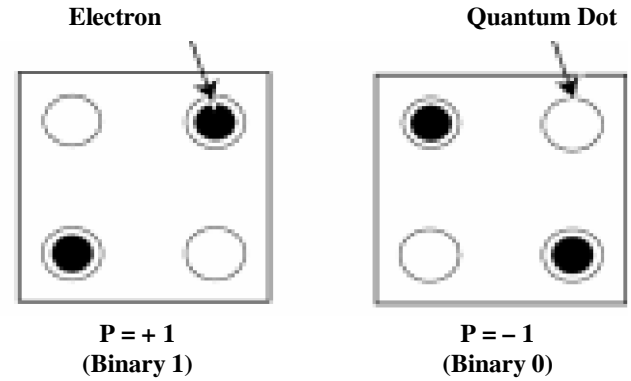

Figure 1: QCA Cell

(B) QCA Cable

One method for moving information from call attention to bring up of a QCA circuit[5] is with a 90-degree wire. The QCA wire is a level line of QCA cells. A twofold banner induces anticlockwise in Fig.1 for the reason that of electrostatic co operations between adjacent cells as appeared in fig. 2 (a). In QCA wire, binary information propagates from input terminal to output terminal due to columbic interaction between two cells. This also called as QCA arrays[6]. A QCA wire in the same way can be considered with 45 degree phase shifted as in fig.2 (b). This type of cells can be used in creating crossover or multilayer in the circuit.

Figure 2 (a): QCA cable

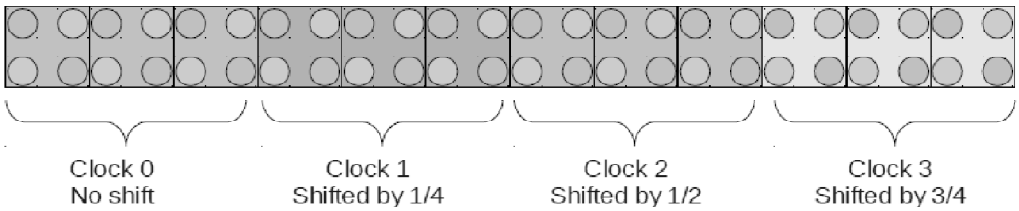

Figure 2(b): QCA cable (with phase shift)

(C) QCA Clock

The movement of electron is done by the help of clocking present in QCA. In clocking zones cells are clocked with four clocking phases such as toggle phase, hold phase, free phase, rest phase [7].

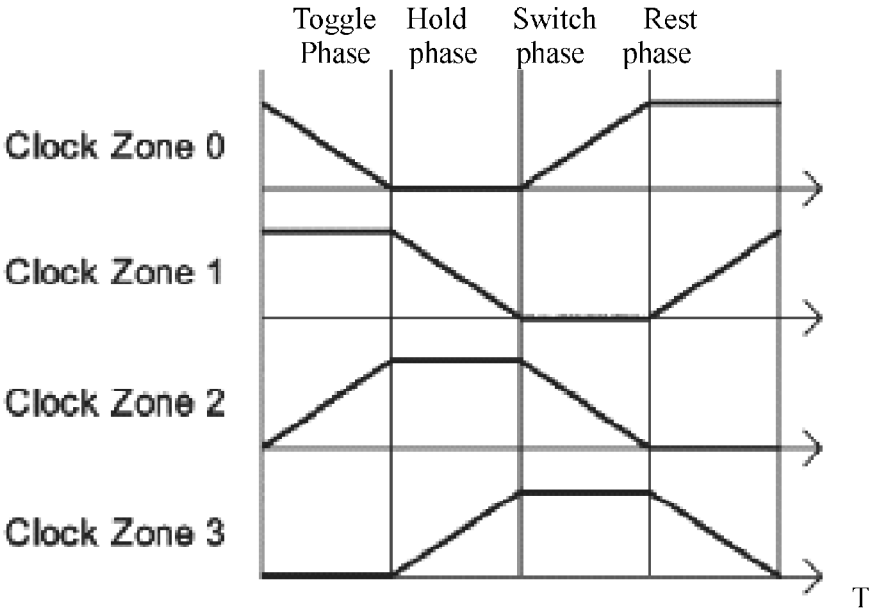

Figure 3: QCA Clock

In toggle phase the cells are unpolarized and with low potential but barriers are raised in this phase as depicted in figure below. In next phase the barriers are held in high potential and in next phase cells are in low potential at the last phase barriers are kept in lower and unpolarized state.

(D) QCA Logic

By appropriately masterminding the cells any basis logic function can be made. Consider the arrangements shown below in figure 4, speaking to the QCA execution of an inverter and a majority gate. By settling the polarization of one contribution to a greater part door, we can deliver regular rationale capacities, for example, the logical AND gate[9] entryway or potentially door.

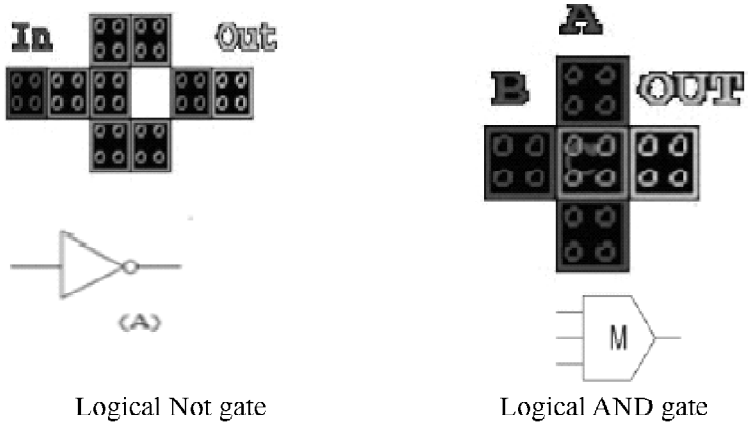

Figure 4: Basic QCA Gates

(E) Steps to Design the QCA Layouts

The various QCA designing steps are as follows:

1. QCA layout is to be designed using majority gates from the proposed logical circuit.
2. Check for Bi-stable or coherence vector parameters in QCA designer tool these are called as simulation engines.
3. Set all parameters for QCA clock as well as for simulation and perform simulation.
4. Then do the simulation for QCA layout that shows results which is same as truth table logic design. Thus the proposed logical circuit working is verified.

1. Proposed Work

A Design of an ALU[7] using QCA nanotechnology is recommended for upcoming maturity from this article. Most of the operations of a CPU are performed by one or more ALUs, which load data from input registers. A register is a small amount of storage available as part of a CPU. The control unit tells the ALU what operation to perform on that data and the ALU stores the result in an output register. The control unit moves the data between these registers, the ALU, and memory.

An arithmetic logic unit (ALU) represents the fundamental building block of the central processing unit of a computer. The reason for the ALU is to perform numerical operations such as arithmetic and logical operations, for example, expansion, subtraction, duplication and division. Moreover, the ALU forms essential intelligent operations like AND/OR estimations. Otherwise called the number-crunching rationale unit, it serves as the computational center point of the Central Processing Unit for a PC framework.

Modern CPUs contain very powerful and complex ALUs. In addition to ALUs, modern CPUs contain a control unit (CU). Here we have designed a 4-bit ALU in cadence and results are compared with that of QCA designer tool. The 4- Bit ALU is designed using four 1-Bit ALUs as shown in figure 5(a).

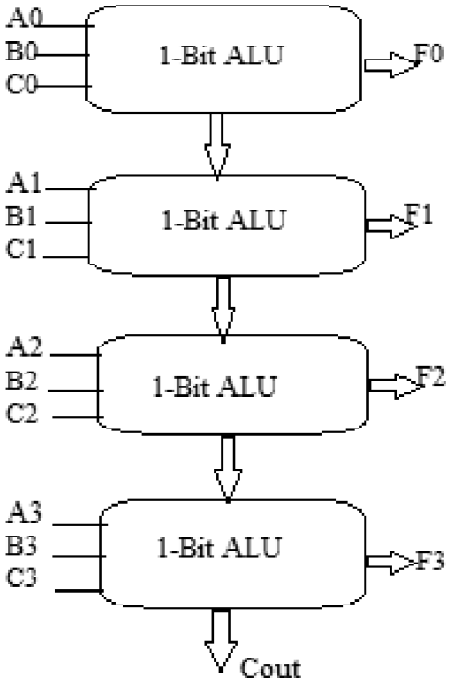

Figure 5 (a): 4-bit ALU

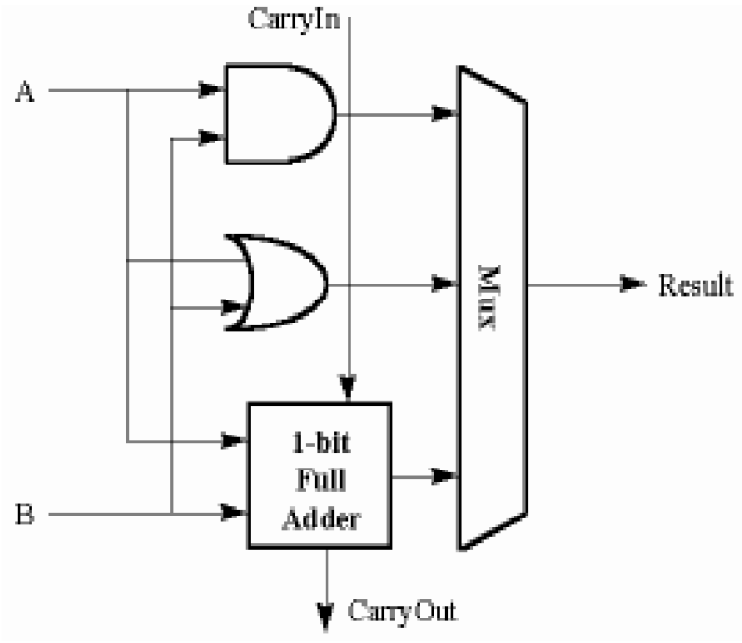

Figure 5(b): 1-bit ALU

Multiplexer (Mux)[3] also called as data selector, is a combinational circuit that is one of the most widely used in digital design. Mux will gate one out of several inputs to a single output. n number of data inputs & one output line & m select lines where $2^m = n$ and depending upon the digital code applied at the select inputs one out of n data input is selected & transmitted to a single output channel.

Block schematic of one-bit ALU is given in Fig. 5(b). Operation performed by a one bit ALU is detailed below in table-1.The operation of the circuit depends on the control signals S0 and S1.

Table 1
Operation of 1-bit Alu

Sr. No.	*Control Signals*		*Output*
	S1	*S0*	*F0*
1	0	0	And Operation F0 = A0.B0
2	0	1	OR Operation; F0 = A0 + B0
3	1	0	XOR Operation; F0 = A0xor B0
4	1	1	Full Adder Operation; Carry = COUT3, F0 = (A XOR B) XOR C

3. SIMULATION RESULTS

For proposed plan of arithmetic and logic computational block, four operations similar to logical-AND/OR and logical Ex-OR estimation as well as arithmetic operation like Adder is considered. Design and Simulations of the design in regularity and additionally QCA are established as follows.

Simulations are done using Xilinx ISE Design 14.4, Cadence and QCA Designer tool. The operation is checked for all possible combinations of inputs and verified. The RTL schematic of a 4-bit ALU is shown below which describes the gate level design of ALU and is used for cadence simulation.

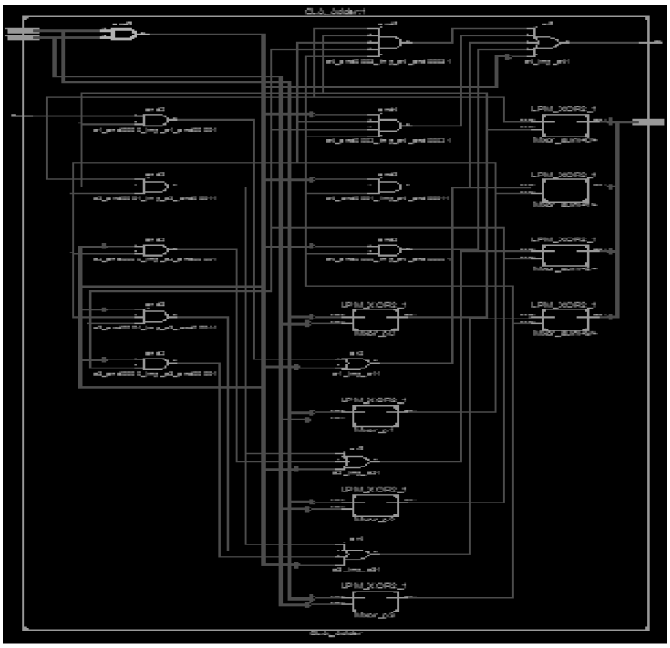

Figure 6: RTL Schematic of 4-Bit ALU

Figure 7: Output of 4-bit ALU in Verilog

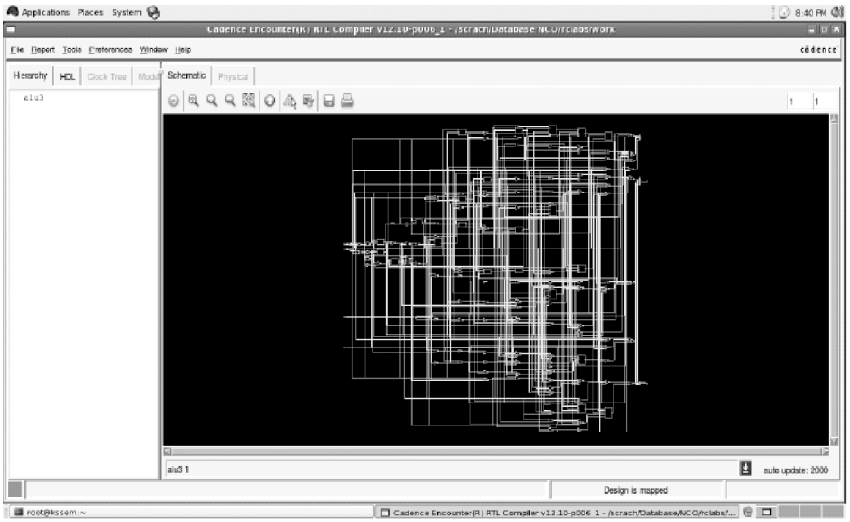

Figure 8: Design of ALU in cadence

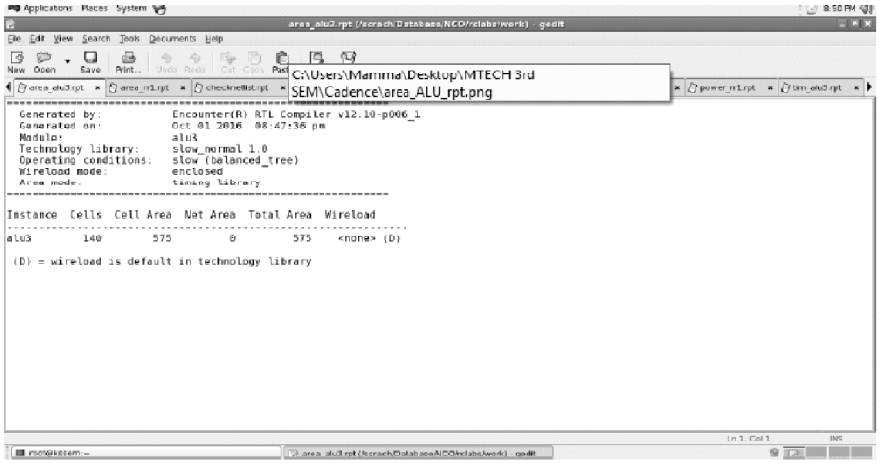

Figure 9: Area and Power used for ALU in cadence

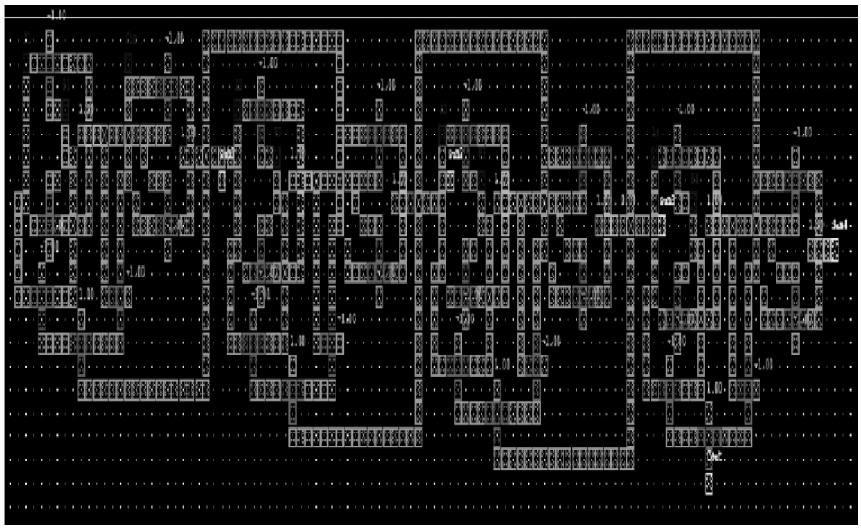

Figure 10: Proposed design of 4-bit ALU in QCA

To prove the QCA nanotechnology is most innovative over the CMOS technology the comparison is done between CMOS technology and QCA technology as illustrated in table 2 shown. From the comparison table 2 as described below it is clearly proved that the QCA has less power, energy dissipation, reduced area and high speed of operation.

Table 2
Comparison between CMOS and QCA based ALU

Parameters	*CMOS Technology*	*QCA Technology*
Area	575um^2	0.789um^2
Number of Cells	148 logic Gates	489 cells
Run time	11s	2s
Power	1372nW	0.233fW

4. CONCLUSION

QCA Designer tool is used for completion and simulation for the proposed design and relative study of the design and its internal elements is done in both CMOS and QCA technology. QCA based ALU is faster because it has got less area (0.789um^2) and runtime is also very less (2s). It is also area efficient compared to CMOS technology, which is a heart of the upcoming Nano processor technology.

5. ACKNOWLEDGEMENT

As a token of appreciation, the authors thank Professor T.Srinivas of Indian Institute of Science, Bangalore for his constant guidance and reading of the Journal article again and again and provide valuable comments to help us improve the final presentation

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