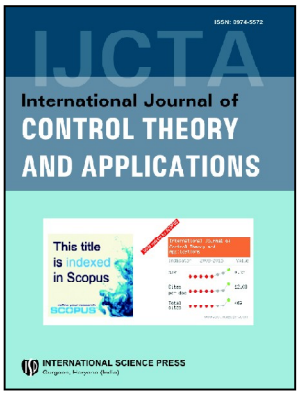

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Design of Combinational Circuits by Implementing NAND Logic using Quantum-Dot Cellular Automata (QCA)

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Abstract: Moore's Law states that the number of transistors per square inch on integrated circuits has doubled approximately every two years, this is true for CMOS based VLSI circuit design. Quantum-Dot Cellular Automata (QCA) replaces CMOS based VLSI technology. The assembly of quantum dots replaces transistors which is said to be "Quantum Dot Cellular Automata", an emerging nanotechnology in the field of quantum electronics. Such type of circuit can be used in many digital applications and has an advantage of reduced area utilization. Quantum mechanics and cellular automata are together said to be Quantum Dot Cellular Automata. QCA technology has advantages like small size and high speed. CMOS technology uses transistors to create a logic gates but in QCA technology, logic gates and wires are created by using QCA cells. The basic logic gates like AND, OR, inverter, majority gates are implemented. Many combinational and sequential circuits are designed by using these basic gates. This paper aims at the design of some basic combinational circuits like Half adder, Half subtractor, Multiplexer and Demultiplexer using NAND logic. The circuit was designed and the functionality of those combinational circuits was verified using QCADesigner tool and total area of NAND gate designed in QCADesigner 2.3.0 is compared with Microwind 3.1 (CMOS technology).

Keywords: Combinational circuit (NAND logic), QCADesigner 2.3.0, Microwind 3.1

1. INTRODUCTION

In 1965, Gorden Moore proposed Moore's Law which suggests that the chip increases its size exponentially with time [1]. It is true for CMOS based VLSI circuit design. Hence, to fabricate CMOS transistors into smaller size, it will eventually hits its fundamental physical limitations. By reducing the transistor size, we can achieve high speed, high design, low power dissipation. So many alternatives have been proposed and studied by the scientist to invent new technology which increases the device density. Very Large Scale Integration process of creating IC by combining tools of a transistor into a single chip. Before the introduction of technology, the most IC's had a limited set of functions they could perform. A complex circuit like computer is dependent on speed. If the components of computer are too large or the wires interconnecting them are too long, the electric signals could not travel fast through the circuit and it makes the computer too slow to be effective. Solution for this problem is to make all the components and the chip out of the same block of semiconductor material. Number of components

and wires has to be assembled manually, hence circuit becomes smaller. All components are to be integrated into a single silicon wafer came into existence, which lead to development in SSI. Later, LSI as well as VLSI with 10,000's transistors on a single chip.

Nanotechnology is a new computing method which provides a possible alternative to overcome these problems. International Technology Roadmap for Semiconductors (ITRS) reports summarizes several nanotechnologies with **QCA** as a possible option [2].

2. QUANTUM-DOT CELLULAR AUTOMATA

2.1. QCA Survey

In 1993, C.S.Lent et al., proposes QCA to replace CMOS technology [3]. It is based on quantum dots which is suitable for high performance logic circuits. The QCA creates general functions at the nanoscale by simply encoding the binary information in the position of single electron. Based on the principle of QCA, it solves problems which are faced with circuit implementation when their size approaches at the nanoscale. ATIPS (Advanced Technology Information Processing System) laboratory at the University of Calgary by Mi-Na (Microsystem–Nanotechnology) group developed QCADesigner version 2.3.0 which is a layout and simulation tool for Quantum-Dot Cellular Automata.

2.2. Elements of QCA

QCA Cell

In 1997, QCA cell was first fabricated, is the fundamental element of QCA technology. It a small cell that contains four quantum dots called potential wells arranged in square pattern positioned at the corners which are connected by the tunnelling barriers. The cell contains only two electrons which are located diagonally. But in symmetric cell (rotated 45Ú cell) the potential wells are located in the centre of the cell. Electron travel through the tunnel junction from one potential well to other under particular condition, by the clock signal.

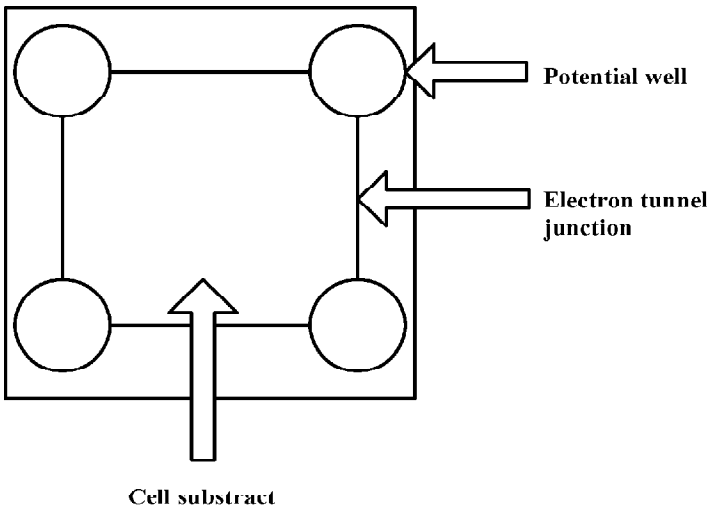


Figure 1: Basic QCA cell

Without any interaction, the two electrons get separated from each other in largest distance, due to the columbic force of interaction between electrons [4]. Because of this columbic force of interaction the electrons are diagonally located inside the potential well, because it will be the largest possible distance.

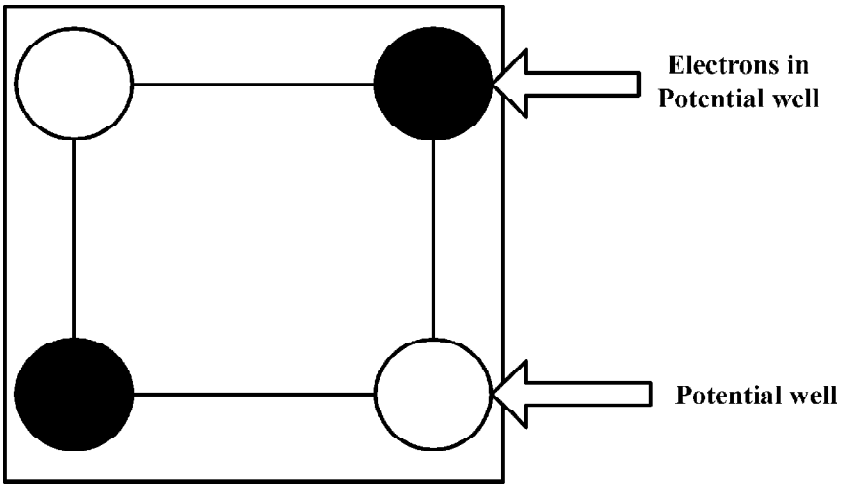


Figure 2: Electrons in QCA Cell

There are two polarization states which are represented by binary information (binary 0 and binary 1) in QCA cell.

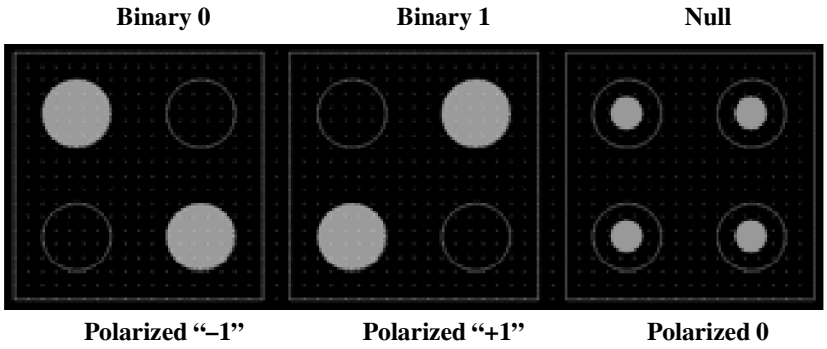


Figure 3: QCA cell polarization

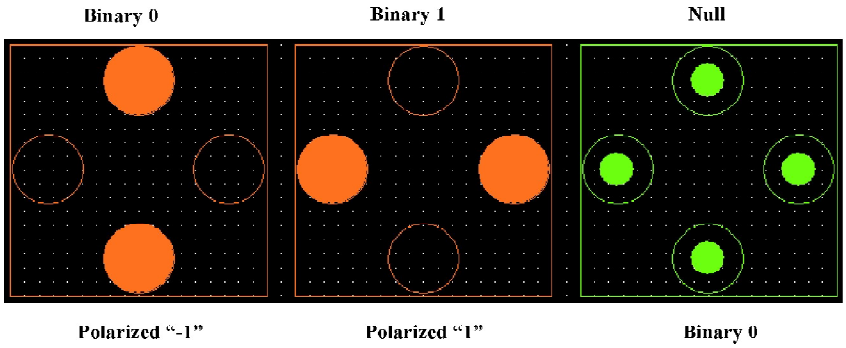


Figure 4: Symmetric (rotated 45°) cell polarization

QCA Wire

Array of QCA cells are called QCA wire and the information is passed from one end to other end through the wire, proper clock signals are to be given in order to maintain the flow of information correctly through the wire. Same polarization state must be carried out through the wire, in normal QCA cell.

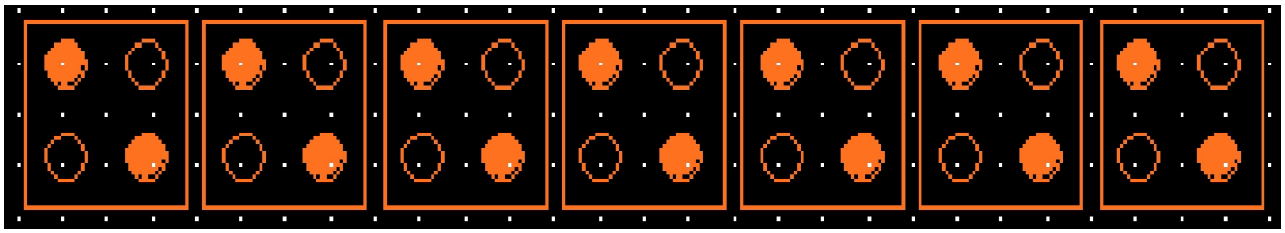


Figure 5: QCA wire

But if the QCA wire is created by using symmetric (rotated 45°) cells, opposite polarization states are carried through the cells. When two cells 45° are placed adjacent to each other, they always have opposite polarities, which results in the ground state of the system of those cells.

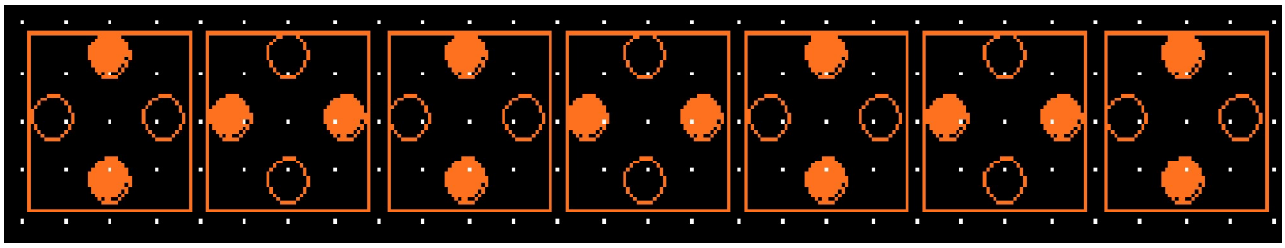


Figure 6: QCA wire using symmetric (rotated 45°) cells

QCA Clocking

Proper clocks are given to maintain the flow of information correctly through the QCA wires [5] The QCA technology consists of four clock phases: **switch** (unpolarised cells are driven by some input and get polarized depending on their neighbour's polarization), **hold** (cells are held in some definite polarization representing a binary state), **release** (cells lose their polarization) and **relax** (when cells lose their polarization in release phase, they remain unpolarised or null in this state). Each of these phases is a quarter of cycle apart from the previous phase which can be implemented by generating four clocks each with ð/2 phase difference from previous one. The four phases of a QCA clock are shown in Figure 8 [5].

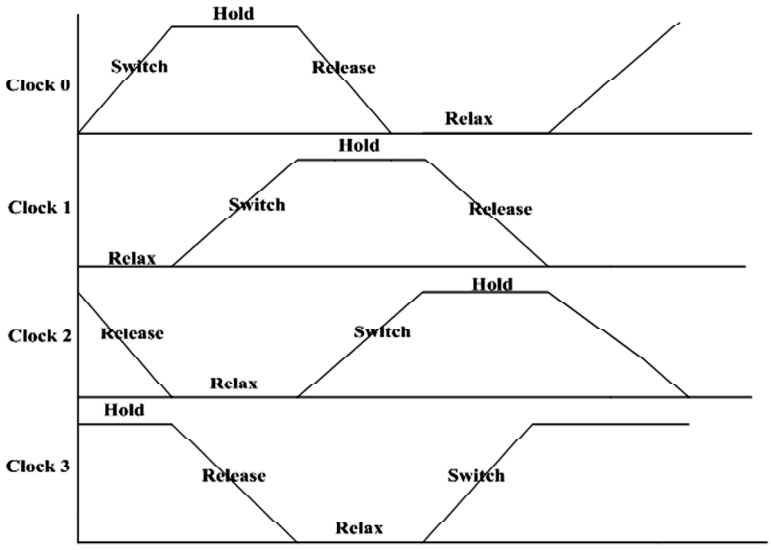


Figure 7: Four clock zones in QCA

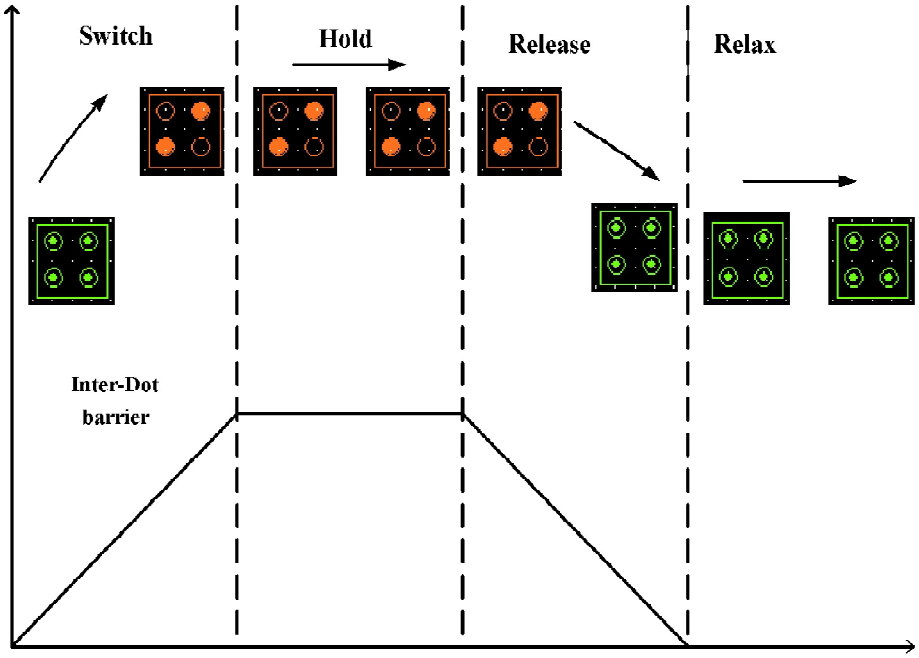


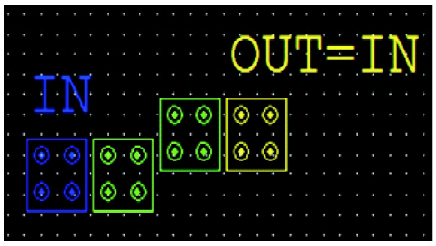
Figure 8: QCA cell behaviour with clock phase

3. LOGIC GATES IN QCA

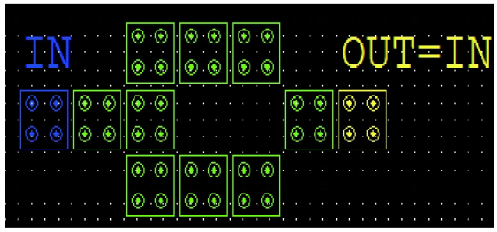
The logic gates are created by specific arrangement of QCA cells. The basic gates in this technology are inverter and majority gate.

3.1. QCA Inverter

Figure 9 shows two ways of creating inverters. In Figure (a), the inverter uses only two cells which are displaced with respect to each other. Figure (b) shows a different type of inverter which is bigger in size but is more robust when compared of two-cell inverter.



(a) Simpler (2-cell) inverter

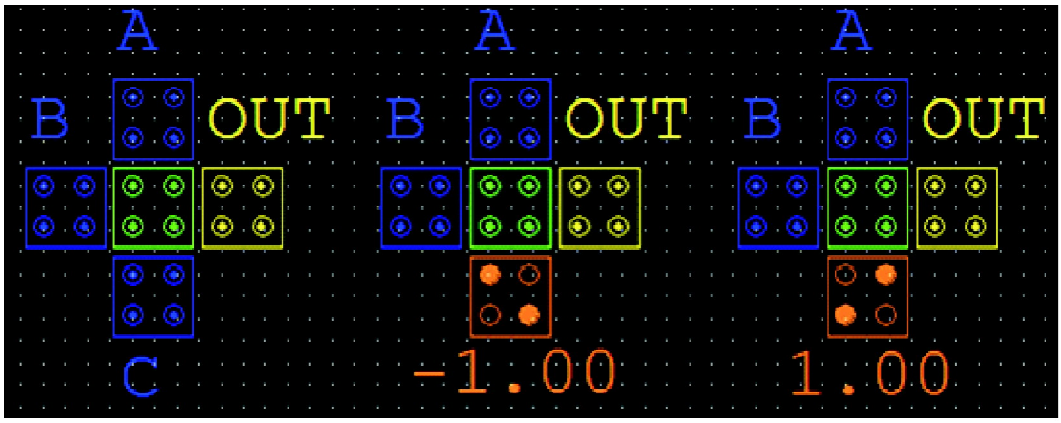


(b) Larger inverter

Figure 9: Types of QCA inverters

3.2. Majority, AND & OR Gates

The majority gate is illustrated in Figure-10. The output F is defined as F = AB+AC+BC. The output F can be propagated using a QCA wire which can then act as an input to other gates. The majority gate is used to build AND and OR gates by making the inputs to 0/1, the result will be AND/OR of remaining two inputs.



(a) Majority gate **(b) AND gate** **(c) OR gate**

Figure 10: QCA Majority, AND, OR gates

3.3. Universal Gates

Other than AND, OR, and NOT gates, NAND and NOR are also used for designing digital circuits. The NAND and NOR gates are called universal gates. A universal gates are used implement any Boolean function without the use any other gate.

NAND Gate

The complement form of AND operation is said to be NAND. It is an abbreviation of NOT AND.

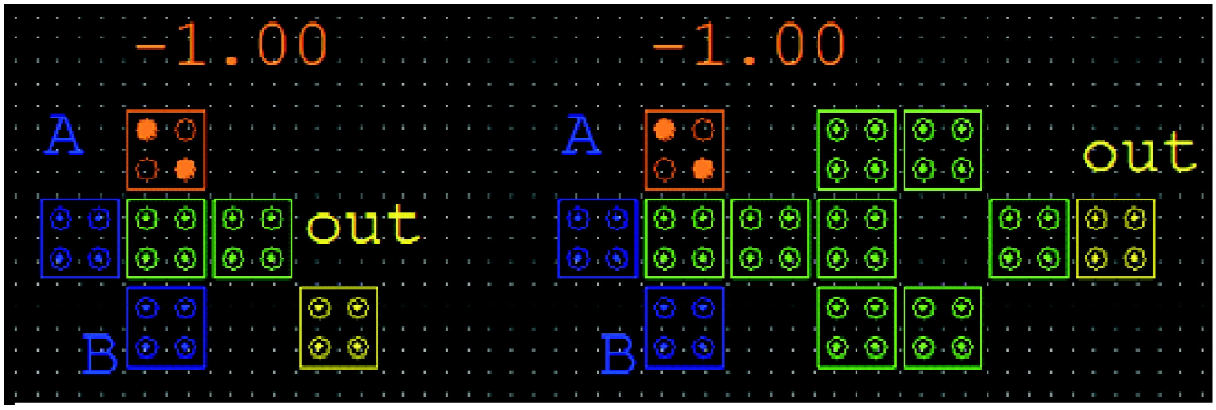


Figure 11: QCA NAND gate

NOR Gate

The complement form of OR operation is said to be NOR. It is an abbreviation of NOT OR.

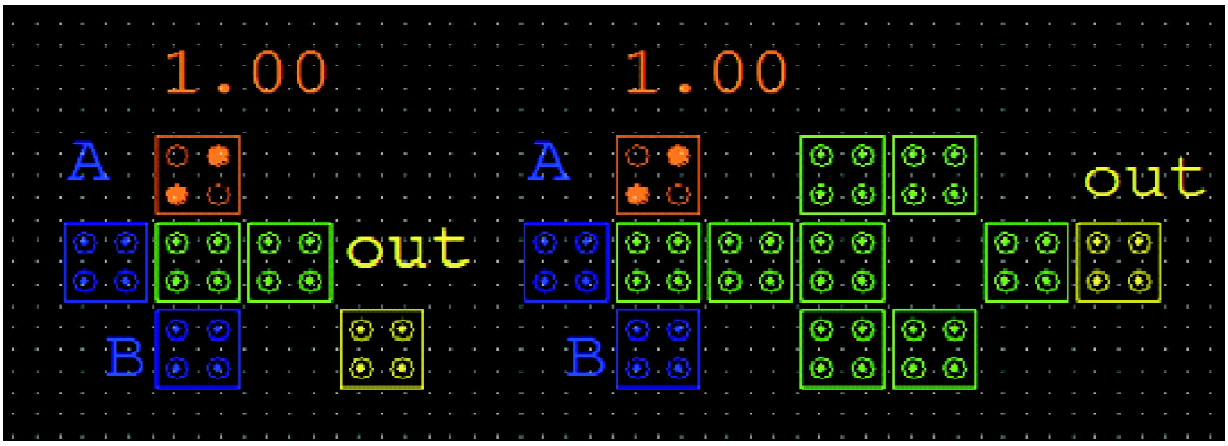


Figure 12: QCA NOR gate

4. DESIGNS USING QCA

4.1. HALF ADDER

Half adder is a combinational arithmetic circuit which adds two numbers and produces a sum bit (S) and carry bit (C) as the output. Half adder is the simplest of all adder circuit, but uses only two input bits (A and B).

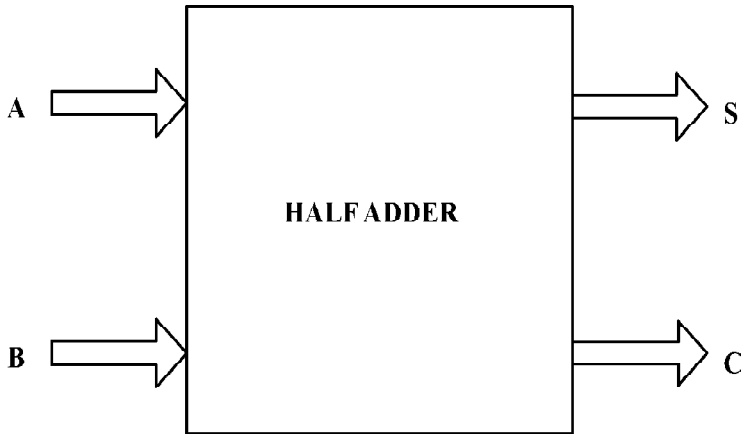


Figure 13: Half adder schematic

Table 1
Half Adder Truth table

INPUT		*OUTPUT*	
A	*B*	*S*	*C*
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Logic Expression

SUM S = A ⊕ B

CARRY C = AB

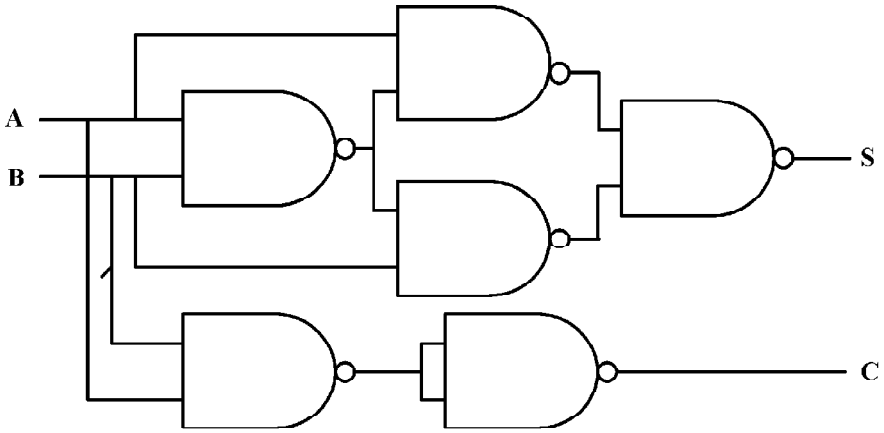
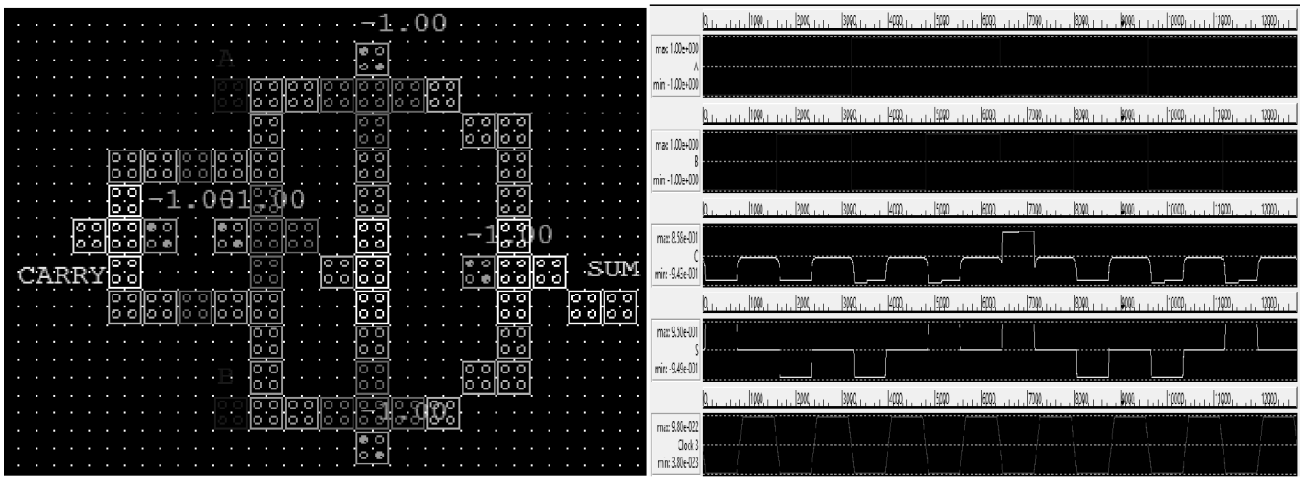


Figure 14: Half adder logic diagram



(a)QCA Half adder **(b) Simulation results of QCA Half adder**

Figure 15: QCA Half adder and its waveforms

Table II
Half Adder Design- Area and Number of Cells

Cell count	62
Area (μm²)	0.08

B. Half Subtractor

The half subtractor performs the subtraction of two bits. It has two inputs, the minuend A and subtrahend B and two outputs the difference D and borrow out B_{out}.

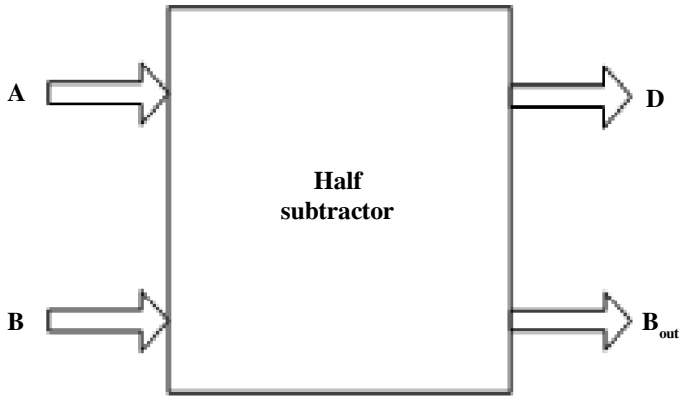


Figure 16: Half subtractor schematic

Table 3
Half subtractor truth table

Input		*Output*	
A	*B*	*D*	B_{out}
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Logic Expression

D = A ⊕ B

Bout = $\overline{A}$. B

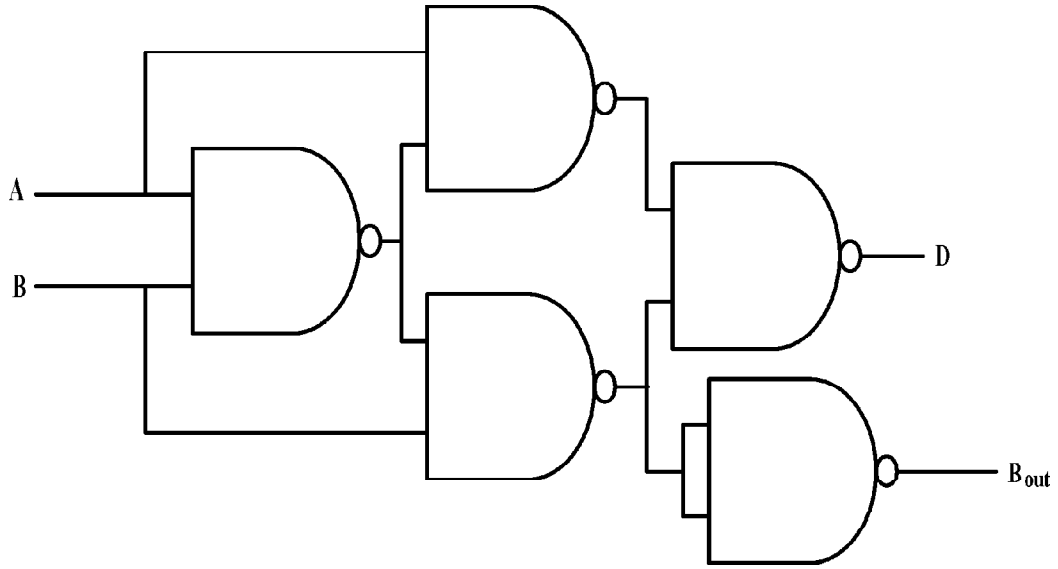
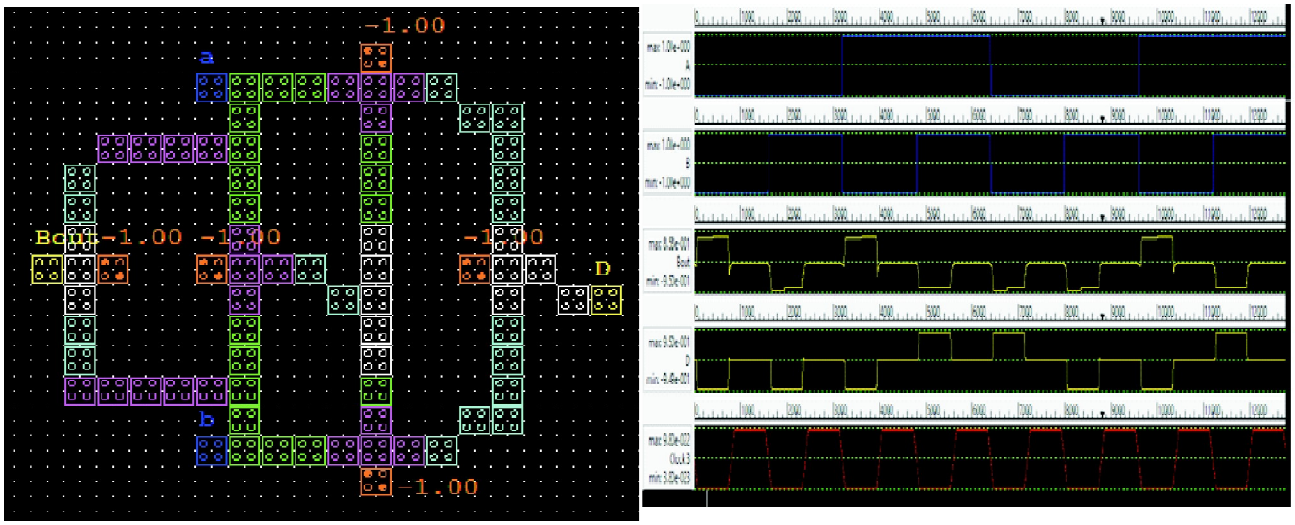


Figure 16: Half subtractor logic diagram



(a) QCA Half subtractor (b)Simulation results of QCA half subtractor

Figure 17: QCA Half subtractor and its waveforms

Table 4
Half Subtractor Design- Area and Number of Cells

Cell count	79
Area (μm^2)	0.12

C. Multiplexer

A Multiplexer (or mux) is a device that selects one of several input signals and send to the selected input into a single line. A multiplexer of 2^n inputs has n select lines, used to select which input line to send to the output.

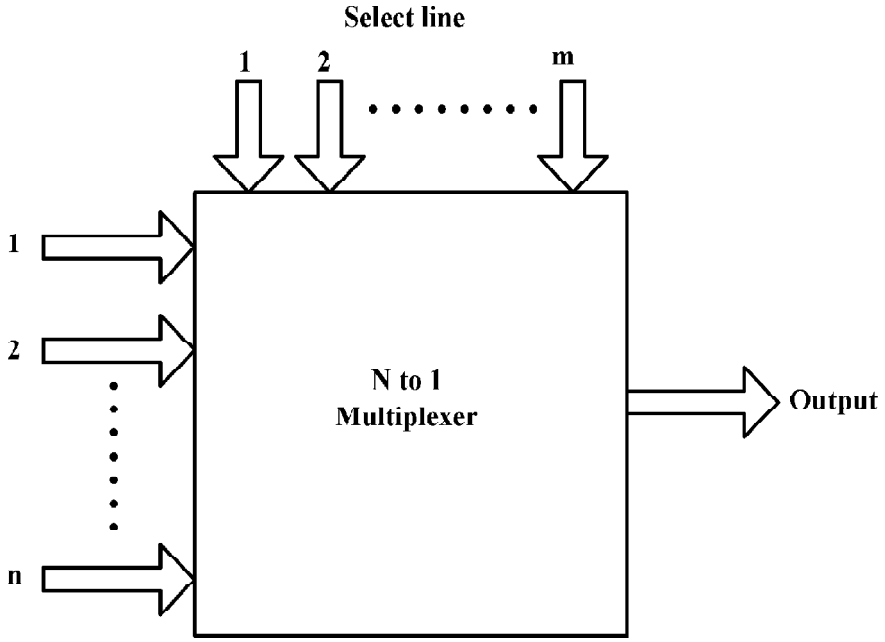


Figure 18: Multiplexer Basic configuration

1.2. Input Multiplexer Design

The 2-input multiplexer connects one of two 1-bit sources to an output, producing a 2-to-1-line multiplexer and Boolean expression for 2-input multiplexer circuit is

$Y = A.I_1 + A.I_0$

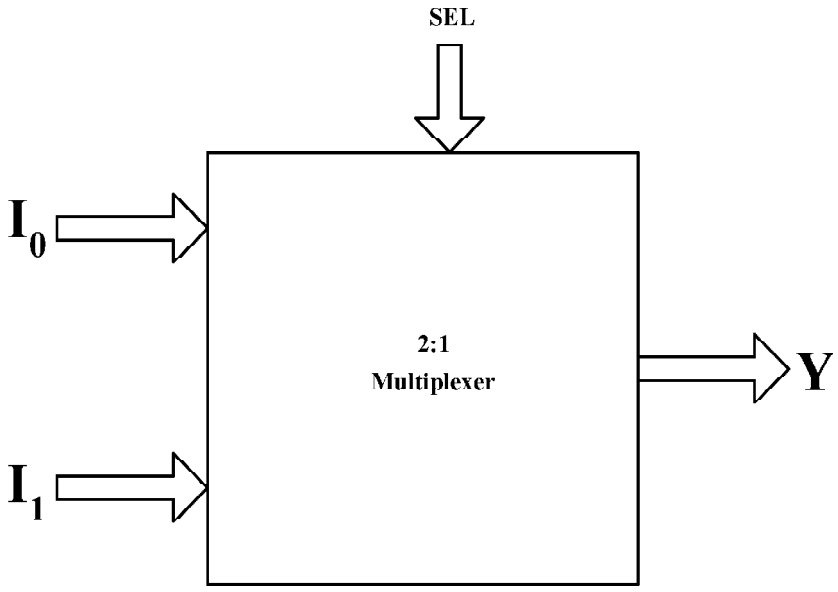


Figure 19: Multiplexer schematic

Table 5
2:1 Multiplexer truth table

Input			*Output*
SEL	I_0	I_1	*Y*
0	0	0	0
0	0	1	0
1	1	0	0
1	1	1	1

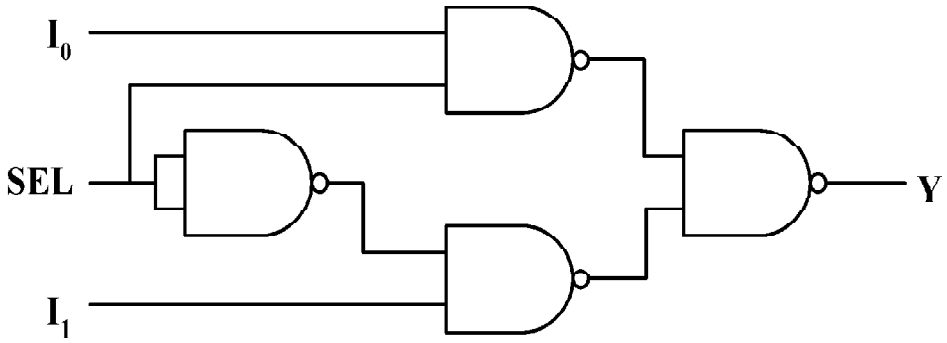
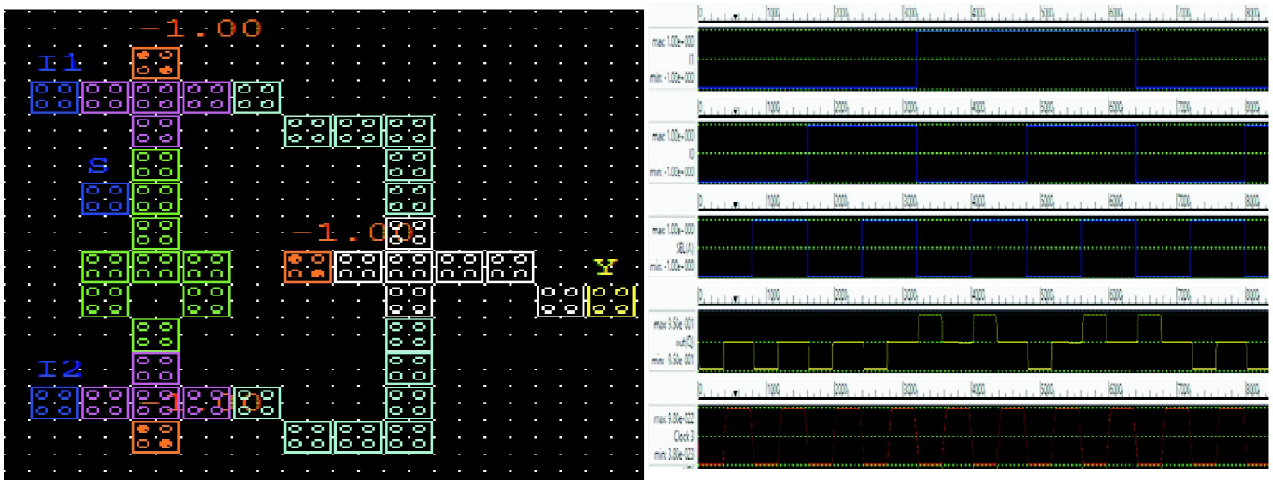


Figure 20: Multiplexer logic diagram

Logic Expression

$Y = I_0\overline{S} + I_1 S$



(a)QCA 2:1 Multiplexer (b)QCA Multiplexer simulation results

Figure 21: QCA Multiplexer and its waveforms

Table 6
Multiplexer Design-Area and Number of Cells

Cell count	44
Area (μm^2)	0.06

4. DEMULTIPLEXER

Demultiplexer is also said to be data distributor, because which is received at the input to different destinations when they transmit same data. Thus, it is a 1-to-N device. It has 1 input, n number of output and m control lines. In this, m control lines are required to produce 2m possible output lines (consider 2m = n).

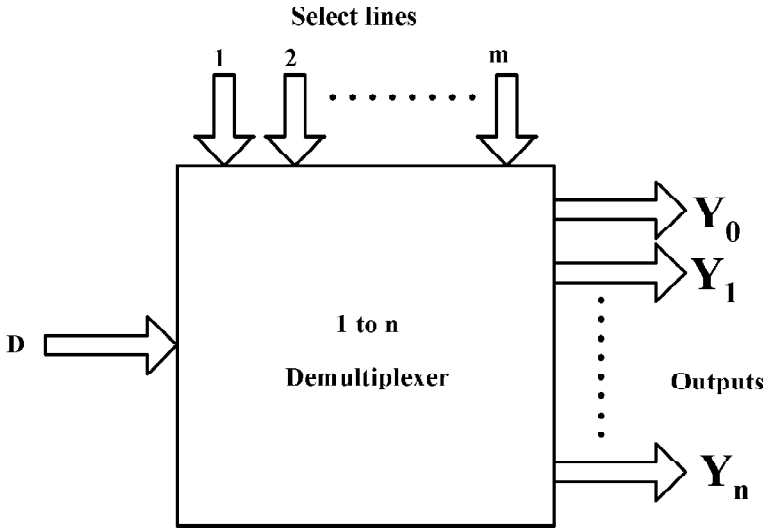


Figure 22: Demultiplexer schematic

1.2. Demultiplexer

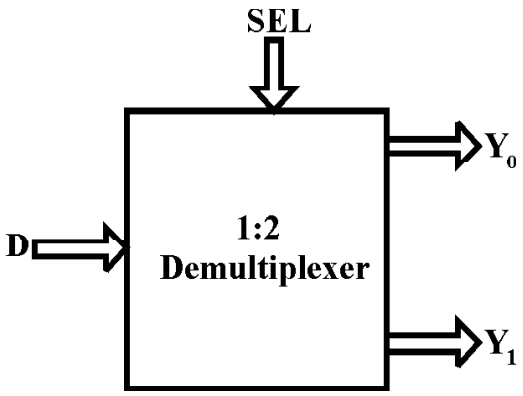


Figure 23: Demultiplexer schematic

Table 7
Demultiplexer truth table

Select	*Input*	*Output*	
S	*D*	Y_0	Y_1
0	0	0	0
0	1	0	1
1	0	0	0
1	1	1	0

Logic Expression

$Y_0 = D\overline{S}$

$Y_1 = DS$

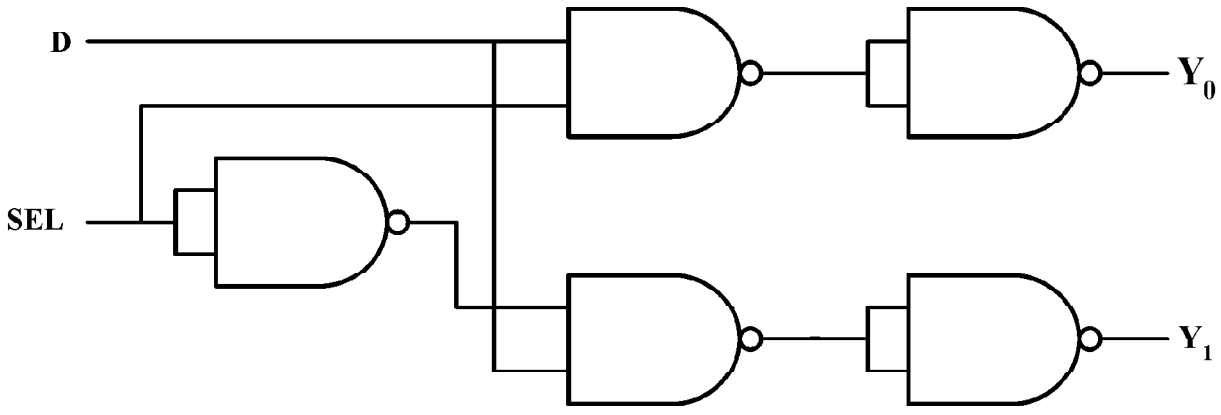
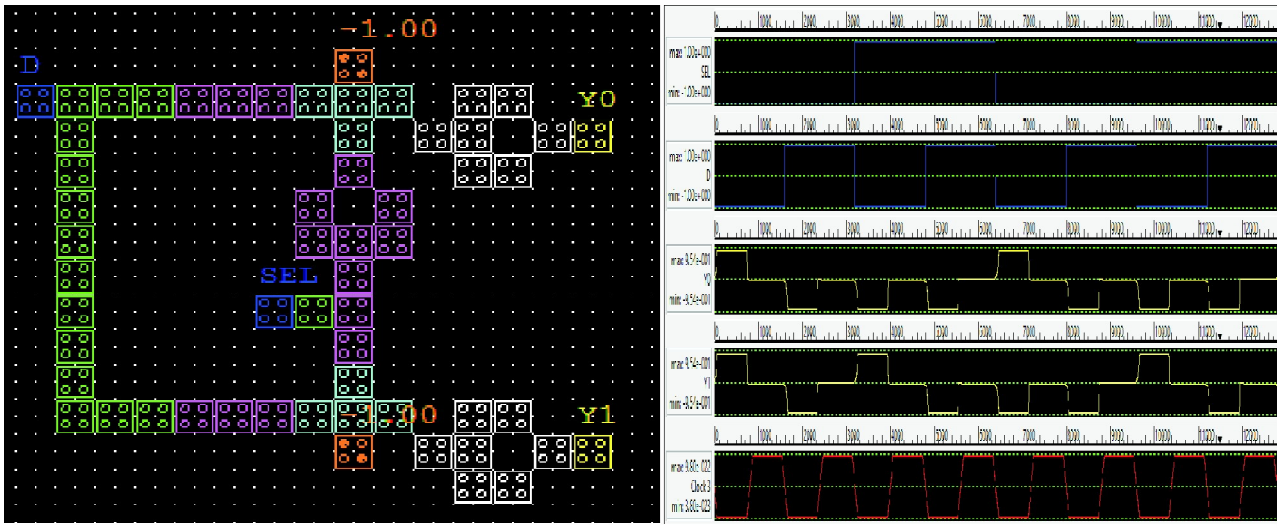


Figure 24: Demultiplexer Logic Diagram



(a) QCA 1:2 Demultiplexer (b) QCA 1:2 Demultiplexer Simulation

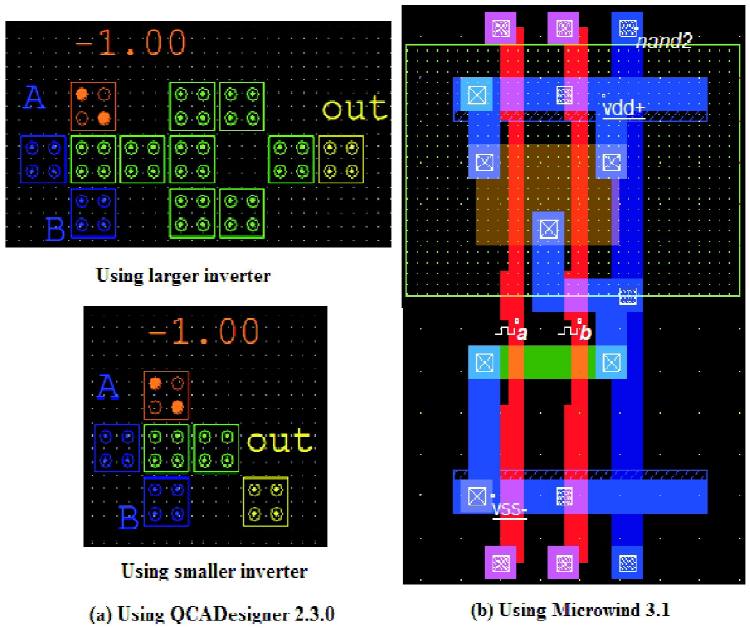
Figure 25: QCA 1:2 Demultiplexer and its waveform

Table 8
1:2 Demultiplexer design- Area, and Number of cells

Cell count	58
Area (μm²)	0.09

5. COMPARISON OF NAND LAYOUT

NAND layout was designed in QCADesigner 2.3.0 and its area was compared by designing in Microwind 3.1 (CMOS Technology).



(a) Using QCADesigner 2.3.0 (b) Using Microwind 3.1

Figure 26: NAND LAYOUT

Table 9
Area Comparison table- QCADesigner and Microwind

Layout	*QCADesigner 2.3.0*		
	Using smaller inverter	*Using larger inverter*	*Microwind 3.1*
NAND	*6318.00nm² = 0.01 μm²*	*11178.00nm² = 0.01 μm²*	*1.900 × 1.700 μm² = 3.23 μm²*

6. CONCLUSION

Thus, the basic combinational circuits like Half adder, Half subtractor, Multiplexer and Demultiplexer using NAND logic was designed. The layout was designed and the functionality of those combinational circuits was verified using QCADesigner tool version 2.3.0 and total area of NAND gate is compared by designing in QCADesigner 2.3.0 and Microwind 3.1 (CMOS technology).

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