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Design of a Flip-Flop to make it Metastable-Hardened by Varying Its Architecture

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ABSTRACT

Continuous scaling down of technology is causing reliability issues such as Metastability in flip flop designs. Metastability, where the system enters into an undesired state other than '0' and '1' is of great concern as this can cause complete system failure. There are many remedies for this issue out of which a metastable-hardened flip-flop is an area which is less researched on. This paper aims at designing and analyzing various simulations and designs for a metastable-hardened flip-flop. The design of Power PC flip-flop to make it metastable-hardened by varying its architecture is discussed here. The design also focuses on the trade-off between power and delay. All the designs are done using CADENCE Virtuoso tool in 0.18μm.

Keywords: Cadence Virtuoso tool, D-flip flop, Metastability, Metastable-hardened flip-flop

1. INTRODUCTION

Scaling down of CMOS technology is the current trend in VLSI design. This downscaling is causing reliability issues such as Metastability in flip-flops. Metastability [1] is a phenomenon where a bi-stable element enters an undesirable third state in which the output is stuck at an intermediate level between logic 0 and 1. Metastability is an issue not only in asynchronous systems but also in synchronous systems, as there are two inputs, data D and the CLK signal. These two inputs, D and CLK potentially can make simultaneous transitions which can violate the flip-flop setup and hold time constraints which lead to a metastable output. In this case of Metastability, the flip-flop output takes an unbounded amount of time to settle to a stable state or it even oscillates several times before settling to a stable state.

Flip-flop Metastability [2] can cause corruption of data, as the state is not stable and this value can be used by another circuit. The ability of a circuit to resolve from a metastable state is extremely important as it prevents the correct functionality of the handshaking protocol in asynchronous systems, or propagating from one stage to another in the pipeline systems would results in complete system failures. The famous Moore's Law describes that, the scaling down of transistors into minimum dimensions enables a large number of them integrated on to a single chip. Along with that the continuous push for higher clock rates which in-turn results in tighter timing budgets makes the flip-flops [5, 7] more susceptible to metastable outputs. While numerous studies have been performed on the remedies for Metastability [3, 4], the design for a metastable-hardened flip-flop has largely been missing in the literature. Therefore, Metastability and metastable-hardened flip-fops are becoming an important design consideration for flip-flop designs.

2. METASTABILITY

Metastability in digital electronics is similar but not hypothetical as Buridan's ass [6], which is an illustration of paradox in philosophy. In 1984, American computer scientist Leslie Lamport calls this "Buridan's

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principle": A discrete decision based upon an input having a continuous range of values cannot be made within a bounded length of time when a circuit must decide between two states when there is an input that is changing value. And this will go hand in hand with digital Metastability as downscaling is trending in a faster pace. Richard Feynman once said that "Nearly everything is really interesting if you go into it deeply enough". It is true for Metastability where even synchronous systems are victims of it when technology scales down.

Metastability is a phenomenon where a bi-stable element enters an undesirable third state in which the output is at an intermediate level between logic '0' and '1'. Flip-flops enters the Metastable region when they violate the setup or hold time constraints i.e., when the input data D makes a transition within $t_{aperture}$ as shown in the Fig. 1.

3. METASTABILITY MODELING IN A CROSS COUPLED INVERTER PAIR

A typical master-slave flip-flop consists of two identical latches, which are used for the illustration of Metastability theories as shown in Fig. 2 [4, 8]. The switches shown in the figure are implemented using CLK-controlled transmission gates in practice. When the latch is transparent, the sample switch is closed

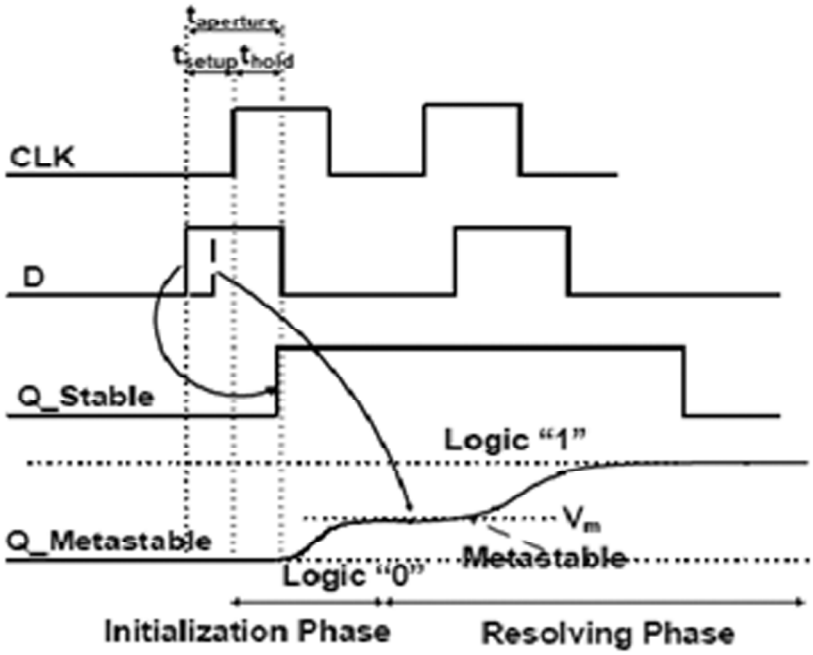

Figure 1: Illustration of Metastability using Timing Waveforms

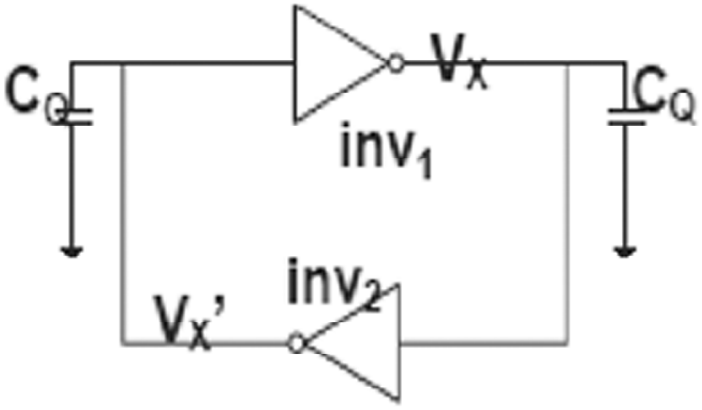

Figure 2: Schematic of cross-coupled inverter pair

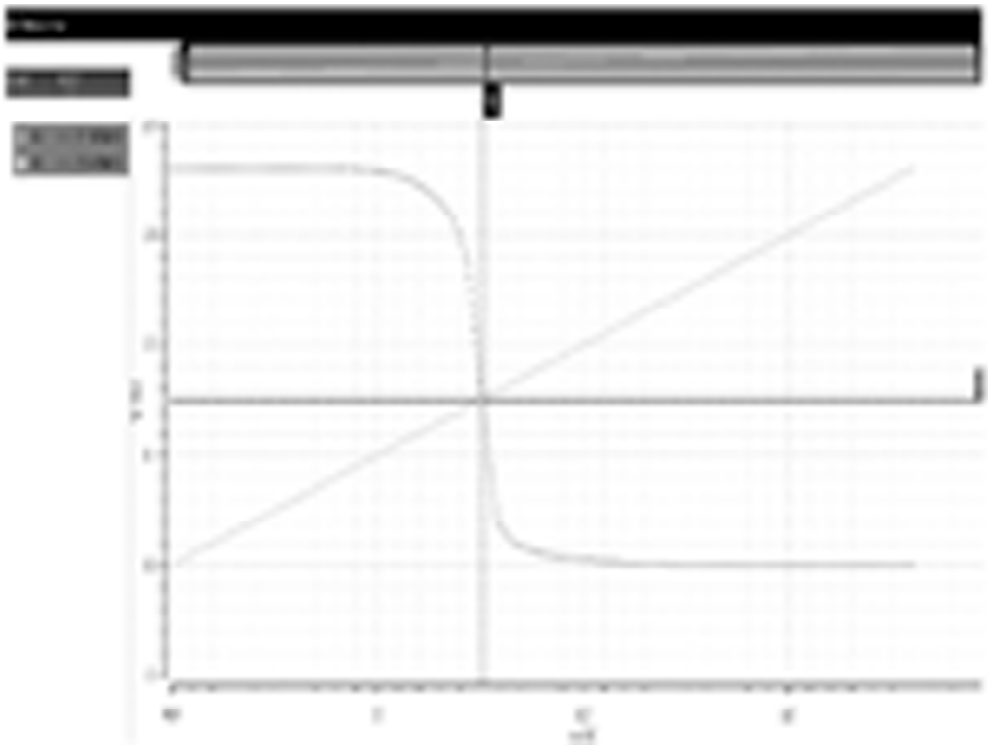

Figure 3: Voltage Transfer Curve of cross-coupled inverter

and the hold switch open. When the latch becomes opaque, the sample switch opens and the hold switch closes. When the latch is opaque, $V_x = V_x'$ and maintains a stable state of either logic 0 or logic 1. During the voltage transfer, both V_x and V_x' can reach the metastable state of V_m, which is an illegal state somewhere between logic 0 and logic 1. This point is called Metastable because the voltages are self-consistent and can remain there indefinitely.

The analysis of a cross-coupled inverter can be incorporated into the design of metastable hardened flip-flops because all the dynamic/critical nodes are stabilized by some form of cross-coupled inverter pair. For that a cross-coupled inverter pair is designed using CADENCE design tool (Fig.2). The resulting DC transfer characteristic curve of the two inverters is plotted as shown in Fig.3 and Voltage Transfer function (VTC) was obtained.

4. POWERPC FLIP-FLOP

The Power PCFF [9] is a transmission-gate based classical master-slave structure with low power consumption and reasonable performance. Its advantages are a short direct path and low-power feedback. It is a combination of Transmission Gate Master Slave flip-flop and mC^2MOS flip-flop. The feedback transmission gate is changed with a clocked inverter. The critical node marked by "X", right after the input transmission-gate in the master-stage, is stabilized by a CLK-controlled feedback inverter and a forward inverter in the critical path. The schematic diagram of a PowerPC flip flop is shown in Fig.4.

5. MODIFIED POWERPC FLIP-FLOP

The Metastability in Power PCFF can be mitigated by varying the architecture of Power PCFF i.e., the PN inverter pair which is shown using red selection in Fig.4. The variation in architecture is done in both master and slave stages. The new architecture styles are used to replace the selected part to make it metastable-hardened.

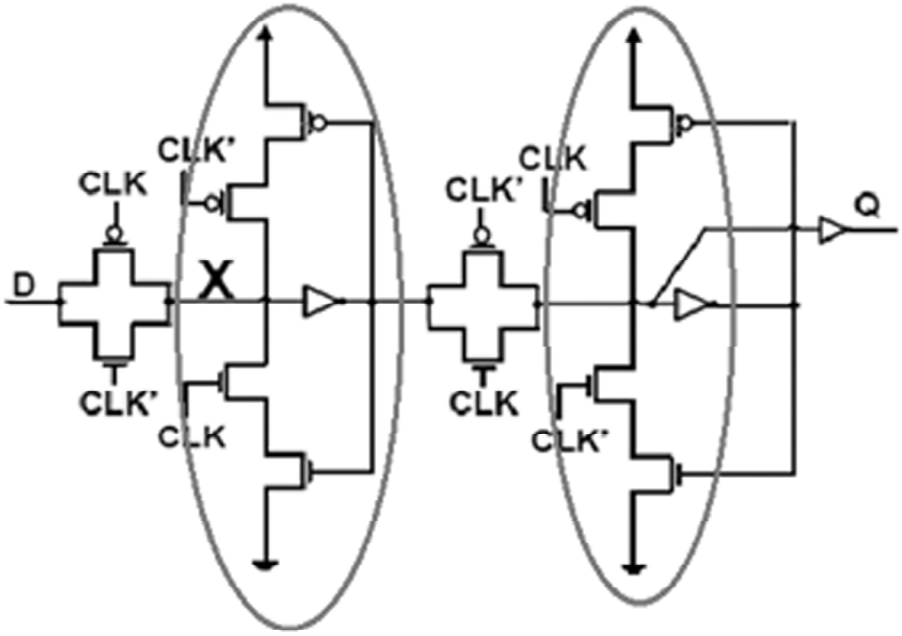

Figure 4: Schematic of a PowerPC flip-flop

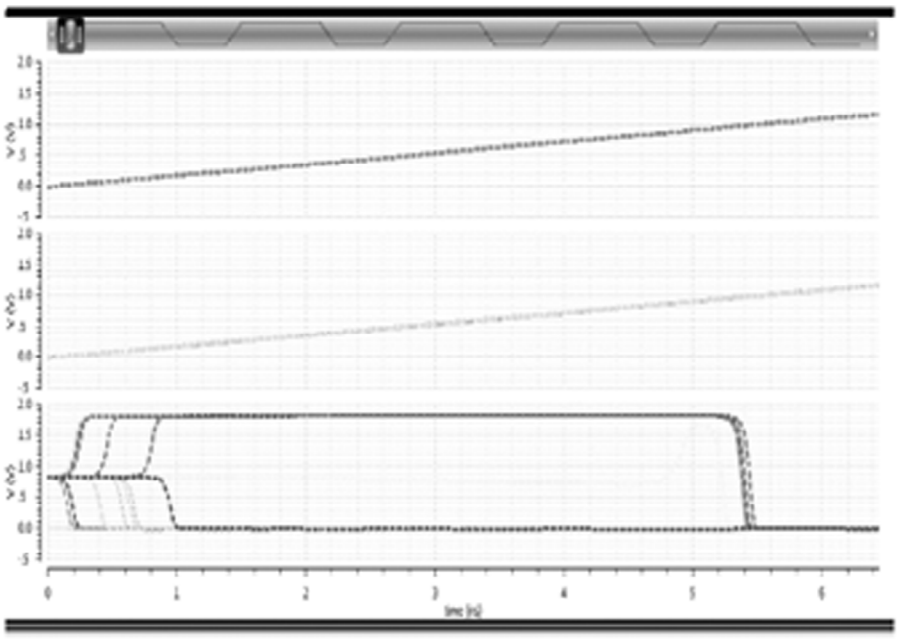

Figure 5: Transient response of PowerPC flip-flop

5.1. Architecture 1- Domino CMOS Inverter + TG (M1-Power PCFF)

Metastability in the Flip-Flop structure which was fully static is mitigated when the part of it is replaced with a dynamic one. The variation in the architecture thus contributed to the correct working of the flip-flop. CMOS Domino logic [10, 12] is the architecture used to correct the Metastability error here.

The schematic diagram of this flip-flop was drawn in CADENCE schematic editor and analysis were done in Analog Design Environment L. Metastability modeling of PowerPC flip-flop was done by delaying the input signal.

The transient response of modified PowerPC flip-flop (M1-Power PCFF) is shown in Fig. 7.

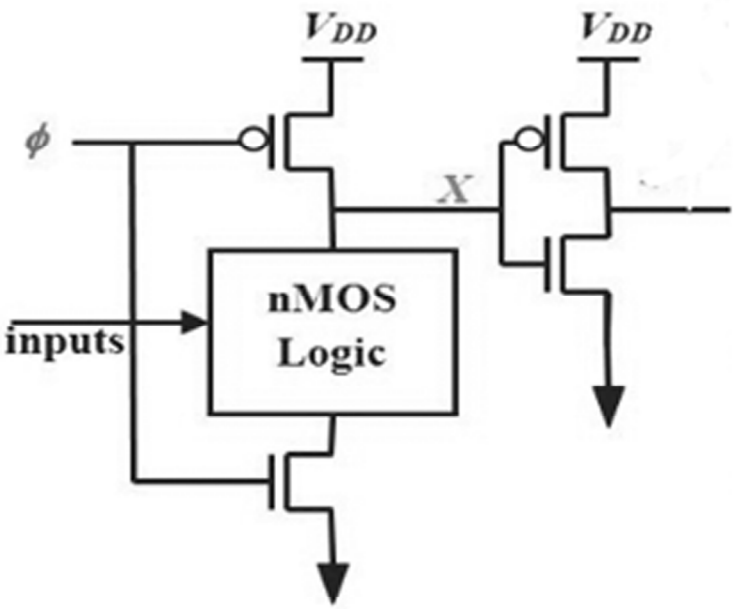

Figure 6: CMOS DOMINO logic (in M1 Power PCFF)

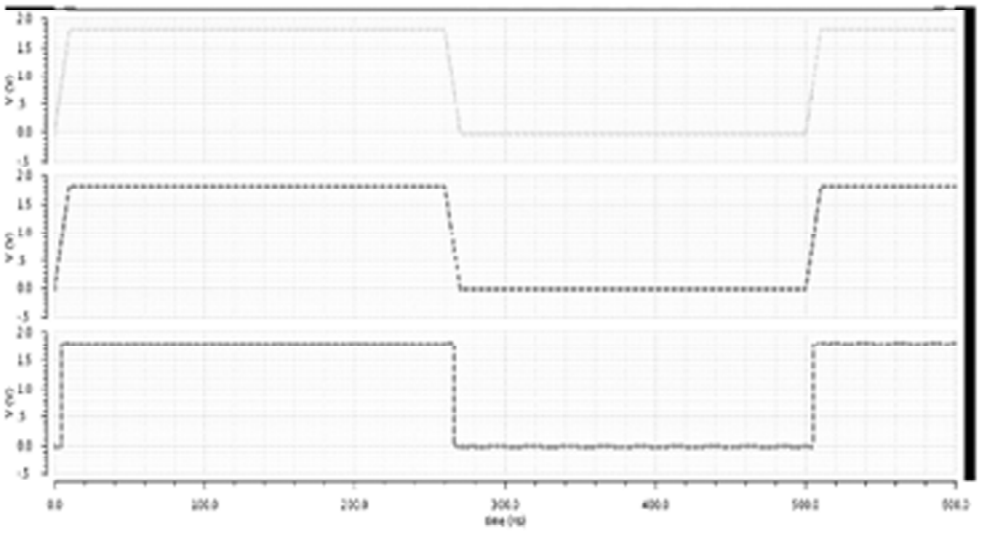

Figure 7: Transient response of M1-Power PCFF

5.2. Architecture 2- Pseudo NMOS Inverter + TG (M2-Power PCFF)

Metastability in the Flip-Flop structure which was fully static is mitigated when the part of it is replaced with another static one. The variation in the architecture thus contributed to the correct working of the flip-flop i.e. metastable-hardened one. Pseudo-NMOS logic [11, 12] is the architecture used to correct the Metastability error here. The power, delay and PDP of the new design were also found out.

6. RESULTS

The design of PowerPC was analyzed and Power and Delay was obtained. From the results shown in Table.1, we can see that Power of the modified structure increased as delay of it got reduced. Delay of the M1-Power PCFF got reduced by 9.69 times whereas the delay of M2-Power PCFF is showing a 101 times decrement in the delay than the original Power PCFF. Power-delay product of architecture 1 (M1-Power PCFF) was found out to be about 5.5 times that of PowerPC original structure. But the power-delay product of architecture 2(M2-Power PCFF) was found out to be 2.1 times that of the original structure.

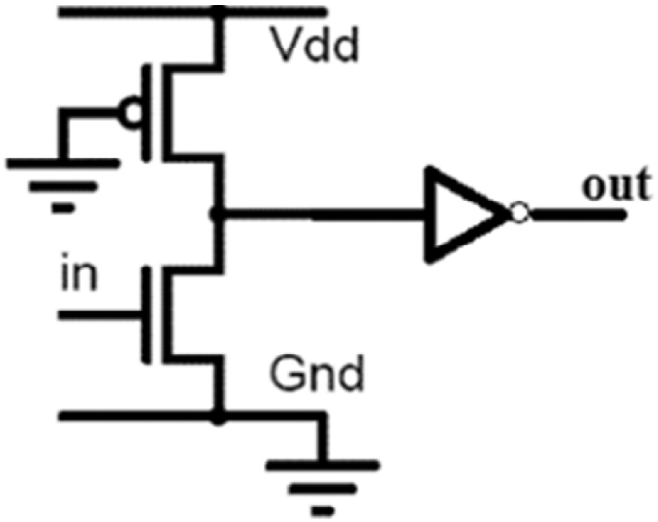

Figure 8: PSEUDO-NMOS logic (in M2-Power PCFF)

Table 1
Power and Delay Analysis of Power PCFLIP-FLOP

STRUCTURE	POWER(μW)	DELAY(PS)	PDP(J)
Power PCFF(original)	2.077	84.529	175.56e-18
M1-Power PCFF	112	8.715	976.1e-18
M2-Power PCFF	441	0.836	369.3e-18

7. CONCLUSION

The work presented in this paper attempts to increase the reliable operation of the flip-flops by incorporating soft-error mitigation techniques into the design of Metastable-hardened flip-flops. The main design approach is to resolve Metastability in the master-stage with a cross-coupled inverter pair in the critical path using two architecture designs. PowerPC flip-flop is designed and a modification in architecture was made to mitigate the timing errors. From the analysis on PowerPC structures, it is found out that the power-delay product (PDP) of architecture 1(M1-Power PCFF) is 5.5 times that of PowerPC original structure. But the power-delay product of architecture 2(M2-Power PCFF) was found out to be 2.1 times that of the original structure. After comparing the two designs it is found that the PDP OF M1-Power PCFF is 2.64 times that of M2-Power PCFF.

REFERENCES

[1] P. Freidin, "FPGA-FAQ 0017: Tell Me About Metastability."http://www.fpgafaq.com/FAQ_Pages/0017_Tell_me_about_metastables.htm/, 2005. [Online; accessed 19-September-2015].

[2] D.Tala,"What is Metastability." http://resalpes.grenoble.cnrs.fr/tutorat/vhdl_altera/divers/metastablity.html/, 2005. [Online; accessed 19-September-2015]

[3] I.Clark, "Metastability Bibliography." http://iangclark.net/metastability.html/, 2008.[Online; accessed 20-September-2015]

[4] D. Li, Design and Analysis of Metastable-Hardened, High-Performance, Low-PowerFlip-Flops. PhD thesis, University of Waterloo, 2011.

[5] O. S. Unsal, J. W. Tschanz, K. Bowman, V. De, X. Vera, A. Gonzalez, and O. Ergin,"Impact of parameter variations on circuits and microarchitecture," Ieee Micro, no. 6,pp. 30–39, 2006.

[6] "Buridan's ass."https://en.wikipedia.org/wiki/Buridan%27s_ass/, 2015. [Online; accessed 15-Decemberr-2015].

[7] H. Unger et al., "Clocking schemes for high-speed digital systems," IEEE transactions on computers, no. 10, pp. 880–895, 1986.

[8] S. T. Oskuii, "Comparative study on low-power high-performance flip-flops," 2004.

[9] Stojanovic, Vladimir, and Vojin G. Oklobdzija. "Comparative analysis of master-slave latches and flip-flops for high-performance and low-power systems." *Solid-State Circuits, IEEE Journal of* 34.4 (1999): 536-548.

[10] Pretorius, Jacobus A., Alex S. Shubat, and C. Andre T. Salama. "Charge redistribution and noise margins in domino CMOS logic." *Circuits and Systems, IEEE Transactions on* 33.8 (1986): 786-793.

[11] Forbes, Leonard. "Monotonic dynamic-static pseudo-NMOS logic circuit." U.S. Patent No. 6,801,056. 5 Oct. 2004.

[12] Weste, Neil HE, and Kamran Eshraghian. *Principles of CMOS VLSI design*. Vol. 188. New York: Addison-Wesley, 1985.