IJCTA, 8(4), 2015, pp. 1539-1552
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Design and implementation of Single phase Quasi ZSI DC-DC Converters Based on Voltage Doubler Rectifier

S. Malathi* & S. Chandramohan**

Abstract: The Z-source inverters are current topological alternatives proposed for buck–boost energy conversion with a number of possible currentand voltage--type circuits. This paper presents a novel single-phase DC-DC converter topologyforenhancing efficiencyand decreasing ripple in the output,the topology comprises of quasi Z source inverter withtwo capacitors,one diode, two inductors for sustaining continuous current and reducing energy losses in the output, a single phase isolation transformer, and a voltage doubler rectifier (VDR).There are two operating modes:non-shoot through (NST) modes (or) active mode and shoot-through (ST). Pulse Width Modulation (PWM) with duty cycle ratio control scheme is utilizedin this for controlling quasi ZSI (impedance source inverter).Byemploying the Simple boost control scheme of shoot- through technique in quasi ZSI (impedance source inverter), component stresses and voltage boost factor are significantly reduced when contrasted with the conventional method.

Keywords: Pulse Width Modulation (PWM), full-bridge converter,shoot through technique, Impedance Source Inverter (ZSI).

1. INTRODUCTION

To acquire high efficiency and less losses, the input LC circuit is utilized to decrease the harmonic pollution and so that the efficiency of the converter get improved [1].The quasi Z (impedance) source is capableof working in both modes such as current fed mode ZCS (Zero Current Switching) and voltage mode called ZVS (Zero Voltage Switching).Based on the mode of operation the quasi Z (impedance) source inverter can be used for boost or buck operation. The consistency of QZSI (Quasi Impedance Source Inverter) is high due to low inrush current and shoot-through capability. These inverters are extensively utilized in high voltage gain such as renewable energy systems or motor controllers. By employing shoot through technique, it is possible to make conduction of phase switches of same leg [2] – [7].

Fig. 1(a) shows ZVS (Zero Voltage Switching) dc-dc converter with single transformer. In this,phase controlled Pulse Width Modulation (PWM) techniqueis utilized for controlling the MOSFET switches S_1-S_4 so as to function in zero voltage switching. The diode across the MOSFET switches S_1-S_4 control the current flow in the single direction.Moreover, the intrinsic diodes in this serve as freewheeling diode for switches. Generally, theconcept of ZVS/ZCS is realized to evade the reverse recovery ofMOSFET with diode. Thus to minimize MOSFET recovery problems the circuit in fig. 1(b) is used. In this active power is transformed to output by freewheeling effect of inductor [8], [9]. So, it can be used for high power and high voltage applications. The magnetising energy in this cannot be reversed due to rise of the series diodes and conduction loss in phase leg.

Thus in Fig.1 (c), the active switches are removed and leakage losses are decreased due to additional transformer TR2 which is in reliant of output current and shifted phase angle. The transformer at the primary side is shorted with switches S1 and S3 or S2 and S4. Here, circulating current is produced and conduction loss gets increased [10].

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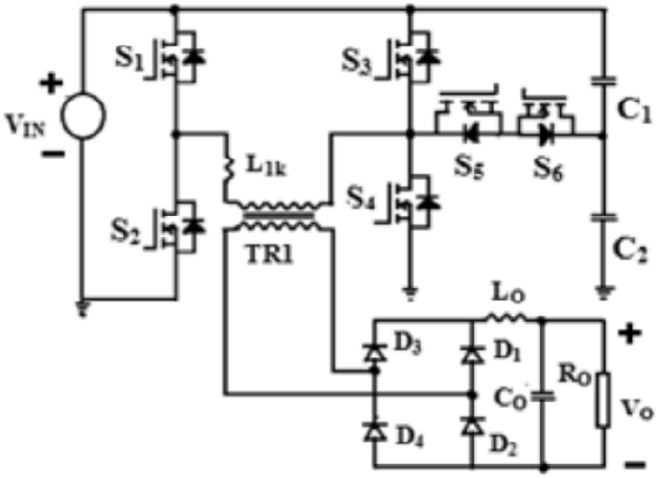
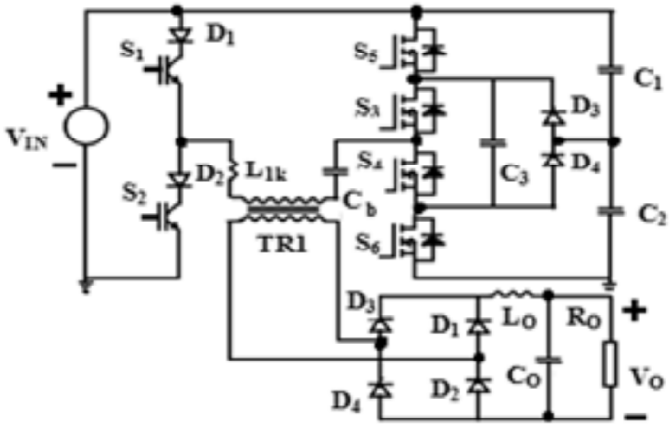
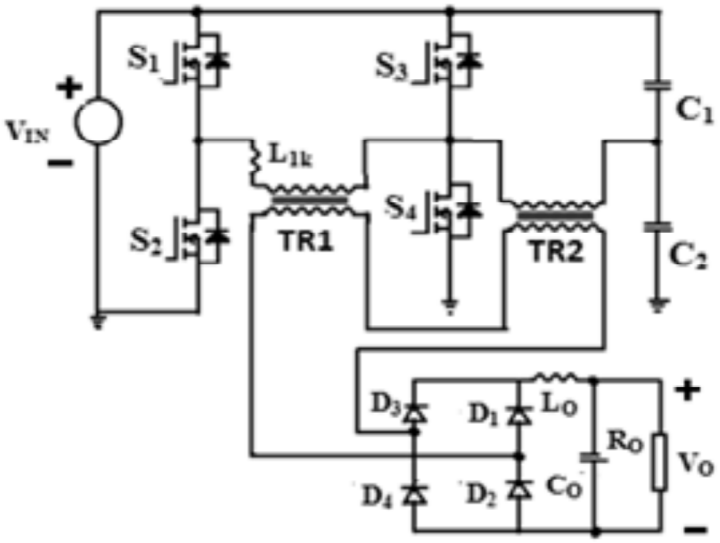


(a) ZVS with single transformer



(b) ZVZCS with single transformer



(c) ZVS with two transformers

Figure 1: Hybrid half- and full-bridge converters

2. RELATED WORK

Fang et.al [11], proposed the Z-source idea could be connected to all dc-to-dc, dc-to-ac, ac-to-dc and ac-to-ac power change. To describe the working rule and control, this paper concentrates on a case: a Z-source inverter for dc-ac power conversion required in cell of fuel requisitions. The Z-source converter utilizes a novel impedance network (or circuit) to combine the converter main circuit to the power source, subsequently giving extraordinary characteristics that can't be acquired in the customary current-source (or current-fed)) and voltage-source (or voltage-fedconverters where a inductor and capacitor are utilized, separately. The Z-source converter beats the applied and hypothetical hindrances and impediments of the traditional current-source and voltage-source converter.

Poh Chiang et.al [12], exhibits a complete examination, indicating how different conventional pulse-width modulation techniques might be changed to switch a voltage-type –z-source inverter either consistently or irregularly, while holding all the special harmonic execution characteristics of these conventional modulation methods. This paper begins by investigating the modulation necessities of a single-phase H-bridge -source inverter, and subsequently extends the analysis to cover the more complex four-phase-leg –Z-source and three-phase-leg inverters.

Poh Chiang et.al [12],[13], For dc dissection, both signal-flow-graph and small-signal strategies are utilized with a proposition of creating an extensive guide on Z-source impedance modelling. A characteristic uncovered by

both demonstrating systems is that the Z-source network has a RHP zero in its control-to-output exchange function, bringing about the dc-link voltages having a non-minimum-phase reaction. Non-minimum-phase response is additionally ended up being in presence through vectorial investigation on the inverter ac-side when PWM state succession with consistent (or zero) invalid interim is utilized. This ac reaction with an introductory dip and slower climb time could be enhanced by utilizing PWM arrangement with a variable padding invalid interim and continuous tuning of dynamic interim, as demonstrated.

Sok Wei Lim et. al [14], introduces the outline and control of two three-level Z-source inverters, whose output voltage could be ventures up or down utilizing just a solitary impedance system associated between the dc information source and either an neutral-point-clamped (NPC) or dc-link fell inverter circuitry. Through careful design of their modulation scheme, both inverters can work with the base of six gadget commutations per half carrier cycle, while preparing the right volt-sec normal and inductive voltage boosting at their ac output terminals. Physically, the designed modulation scheme can conveniently be implemented utilizing a nonexclusive "alternative phase opposition disposition" carrier-based modulator with the fitting triple counterbalance and time development/delay included.

FengGao et.al [15], Shows this impedance network permits the yield end of a voltage-type Z-source inverter to be shorted for voltage boosting withoutringing on an extensive current stream and the terminal current of a current-type inverter to be hindered for current boosting without acquaintingover voltage motions with the framework. In this manner, Z-source inverters are more secure and less unpredictable and might be actualized utilizing just passive components with no extra dynamic semiconductor required. Having confidence in the possibilities of Z-source inverters, this paper helps by presenting another group of embedded EZ-source inverters that can handle the same addition as the Z-source inverters however with smoother and smaller Voltage/Current kept up over the dc data source and inside the impedance network [16]-[18]. These last characteristics are achieved without utilizing any extra passive filter, which most likely is a positive point of interest, since an included channel will raise the framework cost and, at times, can complicate the dynamic tuning and resonant thought of the inverters. The similar embedded idea can likewise be utilized for planning a full range of voltage- and current-type inverters. The embedded EZ-source inverters have the points of interest of designing a smoother current from the dc information sources without utilizing outer second-order filter and an easier obliged capacitive voltage. These advantages are accomplished with no degradation in gain, diode blocking voltage, and other trademark properties of the X-formed impedance system for the same specified shoot-through span.

Ding Li et.al [19], reveal a switched Inductor Z-Source Inverter to extend voltage customizability, the proposed inverter utilizes an unique SL impedance network to couple the power source and the main circuit. Contrasted the classical Z-source inverter [20], [21], the proposed inverter builds the voltage help reversal capacity essentially. Just a short shoot-through zero state is obliged to get high voltage change proportions, which is gainful for enhancing the output power nature of the main circuit. Also, the voltage buck inversion capability is additionally given in the proposed inverter to those provisions that need low ac voltages. Like the classical Z-source inverter, the proposed ideas of SL. It is seen that both the top and bottom SL cells perform the same capacity to retain the vitality put away in the capacitors. By an in-depth topology dissection, it is realized that the proposed inverter can give a solid support reversal capacity to defeat the impediments of the classical Z-source inverter [20].

Minh-Khai Nguyen [22], In correlation to the conventional trans-Z-source/ -trans-semi Z-source Inverters,with a specific end goal to transform the same include and output voltage with the same balance list, the enhanced inverter utilizes an easier transformer turn proportion contrasted with the accepted inverters. In this way, the size and weight of the transformer in the enhanced inverter might be diminished [23], [24].

3. BASIC STRUCTURE OF HYBRID SYSTEM

In Fig. 2 the basic block diagram of hybrid dc-dc converter with Quasi-ZSI (Impedance source Inverter) is shown. Here, DC supply is given as input to impedance source network in order to offerextensivevoltage range than the conventionalcurrent or voltage source inverter. The output from impedance network is given tolagging or

leading leg of single phase inverter based on output type from network. The single phase inverter organizes the current and voltage to provideconstant and adjustable voltage (or) current demanded by the application. Therefore the controllable AC output from single phase inverter is stepped up by isolation transformers. Moreover the isolation transformers also afford isolation to power devices from the power sources and electric shock (or) electrical stress. Then the AC from the inverter is converted to DC by the primary rectifier and fed to the filter circuit to eradicate the ripples at the output. The filter circuit is the integration of the LC circuit or output capacitors which helps in selecting the preferred frequency range. Then finally it is given to the voltage doubler rectifier to double the input voltage and to obtain ripple free output. Ripple free pulse is given to load circuit to acquire quality output. Thus, efficiency of system gets enhanced than the conventional method.

The quasi ZSI (Impedance source inverter) dc-dc converter with shoot through technique is shown in fig. 3. In this, magnetic energy isaugmented by the inductors at input terminals, without the capacitor short circuiting. Hence, increased inductive energy increases the input voltage and ZSI (Impedance Source Inverter)so that the proposed topology to operate as a conventional VSI (Voltage Source Inverter). The capacitors and inductors in the circuit serve as a filter which decreases input ripple and increase the efficiency. The MOSFET switchesbehaviour in a cross conduction so that switching losses will be significantlydecreased. Input current flows I_{in} through the coil L_1 and shunt current I_{sh} flows through the switches. Depending on the boosting factor, input voltagelevelcan be decreased or increased by the use of impedance network. This circuit is advantageous by the small size capacitance and inductance and moreover by its performance as a second order filter.

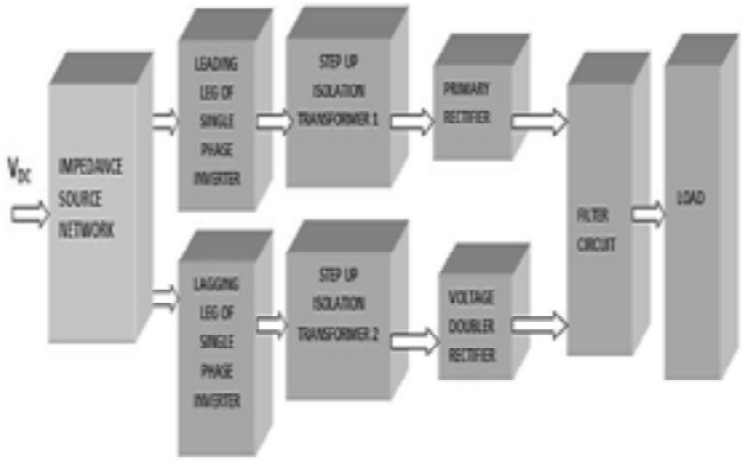


Fig: 2 Structure of Hybrid dc-dc converter with qZSI (Impedances source inverter)

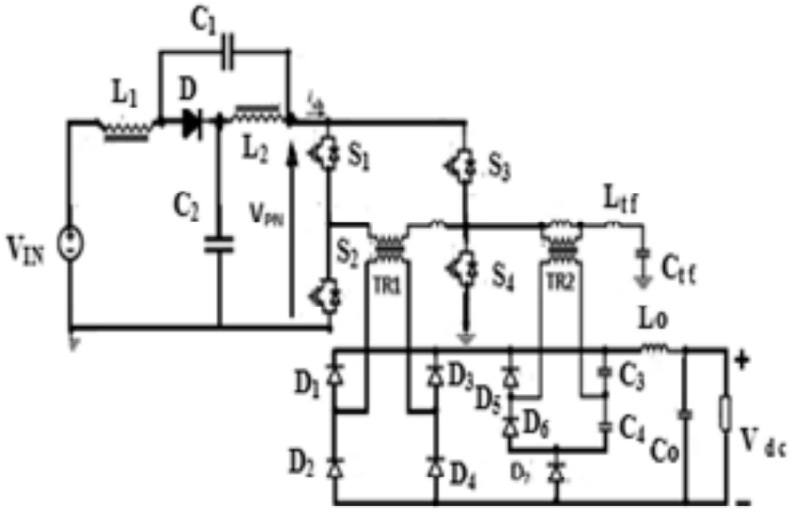


Fig: 3Quasi ZSI (Impedance source inverter) DC-DC converter

Considering the quasi impedance networkcapacitors C_{i1} and C_{i2}andinductors L_{i1} and L_{i2}-- which have same inductance (L) and capacitor (C) correspondingly, then the quasi impedance source network becomes symmetrical.

Using symmetry condition and equivalent circuit, we have

$$V_{Ci1} = V_{Ci2} = V_C \; ; \; V_{Li1} = V_{Li2} = V_L \tag{1}$$

By statement of quasi impedance source dc-dc converter, the shoot through state interval TST during a switching cycle TS-can be moderated to the equivalent circuit, Fig.2 has

$$V_L = V_C \; ; \; V_d = 2V_C \; ; \; V_i = 0 \tag{2}$$

Consider that the quasi *Z* source Inverter Bridge in any one of non-shoot through states (or) active for an interval of TNST.

Hence from the equivalent circuit, Fig. 2 has

$$V_L + V_C = V_{in} \; ; \; V_L = V_{in} - V_C \; ; \; V_d = V_{in}$$
$$V_i = V_C - V_L = 2V_C - V_{in} \tag{3}$$

Where V_{in} is input dc voltage.

The average inductor voltage over single switching period (TS)should be zero. Then by the equation (2) and (3), we get

$$V_L = \frac{T_{ST} V_C + T_{NST} \left(V_{in} - V_C \right)}{T_S} = 0 \tag{4}$$

Or

$$\frac{V_C}{V_{in}} = \frac{T_{NST}}{T_{NST} - T_{ST}} \tag{5}$$

Across the inverter bridge, average dc link voltage is obtained as,

$$V_i = \frac{T_{NST}}{T_{NST} - T_{ST}} V_{in} = V_C \tag{6}$$

Correspondingly, from (3), the maximum dc link voltage across Inverter Bridge can be given as,

$$V_i = V_C - V_L = 2V_C - V_{in} = \frac{T_S}{T_{NST} - T_{ST}} V_{in} = BV_{in} \tag{7}$$

Where T_{ST} = Duration of shoot through state

T_{NST} = Duration of non shoot through state

T_S = operating period i.e. switching cycle

$$T_S = T\text{-}_{ST}\text{-} + T_{NST} \tag{8}$$

$$B = \frac{T_S}{T_{NST} - T_{ST}} = \frac{1}{1 - \frac{T_{ST}}{T_S}\left(1+n\right)} = \frac{1}{1 - D_{ST}\left(1+n\right)} \geq 1 \tag{9}$$

Where n is number of stages

If $n = 1$ for conventional QZSI that is for single stage QZSI

$$B = \frac{1}{1 - 2D_{ST}} \geq 1 \tag{10}$$

DST-duty cycle of the shoot through state can be determined using

$$D_{ST} = \frac{T_{ST}}{T_S} \tag{11}$$

The modulation index of QZS main circuit will be reduced to a very low level and it can be stated as,

$$M \leq 1 - D_{ST}$$

Where M is modulation index

$$M = \frac{Amplitude\ of\ \ Modulation\ waveform}{Amplitude\ of\ \ carrier\ \ Waveform}$$

From (7),

$$V_i = B.V_{in} \tag{12}$$

The equivalent dc link voltage is the maximum dc link voltageof inverter. Hence, the QZS inverter phase voltage of can be given as,

$$V_{dc} = V_i \tag{13}$$

$$V_{dc} = B.V_{in} \tag{14}$$

Resulting from shoot through state B is the boost factor. Then the phase voltage of the Quasi ZSI is given as

$$V_{ac} = M\,\frac{V_i}{2} \tag{15}$$

Using equation (7) & (12), equivalent dc link of inverter can be further expressed as,

$$V_{ac} = M.B.\frac{V_{in}}{2} \tag{16}$$

Above equation (16) further expressed as in terms of buck- boost factor

$$V_{ac} = B_{BB}.\frac{V_{in}}{2} \tag{17}$$

Where B_{BB} is buck boost factor

$$B_{BB} = M.B = \left(0 \approx \infty\right) \tag{18}$$

The QZSI based dc-dc converter starts to function as conventional VSI based dc- dc converter excluding shoot through condition, when input voltage is large, thus accomplish only buck function of the input voltage. From (1), (5) & (10), the capacitor voltage can stated as,

$$V_{C1} = V_{C2} = V_C = \frac{1 - D_{ST}}{1 - 2D_{ST}} . V_{in} \tag{19}$$

Note that the Boost factor B in (10) can be organized by shoot through duty cycle D_{ST} which can be definite by interval of shoot through time T_{ST}. Also, buck boost factor B_{BB} is determined by the modulation index M and boost factor B. In simple boost method Pulse Width Modulation (PWM) techniques the modulation index M can be determined by the ratio of the amplitude of the modulation waveform to amplitude of the carrier waveform.

The voltage conversion ratio of QZS inverter can be expressed as,

$$G = V_{ac} = M.B.\frac{V_{in}}{2}; \quad G = \frac{V_{ac}}{\left(\frac{V_{in}}{2}\right)} = M.B \tag{20}$$

Hence From (1) & (14), the quasi impendence network can perform as the step-up dc–dc conversion from V_{in} to V_{dc}, thus the numerical condition DST is limited to,

$$0 \le D_{ST} \le 0.5 \tag{21}$$

4. EXPERIMENTAL RESULT

In fig. 4 the block diagram of gating signal generator is shown. For active state or zero state control, the different input pulses such as ramp and sinusoidal are compared with the relational operator. ThePulse Width Modulation (PWM) signals are produced and the portion of the output inverted by the logic gates provides the control for the states. The output that is inverted is given to thyristor switches T_1 and T_3 to turn ON. Conversely for the shoot through states the relational operator compares the various signals' amplitude given at the input.The Pulse Width Modulation (PWM) with logic gates and comparator provides the control circuit for shoot through state. The OR gates in this performs addition of the active and shoot-through states. Hence switches T_2 and T_4 get operated according to the gating signals.

Basically the shoot through states is organized by comparator signals. The control from PWM signal is given as the input to logic gates which operates the switches. The upper and lower level signals output are compared with

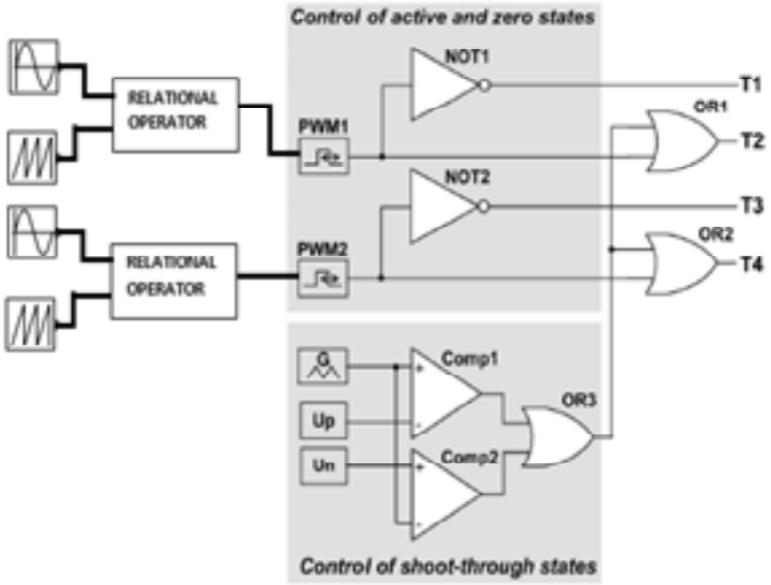


Figure 4: Generalized block diagram of gating signal generator

the help of comparator. The output from comparator is given to logic OR3 and given as one of the input to OR1 and OR2. The resultant is used to operate switches T2 and T4.The generation of shoot through pulses are given by Fig.6.The upper and lower shoot through pulses generated are shown in figure. The peak of pulses is produced with reference DC line voltages. The lower and upper shoot through pulses are generated by comparing with the reference signal or saw tooth waveform.

The lower shoot through pulses are produced as a inter-mediate pulses of upper shoot through pulses. These waves are modified and combined in order to reduce cost and reliability. Thus, the efficiency of power conversion can be greatly increased.In Fig.6; the various pulses that are generated based on input given by the gate signalis shown. At any instant two pulses starts at same time period and remaining two pulse remains in zero position for small interval of time.

The distortion in current waveform is more than that of voltage waveform. The transformer 1 produces output with ripple rich currentshown in Fig.7. This distortion can be reduced by use of filters or capacitive circuits. In Fig.8

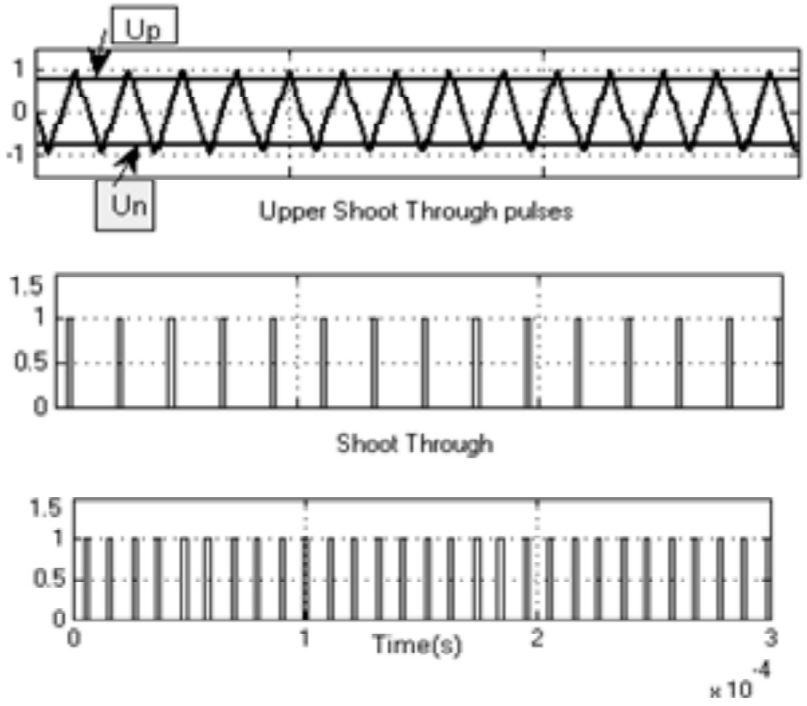


Figure 5: Generetion of upper and lower shoot through pulses

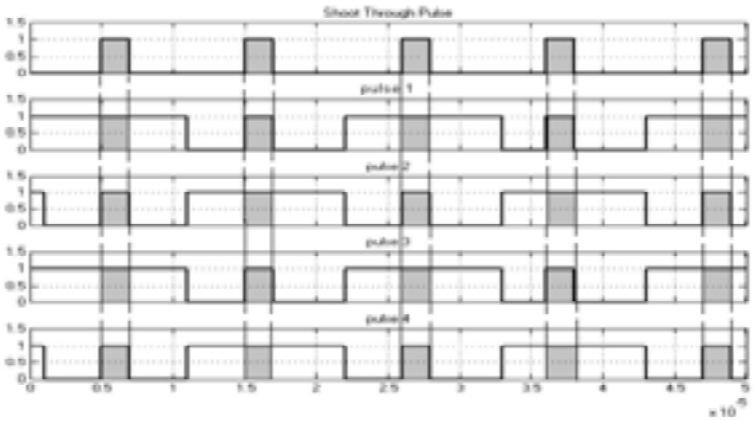
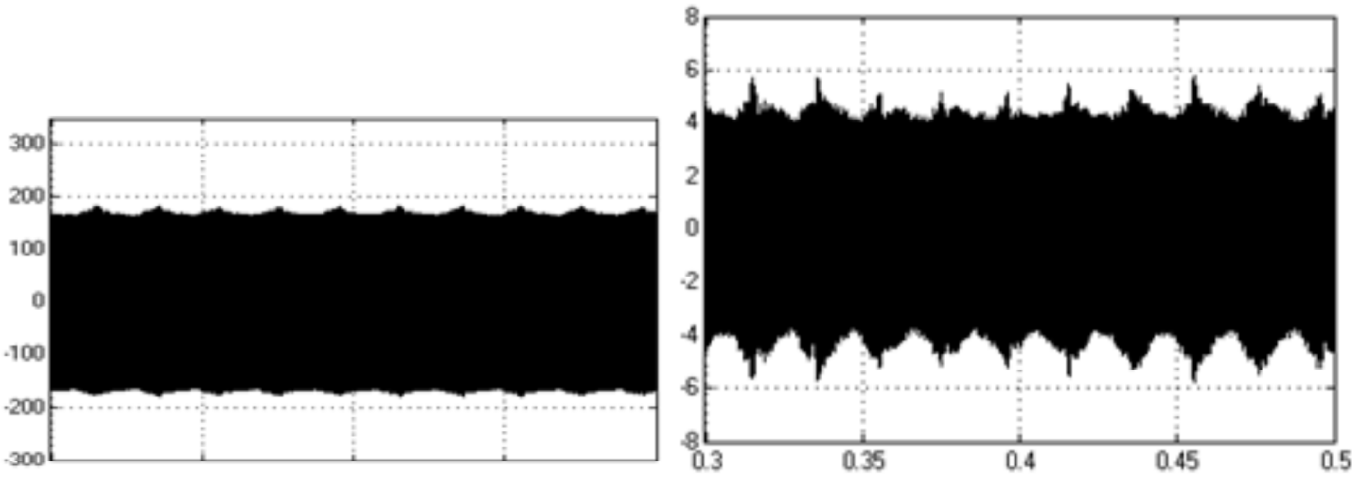


Figure 6: Pulses of various switches

zoom in view of voltage and current waveforms of transformer1 is clearly shown. It is shown that distortion in current waveforms is more than that of voltage. The analog output signals can be generated with combination of Pulse Width Modulation (PWM) and filter circuit. In order to generate different levels of analog signals, the duty cycle and pulse width of digital signal is varied.

In Fig.9 the voltage and current waveforms of transformer2 is clearly shown and when compared to transformer 1, the time duration of pulse generation is less and distortion is also reduced. The current waveform gets distorted more than that of voltage. Thus, distortion can be reduced by use of filters. The various waveforms of voltage and current of elements such as inductor 1 and 2 are shown in Fig.10. The current waveform is almost close to dc output and voltage waveform of inductor 2 is inverted output of inductor 1. The width of pulses is same for both voltage waveforms of inductors. The zoom in view of waveforms is clearly shown in Fig.11 and it is obvious that the waveform is similar to that of conventional converters.

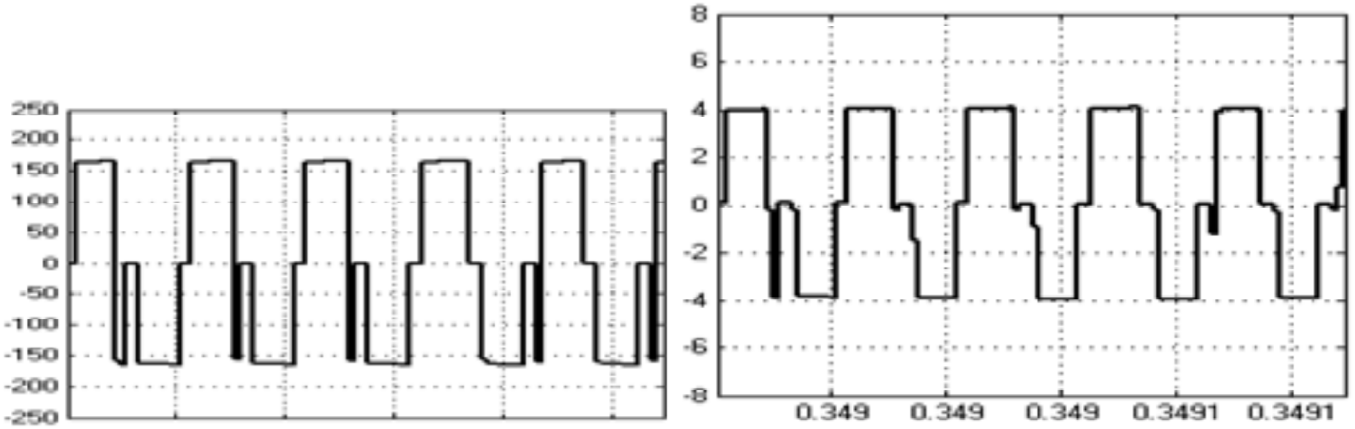
The various voltage and current waveforms during charging and discharging is shown in Fig.12. At various values of Up, the output voltage and current are simulated and shown in Fig.13-15.



(a) Transformer 1 Voltage

(b) Transformer 1Current

Figure 7: Transformer output voltage and current



(a) Transformer 1 Voltage

(b) Transformer 1 current

Figure 8: Zoom in view of voltage and current wavwforms for transformer 1

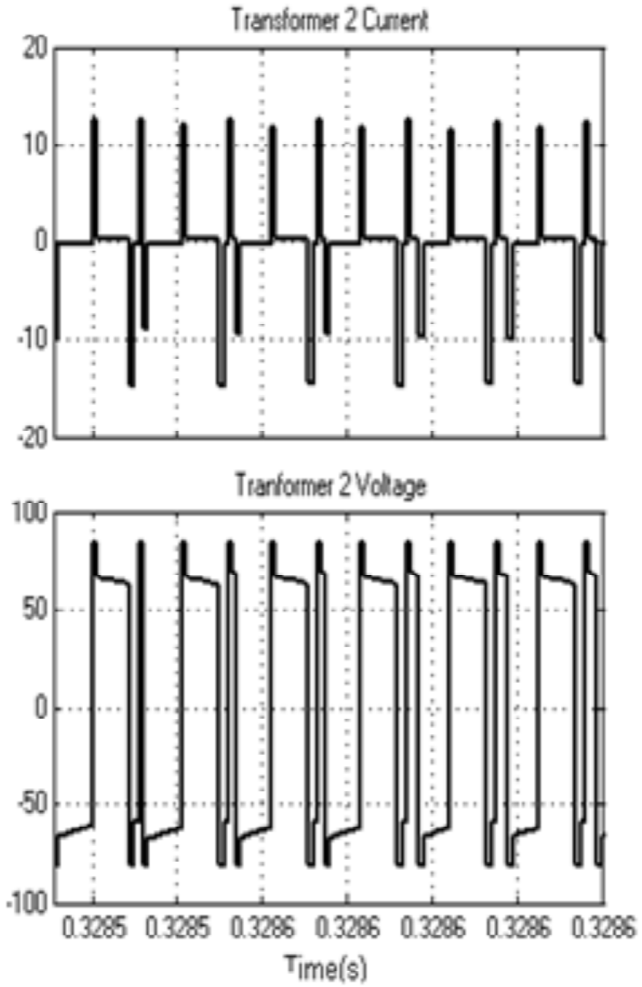


Figure 9: Voltage and current waveforms of transformer 2

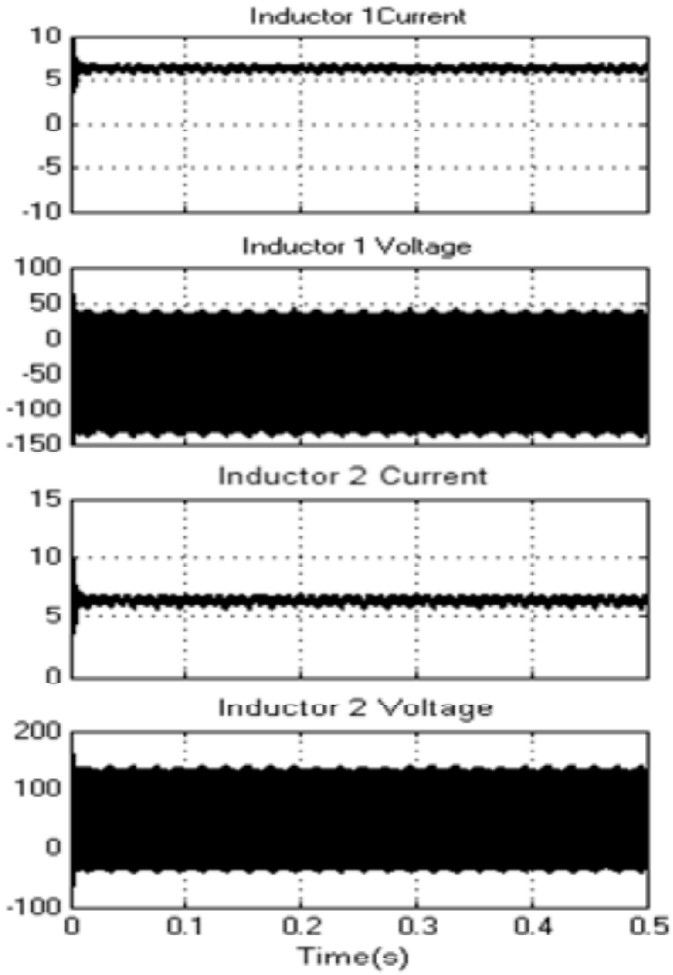


Figure 10: Simulated voltage and current waveforms of inductors 1 and 2

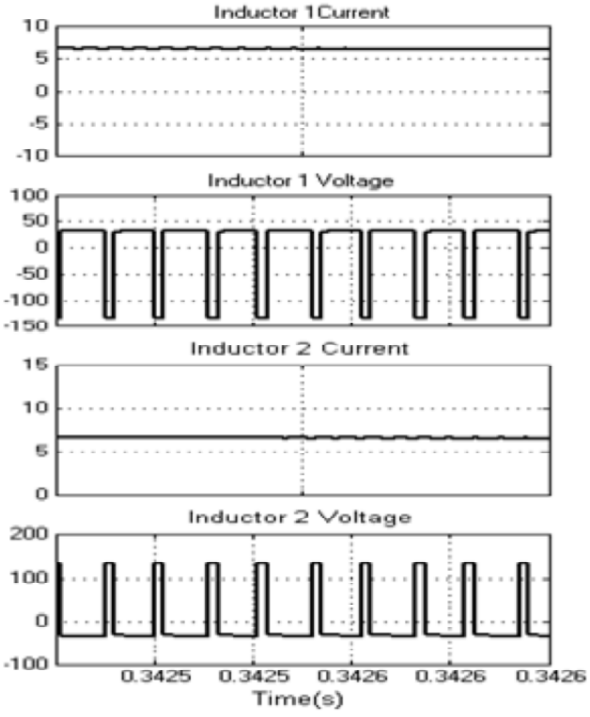


Figure 11: Voltage and current waveforms of inductors

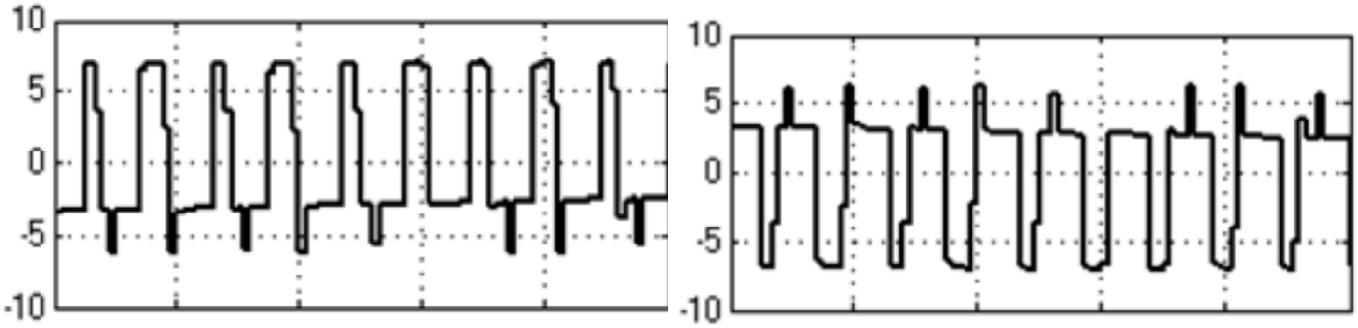


Figure 12: Voltage and current waveforms of capacitor

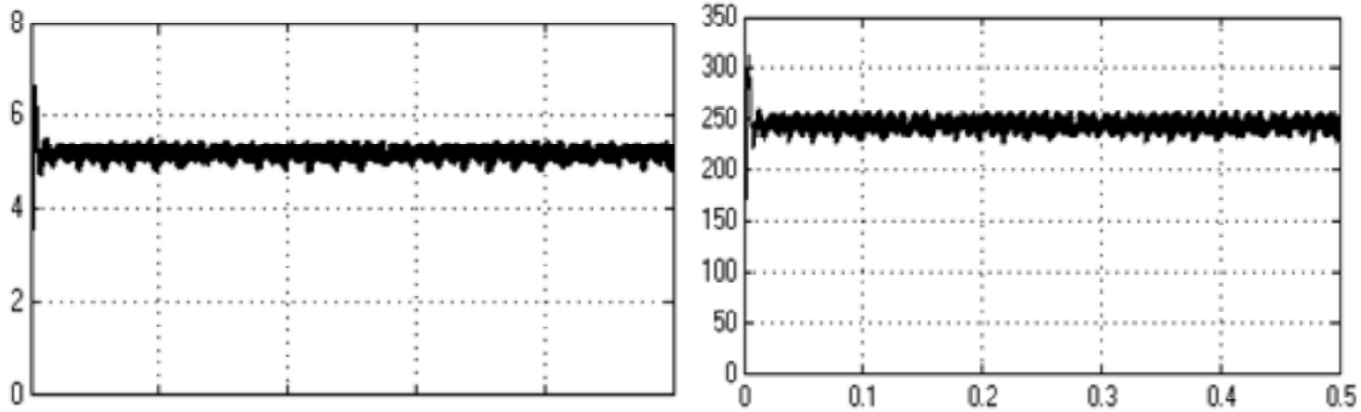


Figure 13: Output voltage and current waveforms when Up = 0.8

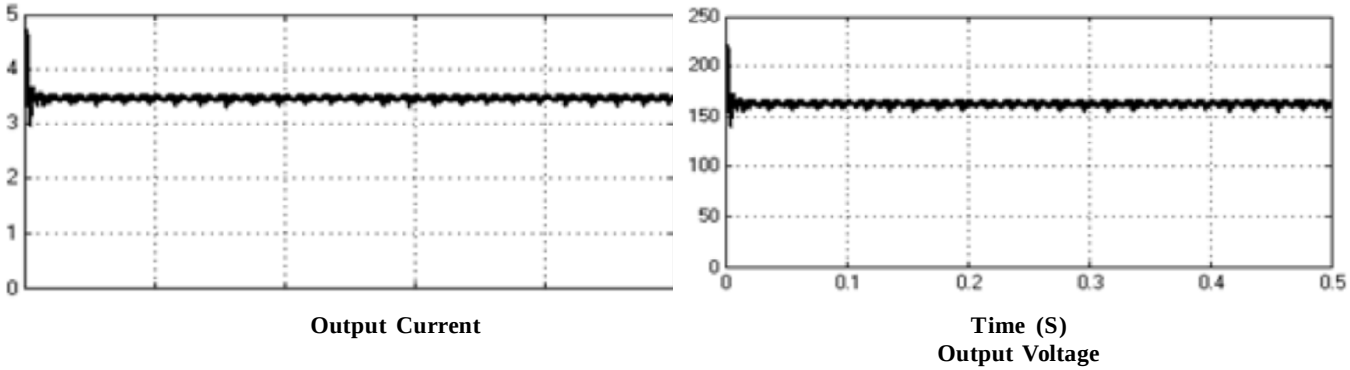


Figure14: Output voltage and current waveforms when Up = 0.7

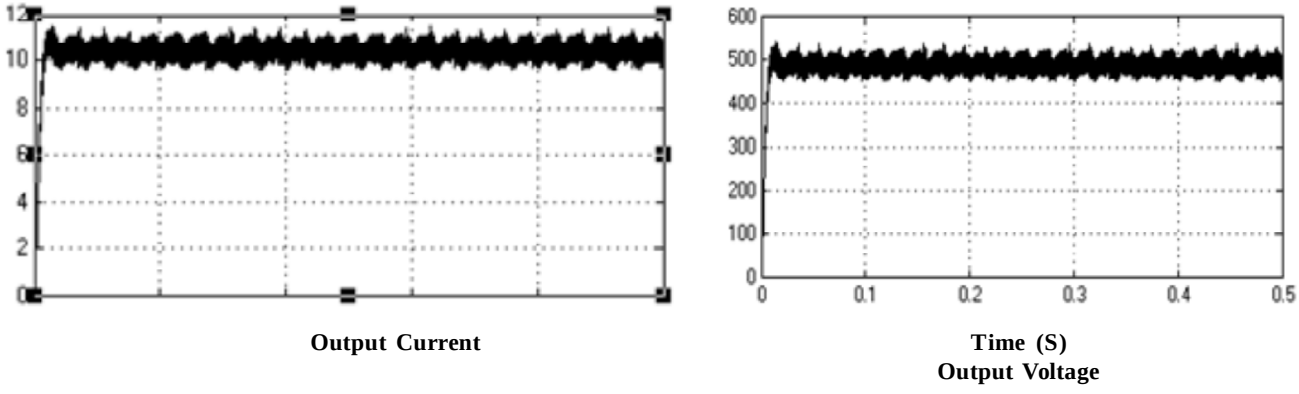


Figure15: Output voltage and current waveforms when Up = 0.6

5. PERFORMANCE ANALYSIS

The parameters used in simulation are shown in Table.1. By using parameters, the results are observed for different operating condition for boost factor and voltage gain. The simulation results are shown in the Table 2. By using various duty cycle and modulation index condition, the results are taken for simple boost control condition.

Table 1
Simulation Parameter

V_{in}	100V
L_1 & L_2	3 mH
C_3 & C_4	20 µF
C_1 & C_2	10 µF
C_0	20 µF
L_0	0.2 mH
R_0	47&!
f_s	47.66KHz
D_{ST}	0.2
V_{dc}	163V
I_{dc}	3.4A

Table 2
Simulation Results of Boost Factor and Voltage Gain in various operating conditions

V_{in}	D_{ST}	M	B	G	V_{dc} Simul.	Calc.
100V	0.1	0.9	1.25	1.125	112.5	112.5
	0.2	0.8	1.67	1.33	163	163
	0.3	0.7	2.5	1.75	250	250
	0.4	0.6	5	3.0	500	500
	0.45	0.55	10	5.5	1000	1000

The Fig.16 shows the boost control ability for proposed converter and is compared with the existing system. The boost control ability for proposed system gets increased rapidly for different shoot through condition i.e., for each duty cycle the boost factor gets increased rapidly.

By varying duty cycle ratio, the output level of analog signal can be increased and vice versa. In Fig.17, the output voltage can be improved with the aid of modulation index. The voltage conversion ratio gets increased with decrease in modulation index and it can be explained with waveforms having different vaues of modulation index. The maximum voltage conversion ratio occurs at value of approximately 0.55. In Fig.18, the duty cycle ratio can be varied to improve the voltage conversion ratio. As voltage level is proportional to duty cycle ratio, the value of voltage conversion capability is also get improved.

6. CONCLUSION

Thus by the quasi ZSI the energy loss in the circuit is significantly reduced. Compared to the conventional dc-dc Conversion method, this method provides high efficiency and high ripple output. Furthermore, the voltage boost factor and voltage stress are enhanced by the shoot-through technique. The value of Up can be adjusted to improve the performance of system.The simulation results also proved that it provided the output voltage twice the input voltagewhich is based on the duty cycle ratio.Moreoverefficiencyincreased of about greater than 90 than the conventional methods.

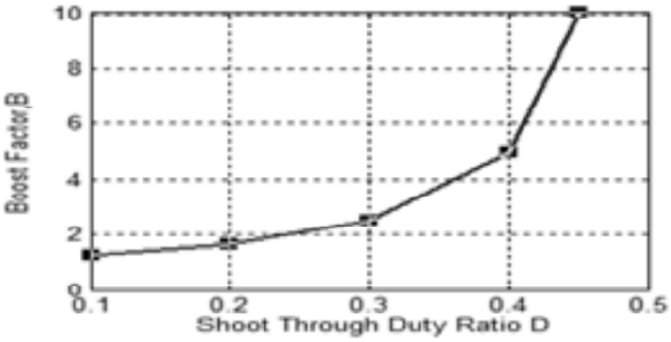


Figure 16: Boost ability comparison of the proposed Q ZI dc-dc converter for various Duty Cycles

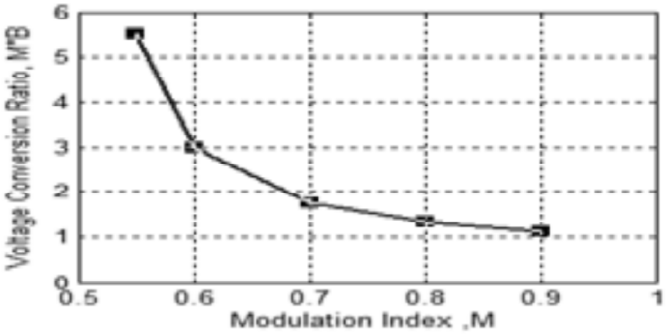


Figure 17: The proposed inverter, under the simple boost control condition for various modulation indexes

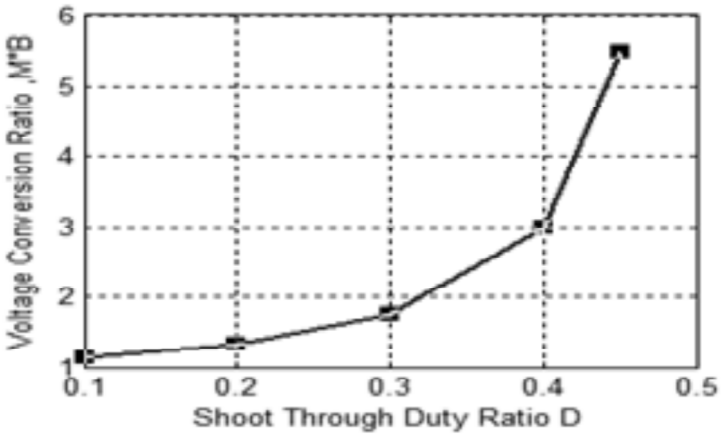


Figure 18: Maximum voltage conversion ratios of the proposed inverter, under the simple boost control condition for various Duty ratios

References

[1] Zhu Liying, "Modeling and dynamics of switching electrical LC-circuits," *IEEE 30th ChineseControl Conference (CCC),* pp. 1555 -1559, July 2011.

[2] Dmitri Vinnikov, Indrek Roasto1, Ryszard Strzelecki and Marek Adamowicz, "Performance Improvement Method for the Voltage-Fed qZSI with Continuous Input Current," *IEEE Transactions on power electronics* 2010.

[3] J.-G. Cho, C.Y. Jeong, and F. C. Lee, "Zero-voltage and zero-currentswitching full-bridge PWM converter using secondary active clamp," *IEEE Trans. Power Electron.,* vol. 13, no. 4, pp. 601-607, Jul. 1998.

[4] W. Yu, J.-S. Lai, and H. Qian, "A family of novel zero-voltage and zerocurrent switching full bridge converters using output voltage reset for fuel cell applications," in *Proc. Annu. Conf. IEEE Ind. Electron. Soc.,* pp. 622-627, Mar. 2007.

[5] M. Boarage, S. Tiwari, S. Bhardwaj, and S. Kotaiah, "A full-bridgeDC–DC converter with zero-voltage-switching over the entire conversion ranges," *IEEE Trans. Power Electron.,* vol. 23, no. 4, pp. 1743-1750, Jul. 2008.

[6] R. Ayyanar and N. Mohan, "Novel soft-switching DC–DC converter with full ZVS-range and reduced filter requirement. I: Regulated-output applications," *IEEE Trans. Power Electron.,* vol. 16, no. 2, pp. 184-192, Mar. 2001.

[7] Il-Oun Lee, and Gun-Woo Moon, Soft-Switching DC/DC Converter With a Full ZVS Range and Reduced Output Filter for High-Voltage Applications, *IEEE Transactions On Power Electronics,* Vol. 28, No. 1, January 2013.

[8] Y. Jang, M. M. Jovanovich, and Y. M. Chang, "A new ZVS-PWM fullbridge converter," *IEEE Trans. Power Electron.,* vol. 18, no. 5, pp. 1122-1129, Sep. 2003.

[9] Wensong Yu, Jih-Sheng (Jason) Lai, Wei-Han Lai, and Hongmei Wan," Hybrid Resonant and PWM Converter with High Efficiency and Full Soft-Switching Range", *IEEE Transactions on power electronics,* vol. 27, no. 12, December 2012.

[10] Jin-Yuan Lin,Chung-Yi Lin and Yu-Kang Lo, "Active-clamping ZVS flyback converter employing two transformers," *IEEE International Aegean Conference on Electrical Machines and Power Electronics*, pp. 498-501, Sept. 2007.

[11] Fang Zheng Peng, "Z-Source Inverter", in proc of *IEEE Trans. on Industry Applications,* vol. 39, no. 2, pp.504-510. March/ April 2003.

[12] Poh Chiang Loh, D. Mahinda Vilathgamuwa, Yue Sen Lai, Geok Tin Chua, and Yunwei Li "Pulse-Width Modulation of Z-Source Inverters", *in procof IEEE Trans on power Electronics,* pp.1346-1355.. vol. 20, no. 6, Nov 2005.

[13] Poh Chiang Loh, D. MahindaVilathgamuwa, "Transient Modeling and Analysis of Pulse-Width Modulated Z-Source Inverter, *IEEE Trans. on Power Electronics,* pp. 498-507, vol. 22, no. 2, March 2007.

[14] Sok Wei Lim, Poh Chiang Loh, FengGao, and FredeBlaabjerg, "Three-Level Z-Source Inverters Using a Single *LC* Impedance Network",*IEEE Trans on Power Electronics*, pp. 706-711, vol.. 22, no. 2, March 2007.

[15] Poh Chiang Loh, Feng Gao, and FredeBlaabjerg, "Embedded EZ-Source Inverters" *IEEE Trans. on Power Electronics*, pp.256-267. vol. 46, no. 1, Jan/Feb 2010.

[16] R. Redl, N. O. Sokal, and L. Balogh, "A novel soft-switching full-bridge DC/DC converter: Analysis, design considerations, and experimental results at 1.5 kW, 100 kHz," *IEEE Trans. Power Electron.*, vol. 6, no. 3, pp. 408-418, Jul. 1991.

[17] L. Saro, K. Dierberger, and R. Redl, "High-voltage MOSFET behavior in soft-switching converters: Analysis and reliability improvements," in *Proc. 20th* IEEE INTELEC. Conf. Rec., 1998, pp. 30-40.

[18] J. Sebastian, P. J.Villegas, F. Nuno, andM.M.Hernando, "High-efficiency and wide-bandwidth performance obtainable from a two-input buck converter,"*IEEE Trans. Power Electron*, vol. 13, no. 4, pp. 706-717, Jul. 1998.

[19] Ding Li, Poh Chiang Loh, Miao Zhu, FengGao, FredeBlaabjerg, "Generalized Multicell Switched-Inductor and Switched-Capacitor Z-Source Inverters" *IEEE Trans On Power Electronics*, pp.837-848, vol. 25, no.. 8, August 2010.

[20] W. Song and B. Lehman, "Dual-bridge DC–DC converter:Anewtopology characterized with no dead time operation," *IEEE Trans. Power Electron*, vol. 51, no. 1, pp. 94-103, Jan. 2004.

[21] O. D. Petterson and D. M. Divan, "Pseudo-resonant full bridge dc/dc converter," in *Proc. IEEE Power Electron. Spec. Conf.,* 1987, pp. 424-430.

[22] Minh-Khai Nguyen, Young-Cheol Lim,Sung-Jun Park, "Improved Trans-Z-Source Inverter with Continuous Input Current and Boost Inversion Capability" *IEEE Trans. on Power Electronics*, pp.4500-4510, vol. 28, no. 10, Oct. 2013.

[23] Quoc-Nam Trinh and Hong-Hee Lee, "A New Z-Source Inverter Topology with High Voltage Boost Ability," *Journal of Electrical Engineering & Technology*, vol. 7, no. 5, pp. 714-723, 2012.

[24] V. Dhivyaand M.Sasikumar, "Implementation of Cascaded Quasi-Z-Source Network Based Step-Up Dc/Dc Converters for Drive Systems,"*Indian Streams Research Journal,* ISSN:-2230-7850 April 12th, 2013.

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