Design of Thirteen Level Cascaded H-Bridge Inverter for Low Power Applications

S. Vaishali*, R. Sai Janani**, Jodhi Mohana Monica** and V. Swetha**

ABSTRACT

A MULTILEVEL CASCADED H-BRIDGE inverter is proposed in this paper which is incorporated as an Uninterrupted Power Supply working in low power. Cascaded H-Bridge Multilevel inverter technology is swiftly attaining reputation because of its benefits amid all other techniques for low power application. An attempt has been made to include this technology which could result in supplying power to six typical computers, thereby replacing six separate conventional UPS. The inverter constructed using cascaded H-bridge multilevel inverter technology produces a stepped AC voltage waveform at the output when the input is comprised of six separate batteries. This makes the Cascaded H-bridge multilevel inverter technology as most suitable for this low power application. The modulation technique used is PULSE WIDTH MODULATION.

Keywords: Multilevel, cascaded H-bridge, Low power Application, Pulse width modulation.

1. INTRODUCTION

The prime usage of UPS is to secure susceptible loads like medical facilities and industrial processing systems. Irrespective of the standards of DC power source, uninterrupted power supply (UPS) system has to deliver distortion free high quality waveforms so as to guarantee consistent working of the load. Basic types uninterrupted power supply systems are (i) online uninterrupted supply, (ii) offline uninterrupted power supply (iii) Hybrid uninterrupted power supply systems.Using large number of switches in an inverter leads to high cost which could restrict it from beingimplemented in cost concerned applications [1][5].

This becomes a great disadvantage of conventional uninterrupted power supply topology. Reducing the cost of UPS systems in order to draw researchers interest has been the keen reason for seeking different

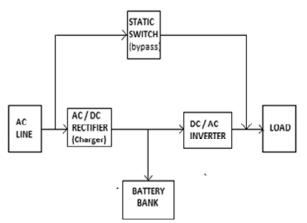


Figure 1: Block diagram of a typical on-line UPS system

^{*} Asst. Professor,

^{**} B. Tech Students, Department of Electrical and Electronics, SRM University, Chennai, Emails: vaivin2722@yahoo.co.in, rsaijanani95@gmail.com, jmmoni07@gmail.com, venkatswetha95@gmail.com

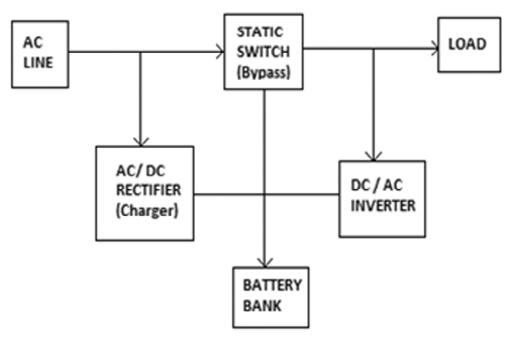


Figure 2: Block diagram of a typical off-line UPS

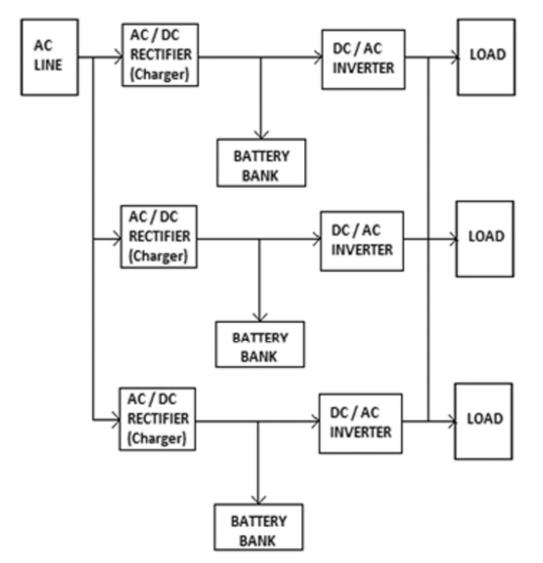


Figure 3: Schematic diagram of UPS

topologies. Thus, in the other topologies decline in cost is attained by (i) decreasing the number of switches (ii) lowering the voltage stress across the switches (iii) removing bulky passive components like transformers [1]. The main objective of the cascaded H-Bridge multilevel inverter topology is cascading the DC sources to receive a stepped output voltage waveform [9].

The cascaded H-bridge design can be upgraded into higher capacity by varying the current ratings of components and therefore it has the ability to serve large loads [11]. The demerits of conventional inverter are (i) The battery plays the alternate role during the failure of main supply, due to some fault, if the battery is not charged, it leads to failure of power to the load. (ii) A basic conventional inverter has the capacity to supply a single computer. Multilevel inverter's advantage over the conventional inverter is the removalof bulky transformers[11].

2. PROPOSED SYSTEM

2.1. Inverter Topology

The inverter design is made by using cascaded H-bridge multilevel inverter topology which is its main significant characteristic. The main advantage of this multilevel inverter is (i) reduced switching frequency (ii) reduced voltage applied per semiconductor device [3]. The above mentioned two features appreciably decreases the switching stress due to semiconductor device's lifetime recuperating the durability of the proposed UPS. To reduce the complication of the controller, all the six batteries voltages are equal step size is assumed and hence, recognized as a symmetrical source inverter [5]. In additional to this, the equal size batteries usage provides the benefit of easy replacement. There is a relationship between the number of DC sources and the output levelwhich is related as

$$N = 2 \times S + 1 \tag{1}$$

N = Number of levels of the output

S = Number of separate DC sources

The proposed inverter is constructed for 13 levels for which six separate DC sources are required in order to accomplish conciliation between these two factors. The schematic of the proposed system is shown

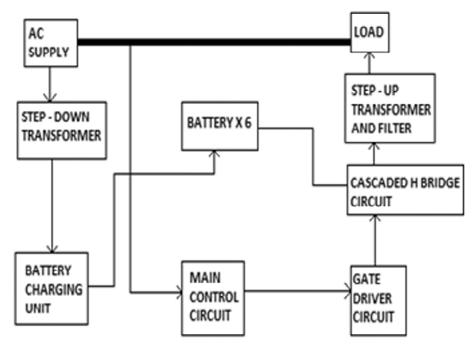
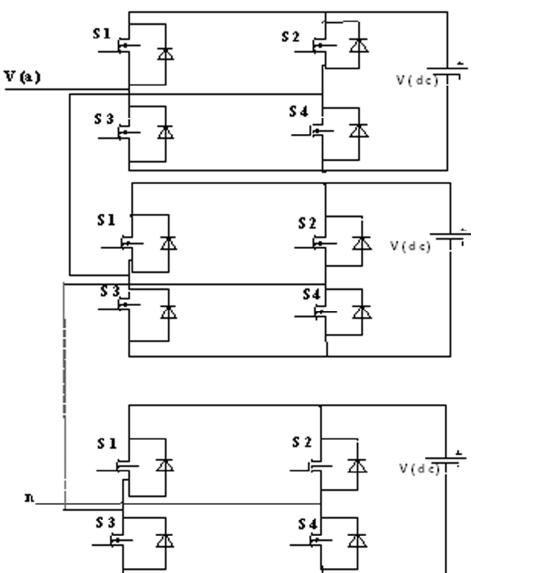


Figure 4: Schematic diagram of the proposed UPS

in fig.4. The main supply is connected to the load directly. The battery is charged during this time. Whenever there is failure of power the switch connects the battery to the load through the inverter [1]. The total harmonic distortion of the proposed system for different types of loads are also analysed and the results are compared [10].

2.2. Cascaded H-Bridge Working

There are six single phase full bridges, each connected to a separate DC source, three diverse voltage outputs are produced in each inverter level. +Vdc, 0, -Vdc. When S1 and S4 are switched ON, +Vdc is attained while -Vdc is attained when S2 and S3 are switched on [9]. The output voltage is obtained by either switching on S1 and S2 or S3 and S4. The generated output voltage waveform is the summation of the inverter outputs which is obtained by connecting the AC outputs of each of the different full bridge inverter levels. The number of output voltage levels n is acquired by n = 2p + 1, where n is the number of separate dc sources. For example, a phase voltage waveform of a n level cascade H bridge inverter with five separate DC sources and m full bridge inverter is shown below. The phase voltage is given by



$$V_{an} = V_{a1} + V_{a2} + \dots + V_{am}$$
 (2)

Figure 5: Circuit of a H-Bridge converter.

3. MULTILEVEL INERTER

A power electronic device has the ability to render required alternating voltage level at the output with the help of several lower level DC voltages in the place of input is referred to as multilevel inverter, while focusing on two level inverter, it is noted that it generates two different voltages for the load, where the output will be positive half and negative half of the supply voltage [2]. An alteration in this two level inverter directs to the idea of multilevel inverter [11]. The voltage levels are directly proportional to the ease of the waveform and hence the proposed multilevel inverter results in smoother voltage waveform which is a representation of lower harmonic distortions. The three basic categories of multilevel inverter topologies are (i) cascaded H-Bridge multilevel inverter (ii) diode clamped (iii) flying capacitor multilevel inverter [2]. The cascaded H bridge multilevel inverter generates a sinusoidal multilevel inverter. The cascaded H-bridge multilevel inverter is a sum of the voltages generated by each H-bridge circuit. When compared to diode clamped multilevel inverter and flying capacitor multilevel inverter, cascaded H-bridge inverter needs decreased number of components. Hence, its overall weight is reduced resulting in a lower price.

Merits of cascaded H-bridge inverter [7]:

- (i) The input current is drawn with low distortion in multilevel inverter.
- (ii) Operation in both fundamental switching frequencies is essential for an inverter. In case of multilevel inverter, it operates in lower switching frequency which results in lower switching loss and higher efficiency.
- (iii) In spite of a lower number of sources, the output voltage levels are twice the number of sources.
- (iv) Manufacture of multilevel inverter is simple and rapid.
- (v) Layout is just and packaging is flexible
- (vi) Control of inverter using transformers has a very good impact.
- (vii) Economical.

4. MODULATION TECHNIQUE

The procedure of bearing data on a chain of pulses and the information to be encrypted in the width of pulses is called PULSE WIDTH MODULATION (PWM) [4]. The magnitude and frequency are the two factors that influence the AC Voltage. Maintaining these two factors within permissible limits is very important [3]. The search for the best way to control the two factors leads us to PWM Technique. The basic idea is to compare the career signal amplitude with the reference signal amplitude. The frequency of the reference signal has a great impact on the frequency of the output voltage [8]. There are many types of Pulse Width Modulation Techniques. The three basic techniquesamong those are listed below:

- (i) Single Pulse Width Modulation Technique
- (ii) Multiple Pulse Width Modulation Technique
- (iii) Sinusoidal Pulse Width Modulation Technique

4.1. Sinusoidal Pulse Width Modulation Technique

A slight modification in Multiple Pulse Width Modulation leads to the identification of Sinusoidal Pulse Width Modulation Technique. The magnitude of sine wave isestimated in the middle of a single pulse and the duration of each pulse is varied based on the magnitude determined. On comparing the sinusoidal

reference wave with a triangular wave of high frequency, the gating signals are generated. The ratio of reference signal amplitude to the career signal amplitude is called MODULATION INDEX. Referring to Fig.6, When the amplitude of the sine wave is more than that of the triangular career wave, the positive group of MOSFETs start conducting, whereas when the amplitude of the sine wave is lower than that of the career wave, the negative group of MOSFETs begins to conduct [4][6].

Merits of PWM Technique [4]:

- (i) As a diode rectifier is used, the power factor of the system is improved.
- (ii) The transient response of Pulse Width Modulation is good.
- (iii) Inspite of reduced speeds, the magnitude of torque variations is decreased.
- (iv) Minimisation of lower order harmonics and implementation of output voltage control is significant.

5. SIMULATION

The proposed cascaded H-Bridge Multilevel inverter has six separate DC sources, each source for each H-Bridge circuit. The AC supply is stepped down using a transformer of corresponding rating and the stepped

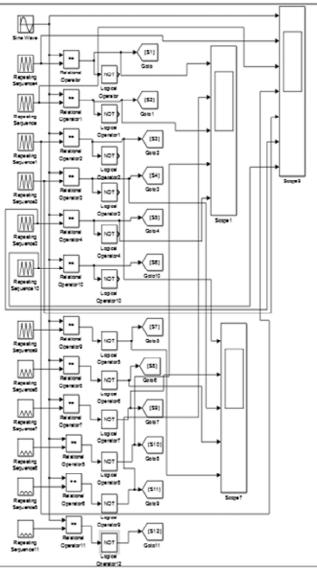


Figure 6: Modulation Circuit

down supply is given to a diode rectifier. The diode rectifier converts the AC supply to DC supply and sends it to the battery. The AC source is connected across the load with a Circuit Breaker and hence in the situation of failure in mains supply the circuit breaker opens and the power begins to be supplied from the battery.

In Multi-level inverter, unlike the conventional inverter the battery is always synchronized with the supply and hence takes very less time for the battery to take-over control. From the battery, the H-Bridge circuits are supplied with power. Fig.6 shows the modulation of the various switches of the inverter.

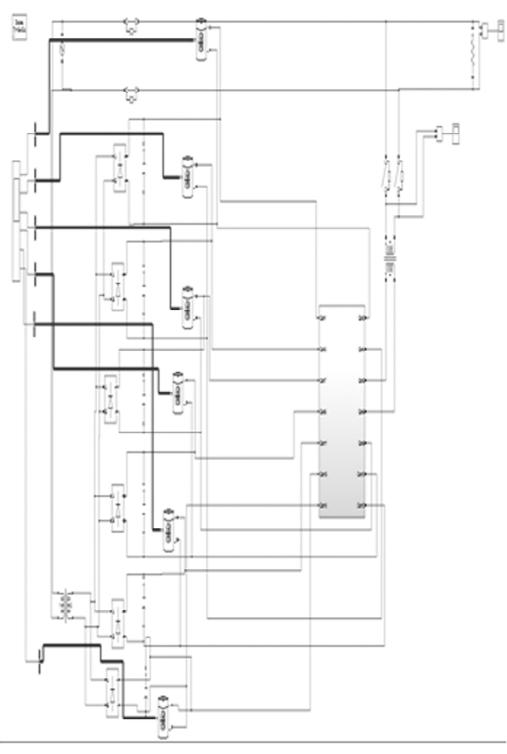


Figure 7: Simulation Circuit of Thirteen Level Cascaded Multilevel Inverter.

The MOSFETs in the bridges conduct based on the supply from the battery and the pulses from the modulation circuit from fig. 6. The output voltage of the inverter is the sum of the output voltages of the six H-Bridge circuits. The output voltage obtained is stepped up using a transformer and then supplied to the load. The stepped waveform obtained through this procedure has higher amplitude than the original AC supply and hence this is of a great advantage. As six DC sources are used and can power six computers in the place of six separate UPSs, this inverter is called as THIRTEEN LEVEL CASCADED H-BRIDGE INVERTER based on the formula

$$N = 2p + 1 \tag{3}$$

 $\Rightarrow N = 2(6) + 1$ $\Rightarrow N = 12 + 1$ $\Rightarrow N = 13$

The overall simulation circuit of the proposed system is shown in Fig. 7.

6. **RESULTS**

The simulated output of the proposed system is shown in Fig. 8 and Fig. 9. The load is directly supplied from the main AC line for duration of 3 seconds and when the power is cut off, the inverter takes is role in supplying to the load. The variation from a pure sine wave to a 13 level stepped wave after a time of 3 seconds is shown.

As specified the amplitude of the inverter output is greater than that of the amplitude of the voltage from the mains supply to the load.

The stepped output voltage waveform has a peak to peak voltage about 420 V which is obtained by the sum of output voltages from the H bridges which is 70V.

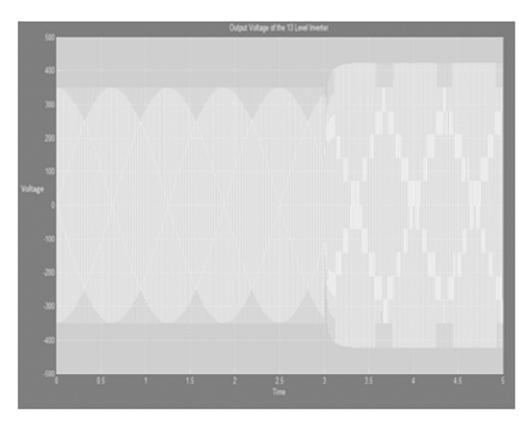


Figure 8: Output waveform

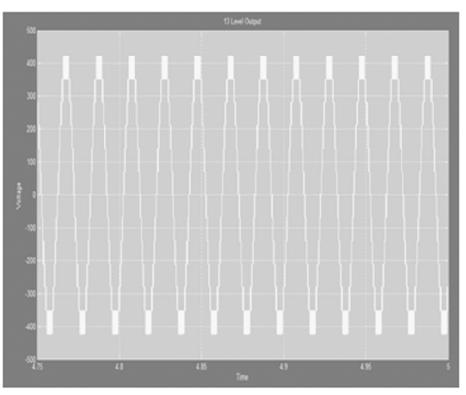


Figure 9: Stepped output waveform of thirteen level Cascaded H-bridge Inverter

Table 1
Comparison of the harmonic levels for various loads

THD ANALYSIS	
Load	Without filter (%)
R	10.89
RL	12.11
RLC	13.09

Table 1 shows the comparative analysis of the harmonics of the proposed system for various loads. The harmonics are less for a pure resistive load and high for an RLC load. As the level of the inverter increases, the harmonics percentage decreases and with the use of filter it decreases further.

7. CONCLUSION

The model of thirteen level Cascaded H Bridge inverter is proposed in this paper for low power applications. Although various studies have been made in the use of Cascaded H Bridge inverts for high power applications, a booming performance of this technique is obtained by integrating the projected inverter in a low power a uninterrupted power supply function. Thus, it is anticipated to substitute six separate conventional uninterrupted power supply to supply six personal computers. This justifies the use of six DC sources generating a thirteen level output. In the view of results from both simulation and authentic performance, it sums up the high performing uninterrupted power supply is provided by including the cascaded h bridge inverter in a standby UPS through distortion reducing PWM. Proper use of filters also reduces the harmonics at the output level.

8. FUTURE SCOPE

- Hardware implementation of the proposed system can be done and real time results can be analysed for various load types.
- The levels of the Multilevel inverter can be further increased and thus harmonics also gets reduced.

REFERENCES

- [1] R.N. Naik R, R. Jayapal. "Design of online ups system with over voltage, under voltage and phase out protection," *International Journal of Modern Engineering Research*, vol. 2, issue. 5, pp. 3684-3688, Sep-Oct. 2012.
- [2] Prof. A.S. Mane, Faculty department of Electrical Engineering, Govt. college of engineering, Karad, India, "Performance analysis of multilevel inverter", Second International Conference on Emerging Trends in Engineering (SICETE) Dr.J.J.Magdum College of Engineering, Jaysingpur.
- [3] Keith Corzine, Missouri University of Science and Technology and Yakov L. Familiant. "A new cascaded multilevel Hbridge drive", IEEE Transactions on power electronics vol. 17, No. 1, January 2012.
- [4] B. P. Mcgrath and D. G Holmes "Reduced PWM harmonic distortion for multi level inverters operating over a wide modulation range" IEEE Transactions on Power Electronics vol. 21 No 4, July 2006.
- [5] P.D.H. Darmawardana, T.D. Kahingala, K.M.C.G. Karunarathna, L.B.S.N. Kularatne, J.P. Karunadasa, University of Moratuwa, Sri Lanka, "Nine Level Cascaded H Bridge Inverter For High Performing UPS Applications", IEEE, 2015.
- [6] NasrudinAbd. Rahim, Mohamad Fathi Mohamad Elias, Wooi Ping Hew, IEEE transaction. Industry Electronics, "Design of filter to reduce harmonic distortion in industrial power system", Vol. 60, No: 8, 2943-2956, August 2013.
- [7] Rodríguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A Survey of topologies and controls, and applications", IEEE Trans.Ind.Electron,vol. 49, no. 4, pp. 724–738, Aug. 2002.
- [8] Kouro, Samir, Jaime Rebolledo, and José Rodríguez. "Reduced switching-frequency-modulation algorithm for high-power multilevel inverters." *IEEE Trans. Ind. Electron*, vol. 54, no. 5, pp. 2894-2901, 2007.
- [9] Divya Subramanian and Rebiya Rasheed "Five Level Cascaded H bridge Multilevel Inverter Using Multicarrier Pulse Width Modulation Technique", International Journal of Engineering and Innovative Technology, vol. 3, issue 1, July 2013.
- [10] Jagdish Kumar, "THD analysis for different levels of cascaded multilevel inverters for industrial applications," *International Journal of Emerging Technology and Advanced Engineering*, vol.2, issue 10, Oct.2012.
- [11] L. G. Franquelo, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," IEEE Ind.Electron. Mag., vol. 2, no. 2, pp. 28–39, Jun. 2008.