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Modeling and Analysis of 11 Level Hybrid H-Bridge Multilevel Inverter with Minimum Number of Switches

A. Ramesh[*], O. Chandra Sekhar[**] and M. Siva Kumar[***]

Abstract: The need for converters of high power and high voltage with quality waveform and better spectrum of harmonics has been increasing rapidly for industrial applications. In this connection, the multilevel inverter came into existence and became popular. Out of various types of multilevel inverters, the cascaded H-Bridge type got its own identity because of its unique features. The voltage stress on the switches and harmonics can also be minimized by increasing the number of levels. But, as the number of levels increases, the number of switches required would also increase, further cost increases. This paper proposed a new topology named as hybrid H-Bridge multilevel inverter. Using this proposed topology, we can decrease the number of switches when compared to cascaded H-Bridge (CHB) for same level of output voltage. In this paper, the modeling and simulation for eleven level multilevel H-bridge inverter is done and the results are displayed and compared.

Keywords: Cascaded H-Bridge, Harmonics, hybrid H-Bridge, and multilevel inverters.

1. INTRODUCTION

The most common problem with *dc* to *ac* conversion is quality in waveform, which includes harmonics. All conventional inverters produce the two level output voltage (square wave) in which more harmonic [1-3] components present. Due to this harmonics, there would be more heat losses and the parasitic torque is developed in case of rotating machines. Therefore, the research has been started to overcome this problem and the multilevel inverter topology is one of the solutions. The multilevel inverter [4-6] has features like, producing the output voltage with lower *dv*/*dt*, less distortion in input current and low switching frequency. And these multilevel inverters are classified as diode clamped, flying capacitor and cascaded H-Bridge type [7-9]. The diode clamped and flying capacitor type multilevel inverters require more number of diodes and capacitors respectively. So, the cascaded H-Bridge type multilevel inverter is the commonly implemented type. Using this topology, we can get nearly sinusoidal waveform by increasing the number of levels in output voltage. As the number of levels is increasing, the number of H-Bridges to be cascaded is also increases. Each H-Bridge consists of four switches, and the generalized formula for number of levels is $2n + 1$. Here n is number of H-Bridges. For example if we need to get seven levels the required number of bridges is 3 and for eleven level 5 bridges required. For eleven level output the rate of change of voltage (*dv*/*dt*) for each level is $V_{dc}/5$. But for more levels the number of switches required is increasing, which causes to increase the cost of inverter.

Therefore, the hybrid H-Bridge type multilevel inverter is proposed to overcome the problem in cascaded-Bridge. In this proposed topology, the same H-Bridge is used and the bidirectional switch along with Diode Bridge is connected at input side. By operating this switch in different combinations with other switches, we can get the eleven level output with less number of switches when compared to cascaded H-Bridge multilevel inverter [10-12]. The design and simulation is done for both cascaded and hybrid

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H-Bridge inverters using Matlab/Simulink software. The FFT analysis is also done for evaluating the total harmonic distortion (THD) for both the topologies. We also compared the topology and switching table for same eleven level output voltage.

2. ELEVEN LELEL CASCADED H-BRIDGE MULTILEVEL INVERTER

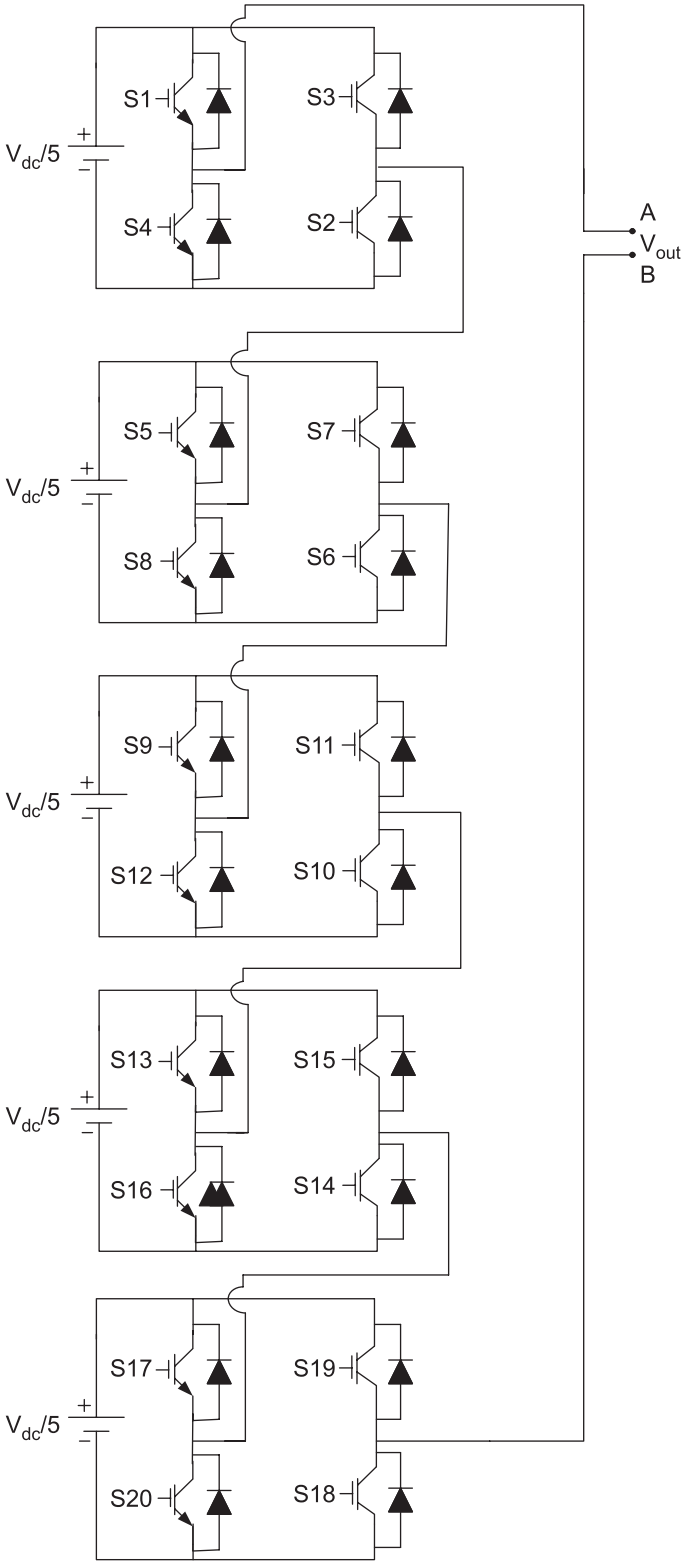


Figure 1: 11 level cascaded H-Bridge multilevel inverter

The Figure 1 represents the 11 Level cascaded H-Bridge multilevel inverter configuration. In this configuration, total five H-Bridges have connected in series to get the output voltage and each bridge consists of four switches. The total number of switches required is 20. The voltage source connected to each bridge is $V_{dc}/5$. The number of gate driver circuits and protection circuits for switches is 20 each. However, the rate of change of voltage (dv/dt) for each level is $V_{dc}/5$. Hence, the stress on switches would decrease.

Table 1 gives the switching sequence for 11 level cascaded H-Bridge multilevel inverter. To get the corresponding level the number of switches to be active is clearly shown in this table. For example, to get zero output voltage the load must be short circuited by all the bottom switches and the path is A-S2-S4-S6-S8-S10-S12-S14-S16-S18-S20-B. To get $2V_{dc}/5$, the switches S5 & S6 should be ON. In this manner by giving the gate pulse to required switches for particular level, we can get 11 level output voltage.

Table 1
Switching Sequence for 11 Level Cascaded H-Bridge

Voltage level	*Switching operation*																			
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{16}	S_{17}	S_{18}	S_{19}	S_{20}
0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
$V_{dc}/5$	1	1	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$2V_{dc}/5$	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$3V_{dc}/5$	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0
$4V_{dc}/5$	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0
V_{dc}	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
$-V_{dc}/5$	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$-2V_{dc}/5$	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
$-3V_{dc}/5$	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0
$-4V_{dc}/5$	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0
$-V_{dc}$	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0	1	1

3. ELEVEN LEVEL HYBRID H-BRIDGE MULTILEVEL INVERTER

Figure 2 represents 11-level hybrid H-Bridge multi level inverter. It could be clearly observed that the number of switches for this configuration is 8 which are 60% less than the switches required as in case of cascaded H-Bridge multilevel inverter. And the diode bridge circuits are connected to the source side switches in order to have bidirectional operation of switches. Using this bidirectional switches we could get number of levels by Operating only two switches for each level. The output is connected between terminals A and B. However, in this topology also we have used five voltage sources of $V_{dc}/5$ each. The foremost advantage of this topology is, it requires less number of switches for the same voltage levels when compared to cascaded H-Bridge type. Therefore, the cost decreases, the number of gate driver circuits would be less and the required protection circuits for switches also be minimized. Here the rate of change of voltage is $V_{dc}/5$ and the stress on the switches is low. Moreover, the size of the inverter is also reduced.

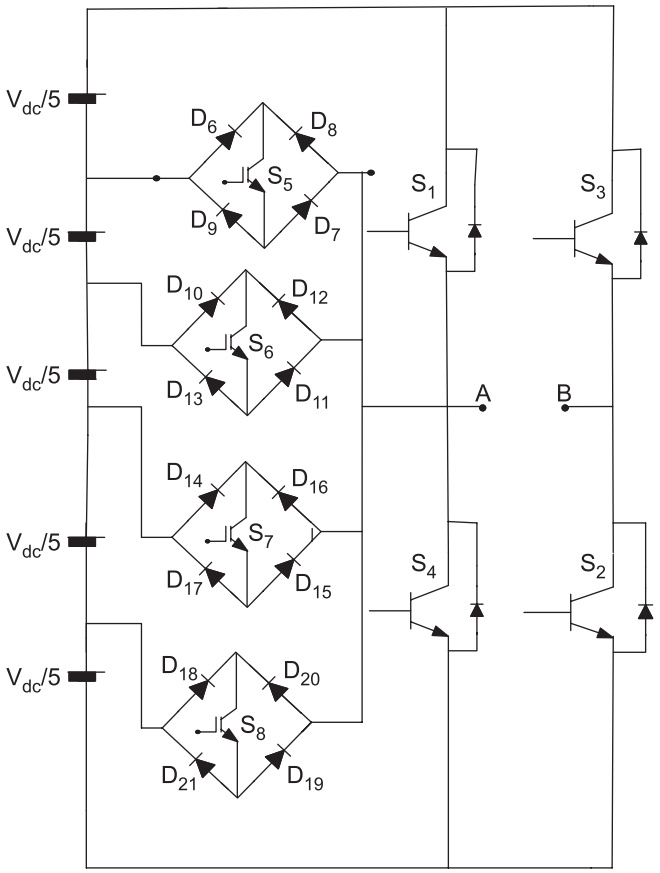


Figure 2: 11 level hybrid H-Bridge multilevel inverter

Table 2
Switching Sequence for 11 Level Hybrid H-Bridge

Voltage level	*Switching operation*							
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
0	0	1	0	1	0	0	0	0
$V_{dc}/5$	0	1	0	0	0	0	0	1
$2V_{dc}/5$	0	1	0	0	0	0	1	0
$3V_{dc}/5$	0	1	0	0	0	1	0	0
$4V_{dc}/5$	0	1	0	0	1	0	0	0
V_{dc}	1	1	0	0	0	0	0	0
$-V_{dc}/5$	0	0	1	0	1	0	0	0
$-2V_{dc}/5$	0	0	1	0	0	1	0	0
$-3V_{dc}/5$	0	0	1	0	0	0	1	0
$-4V_{dc}/5$	0	0	1	0	0	0	0	1
$-V_{dc}$	0	0	1	1	0	0	0	0

The above table shows the switching sequence for 11 level hybrid H-Bridge. As the number of switches are less, the switching operation is simple and we can observe that at any time only two switches will be in active mode. For instance, if we consider $3V_{dc}/5$ level, the switches S_2 and S_6 are in active mode (ON) and for $V_{dc}/5$ level switches S_3 and S_5 are in active mode.

4. MODES OF OPERATION FOR 11 LEVEL HYBRID H-BRIDGE

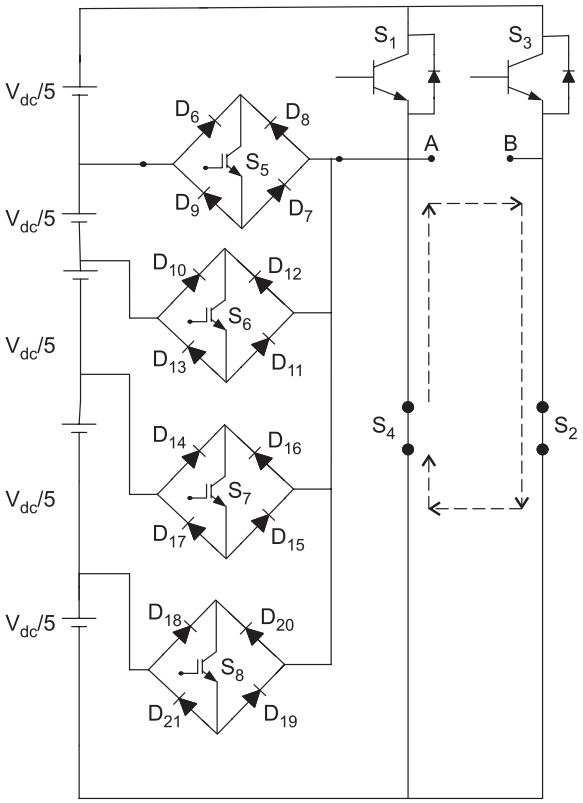


Figure 3: (a) Circuit for zero voltage level

The current path for zero voltage level is shown above and the path is $S_4 - A - B - S_2 - S_4$.

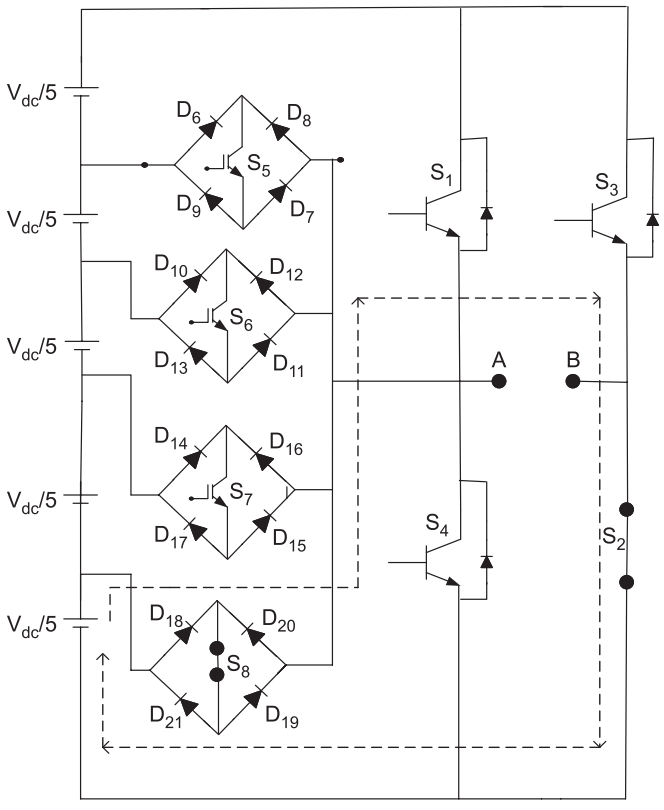


Figure 3: (b) Circuit for voltage level of $V_{dc}/5$

The current path for voltage level of $V_{dc}/5$ is shown above and the path is through S_2 and S_8.

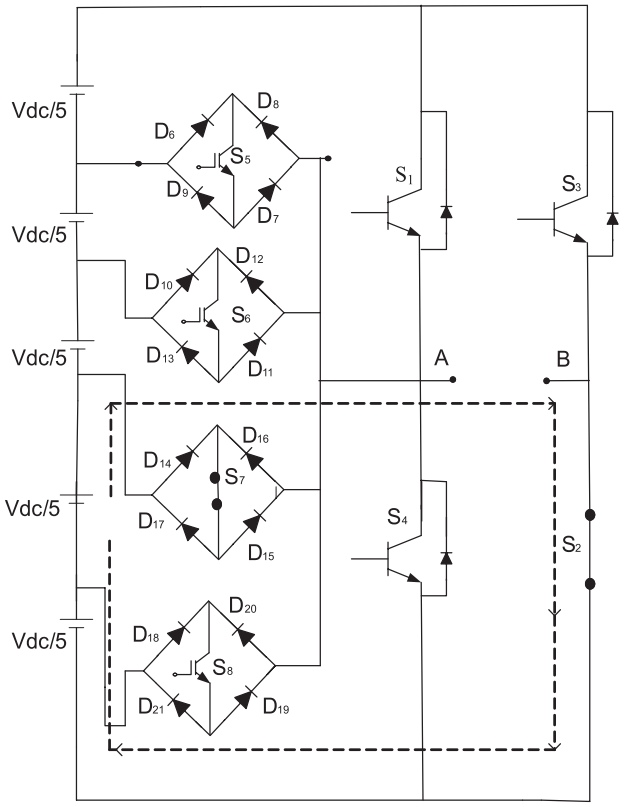


Figure 3: (c) Circuit for voltage level of $2V_{dc}/5$

The current path for voltage level of $2V_{dc}/5$ is shown above and the path is through S_2 and S_7.

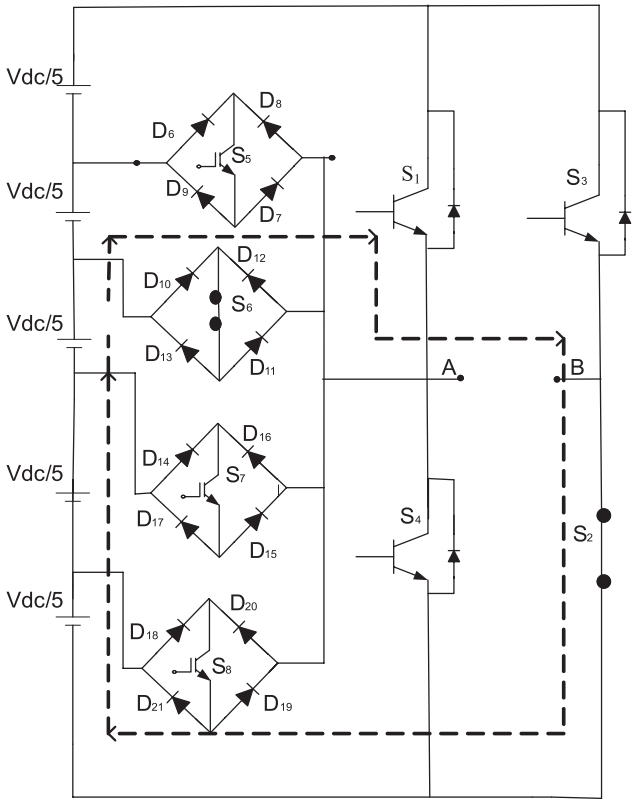


Figure 3: (d) Circuit for voltage level of $3V_{dc}/5$

The current path for voltage level of $3V_{dc}/5$ is shown above and the path is through S_2 and S_6.

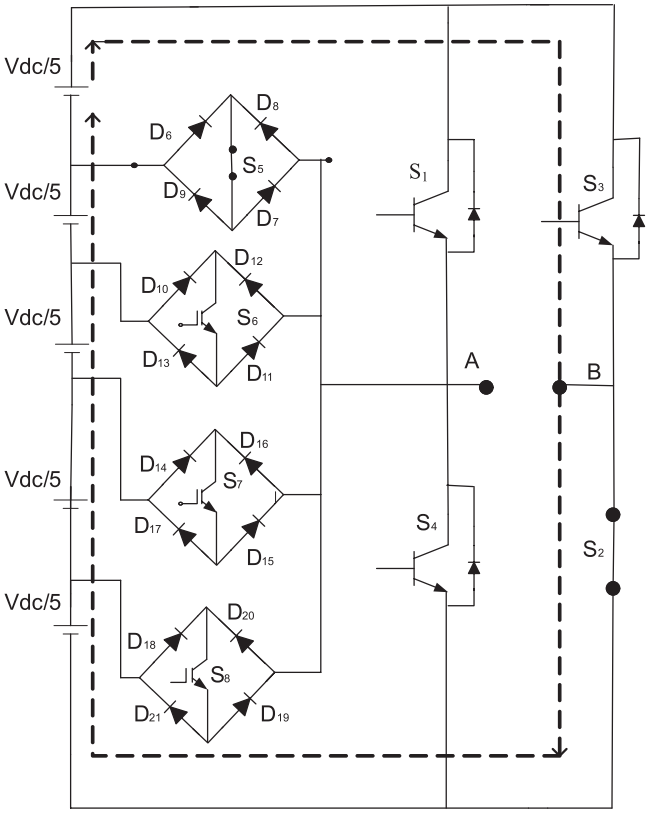


Figure 3: (e) Circuit for voltage level of $4V_{dc}/5$

The current path for voltage level of $4V_{dc}/5$ is shown above and the path is through S_2 and S_5.

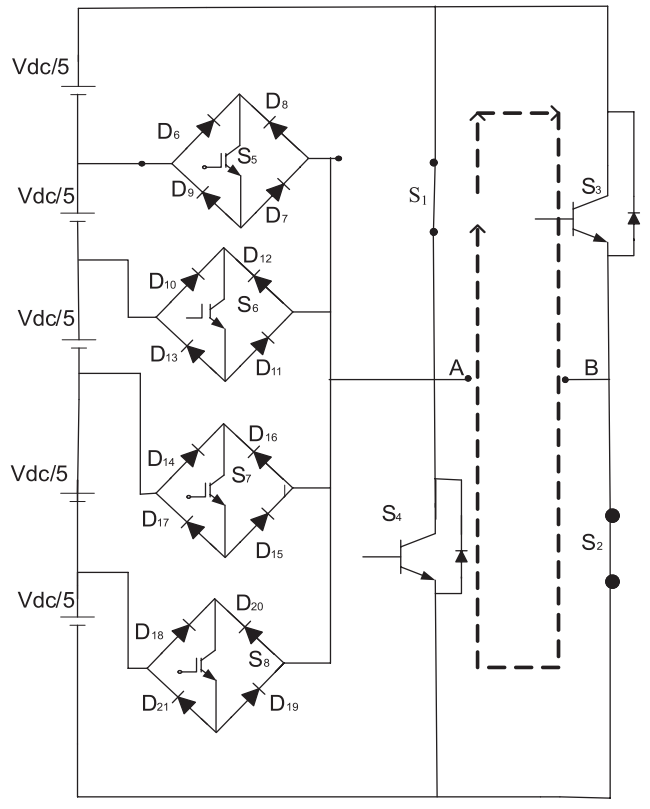


Figure 3: (f) Circuit for voltage level of V_{dc}

The current path for voltage level of V_{dc} is shown above and the path is through S_1 and S_2.

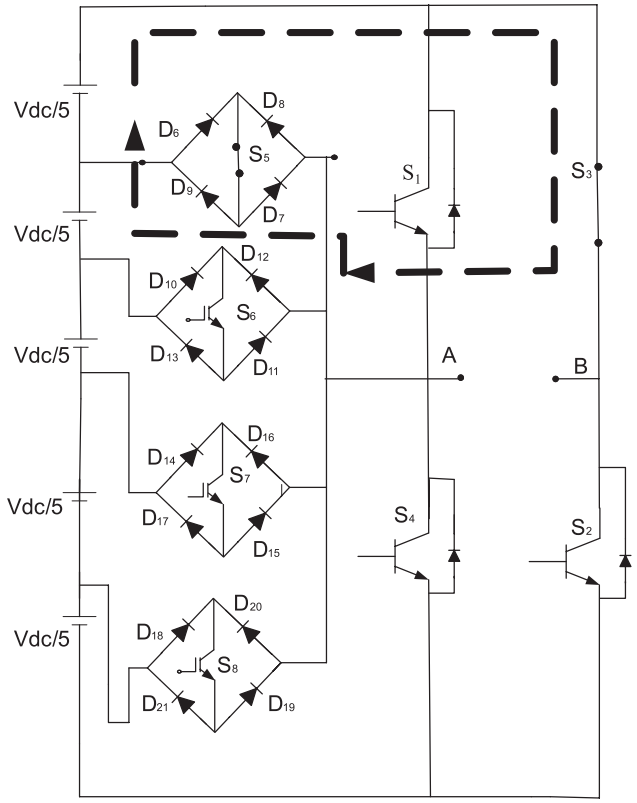


Figure 3: (g) Circuit for voltage level of $-V_{dc}/5$

The current path for voltage level of $-V_{dc}/5$ is shown above and the path is through S_3 and S_5.

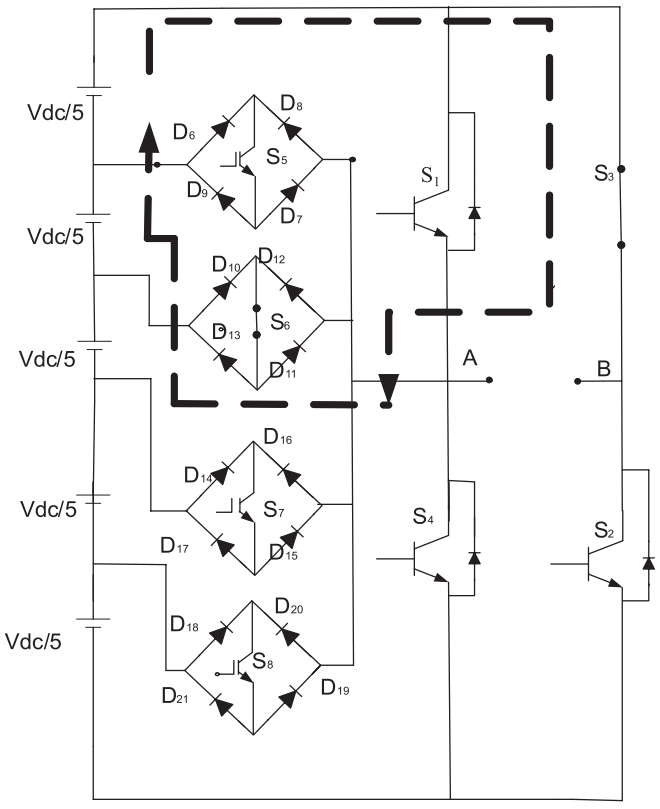


Figure 3: (h) Circuit for voltage level of $-2V_{dc}/5$

The current path for voltage level of $-2V_{dc}/5$ is shown above and the path is through S_3 and S_6.

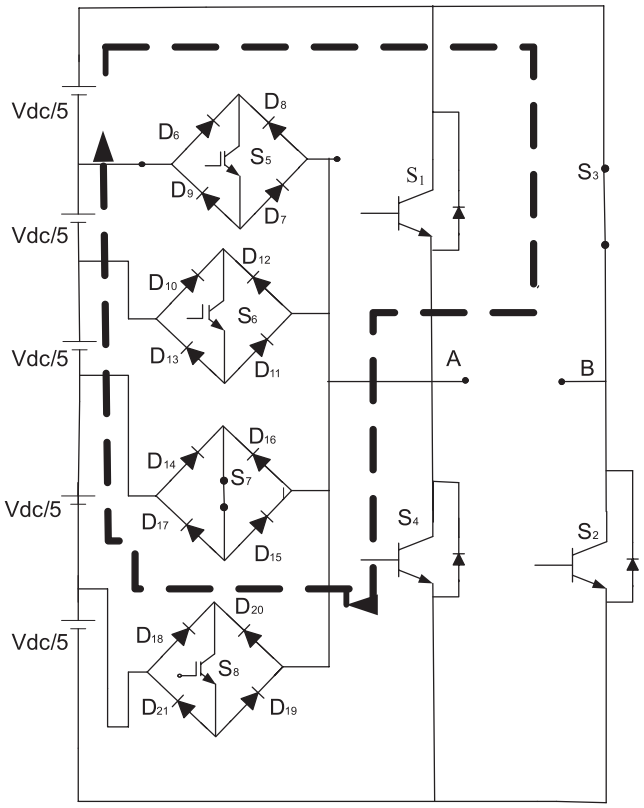


Figure 3: (i) Circuit for voltage level of $-3V_{dc}/5$

The current path for voltage level of $-3V_{dc}/5$ is shown above and the path is through S_3 and S_7.

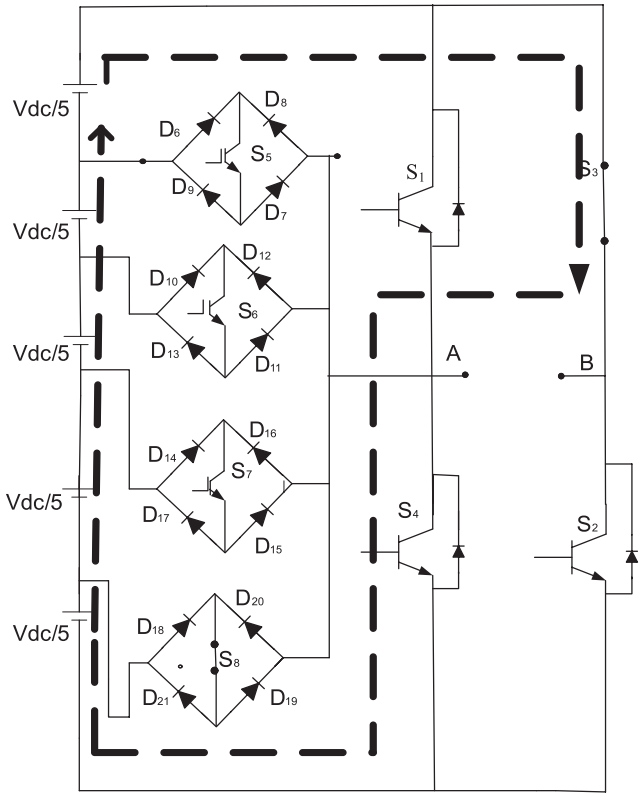


Figure 3: (j) Circuit for voltage level of $-4V_{dc}/5$

The current path for voltage level of $-4V_{dc}/5$ is shown above and the path is through S_3 and S_8.

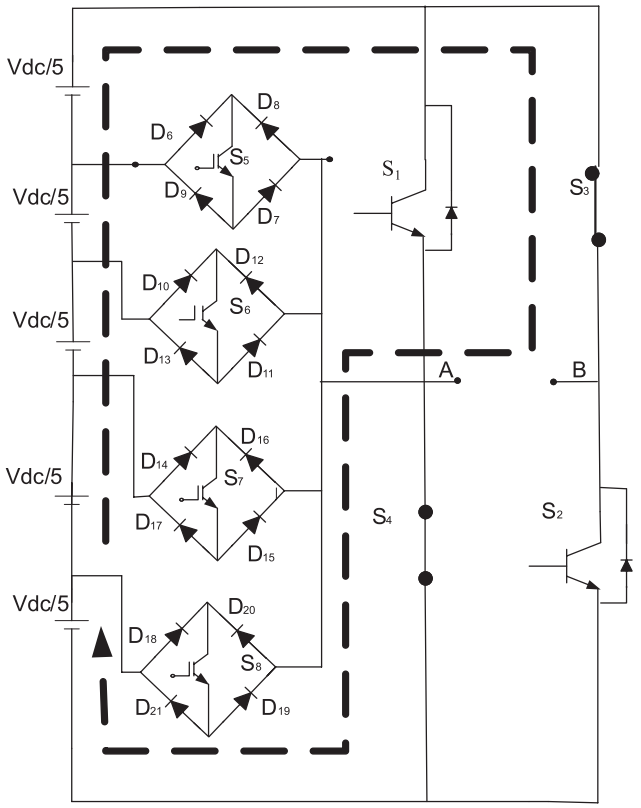


Figure 3: (k) Circuit for voltage level of $-V_{dc}$

The current path for voltage level of $-V_{dc}$ is shown above and the path is through S_3 and S_4.

5. MATLAB MODELING AND SIMULATION RESULTS

In the above figure it is shown that the simulink model of 11 level cascaded H-Bridge multilevel inverter with a resistive load. Here the load is taken as 10 kW and all the required parameters are considered. The repeating sequence block is used to give timing sequence for switches and the same is applied for bottom switches with a NOT operation.

The above figure shows the output voltage and current waveforms for cascaded H-bridge multilevel inverter with resistive load of 10 kW. The current waveform follows the voltage because of resistive load, but the magnitude is different.

Figure 6 gives the FFT analysis of voltage for cascaded H-Bridge inverter. From the FFT analysis of voltage it is seen that the total harmonic distortion (THD) = 14.29%.

The above figure shows the output voltage and current waveforms for cascaded H-bridge multilevel inverter for RL load of 10 kW. Here we can observe the variation in current waveform because of the presence of the inductor in the load.

The simulation for 11 level hybrid H-Bridge is shown above and the difference between cascaded and hybrid H-Bridge is the number of switches which can easily be observed. Here also the same load is connected. In addition we have connected diode bridge circuits at input side switches.

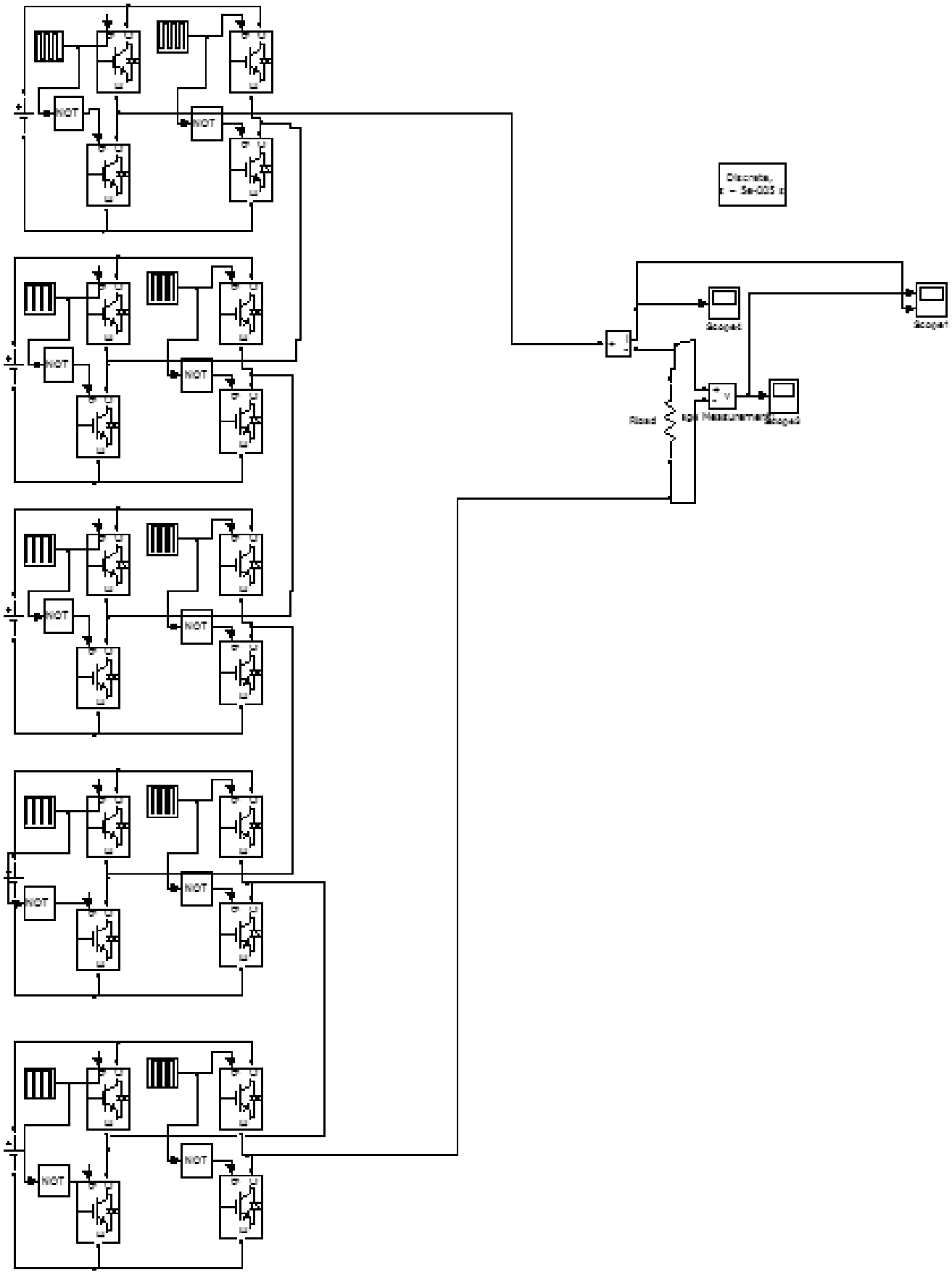


Figure 4: Matlab/simulink model of 11 level cascaded H-Bridge Multilevel inverter

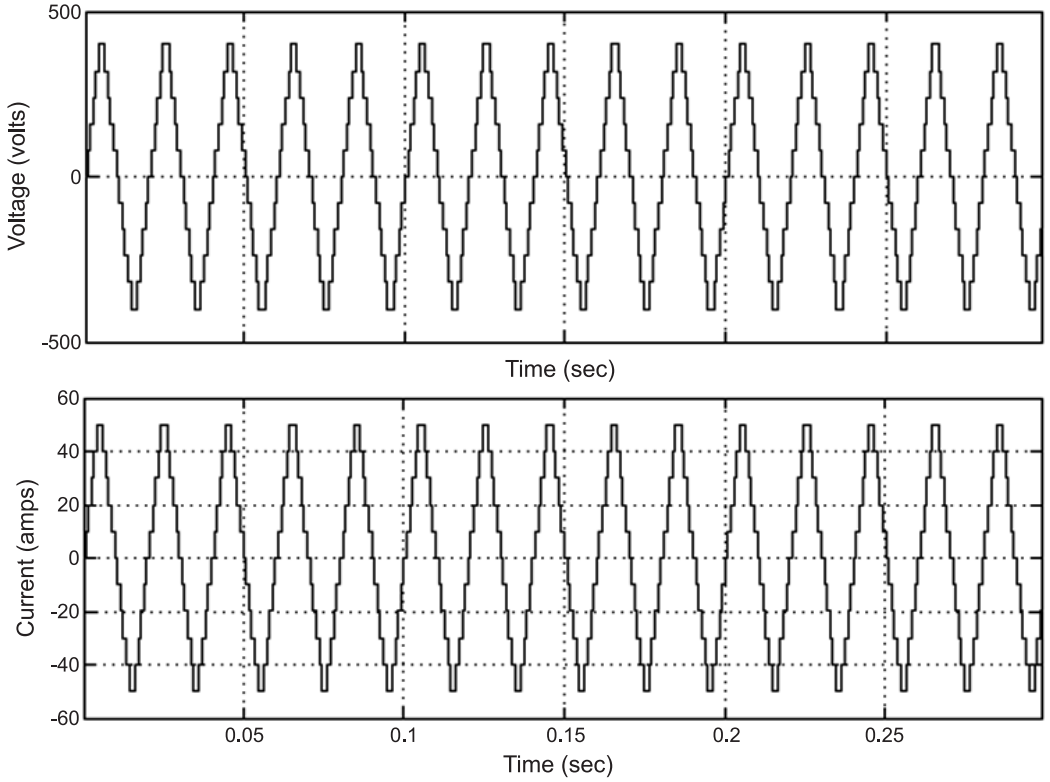


Figure 5: Output wave forms of 11 level cascaded H-Bridge multilevel inverter for R load

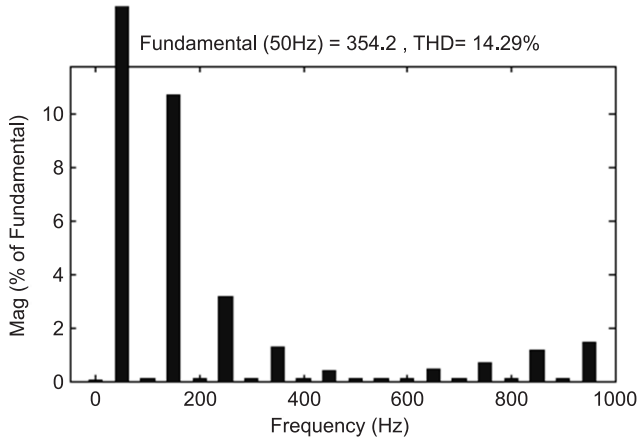
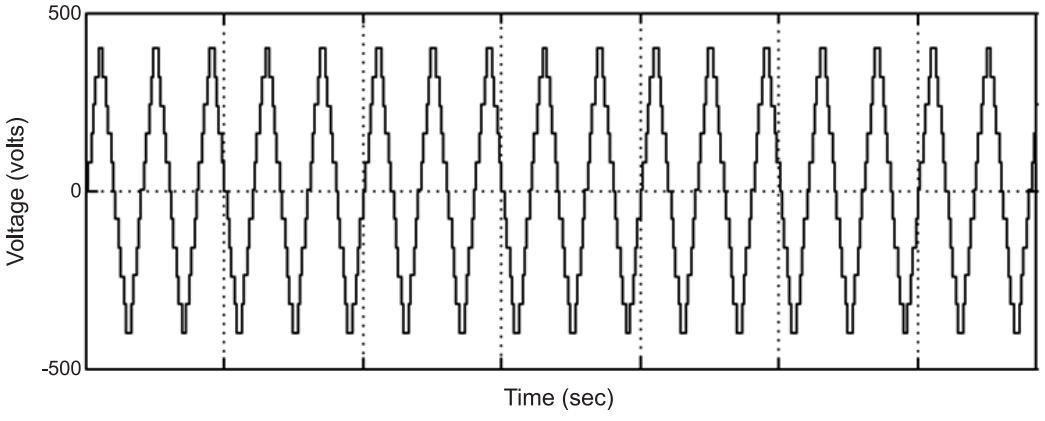


Figure 6: FFT analysis of voltage for eleven level cascaded H-Bridge



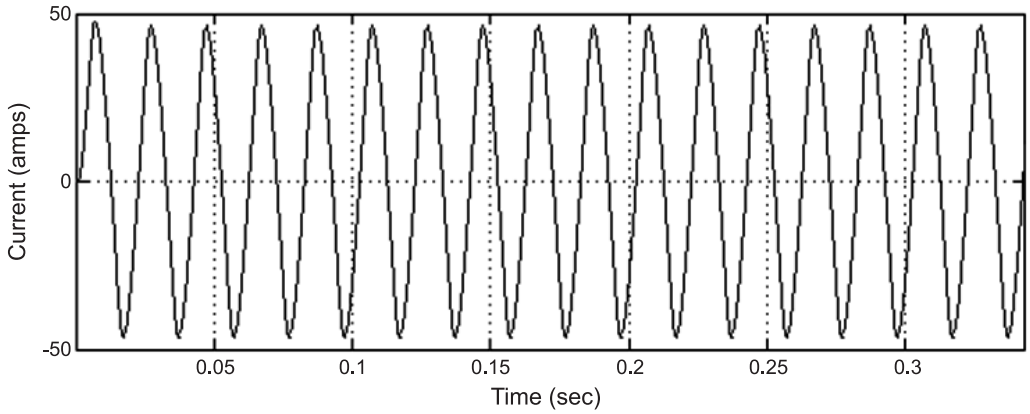


Figure 7: Output wave forms of 11 level cascaded H-Bridge multilevel inverter for RL load

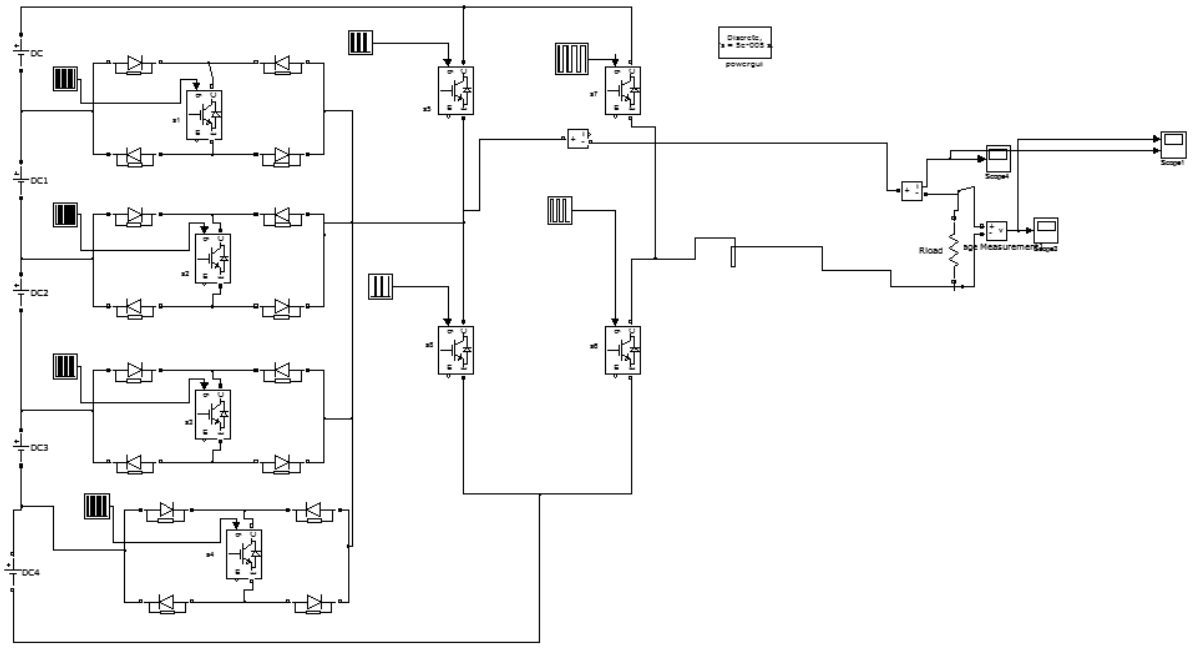
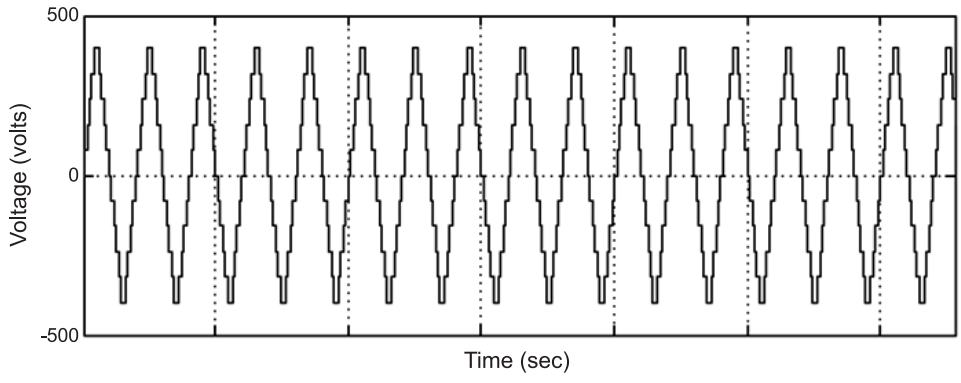


Figure 8: Matlab/Simulink model of 11 level hybrid H-Bridge

The above figure shows the output voltage and current waveforms for hybrid H-bridge multilevel inverter for resistive load of 10 KW. Here also the *dv*/*dt* is same for same load.

Figure 10 shows the FFT analysis of voltage for cascaded H-Bridge inverter. From the FFT analysis of voltage it is seen that the total harmonic distortion (THD) = 14.62%.

Figure 11 depicts the voltage and current waveforms for 11 level hybrid H-Bridge for RL load.



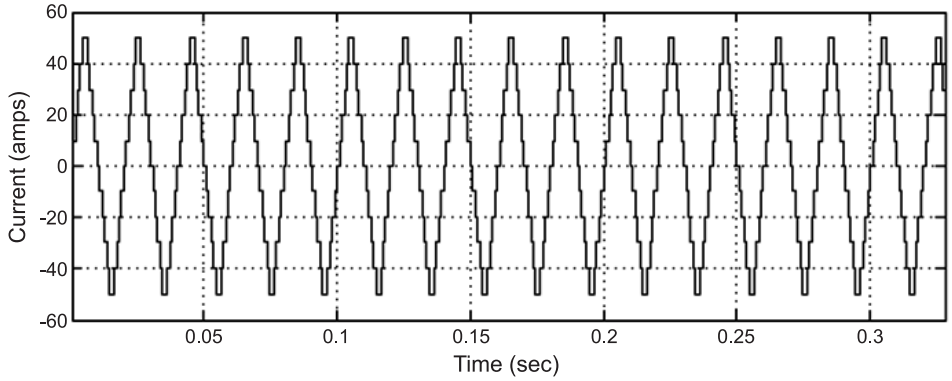


Figure 9: Output wave forms of 11 level hybrid H-Bridge multilevel inverter for R load

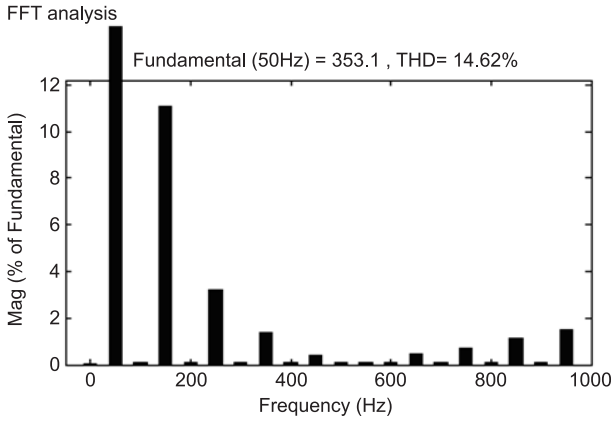


Figure 10: FFT analysis of voltage for eleven level hybrid H-Bridge

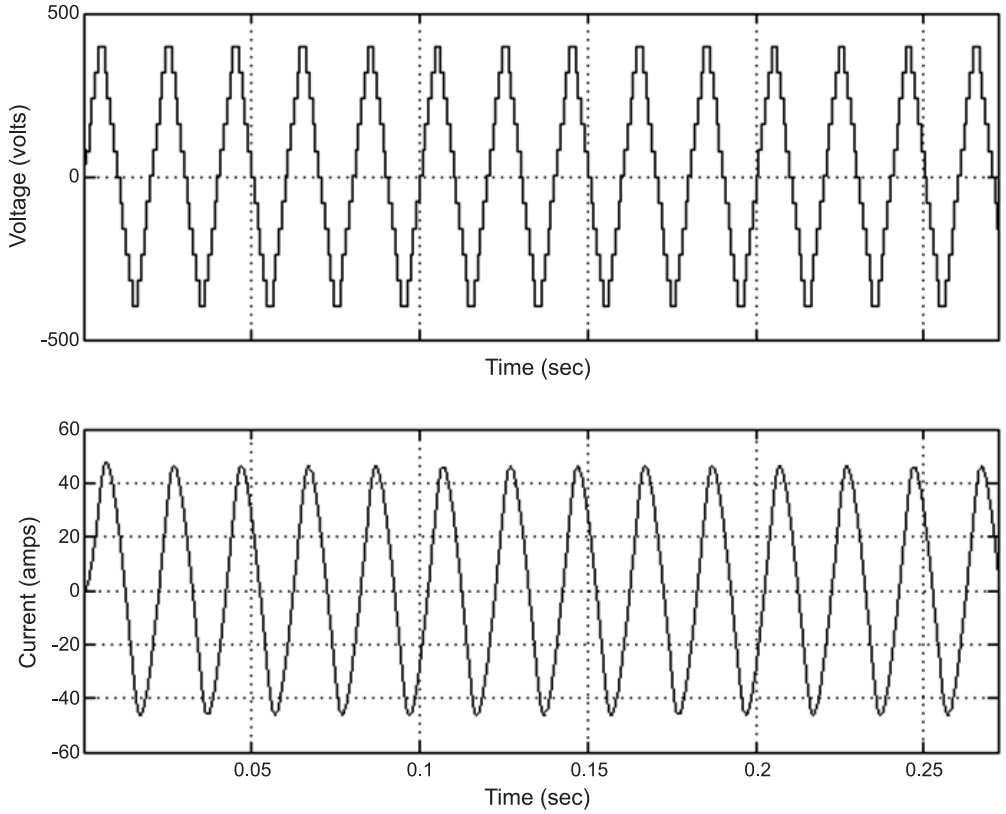


Figure 11: Output wave forms of 11 level hybrid H-Bridge multi level inverter for RL load

6. COMPARISION TABLE

Parameter	*Cascaded H-Bridge*	*Hybrid H-Bridge*
dv/*dt*	$V_{dc}/5$	$V_{dc}/5$
No. of switches	20	8
No. of gate drivers	20	8
No. of protection circuits	20	8
Foot print	More	Less

7. CONCLUSION

After implementing both the topologies, it is strongly confirmed that for the same level of output voltage the cascaded H-Bridge required 20 number of switches and the hybrid H-Bridge required only 8 number of switches. The count in switches has been decreased which decreases the cost. And the number of gate driver circuits required is 8 and the protection circuits required is also minimized to 8. But, in the case of cascaded H-Bridge type the count is only 20. Even though, the rate of change of voltage (*dv*/*dt*), the number of levels in output voltage, and the total harmonic distortion (THD) are same for both topologies, it is firmly recommended the hybrid H-Bridge type because of constraints like cost, size and circuit complexity.

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