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ANALYSIS AND COMPARISON OF VARIOUS PERFORMANCE PARAMETERS AND SHORT CHANNEL EFFECTS OF N CHANNEL AND P CHANNEL DUAL GATE JUNCTIONLESS TRANSISTORS AT DIFFERENT TECHNOLOGY NODES

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Abstract: The junctionless technology being an encouraging technology for designing the devices with lesser flaws, various parameters involved in N-type and P-type dual gate junctionless transistor at different technology nodes 10nm, 20nm, 30nm and 40nm have been compared. Dual gate junctionless transistor has better control on the carriers. In this research paper simulations on TCAD have shown the variation of performance parameters like Subthreshold slope, Drain induced barrier lowering, threshold voltage, on current, off current and On/Off current ratio of both the devices. These junctionless devices operate at opposite work function than conventional one. The main advantage of such devices is easier and lesser fabrication steps.

Key Words: Work function, short channel effects, Junctionless transistor (JLT), P-channel dual gate junctionless transistor (PDGJLT), N-channel dual gate junctionless transistor (NDGJLT).

1. INTRODUCTION

According to international technology roadmap for semiconductors (ITRS), a large trend of swift scaling of the devices is taking place [1]. Transistor acts as a switch and plays a decisive role in various circuits. There is a need of proper control of current to drive any VLSI circuit and also a limit has to be set for current to flow. However, unfortunately we have seen a major drawback in inversion mode MOSFET undergoing scaling. In today's scenario of technology we are working with nanoscale devices, as devices are undergoing a retrenchment more and more entanglements are observed in fabrication field of scaled devices [3]. Also the working of such scaled devices has become more dubious due to presence of short channel effects. Short channel effects occur when devices are retrenched and hence channel becomes short [1], [2], [3]. Inversion mode MOSFET comprises of source and drain junction. During retrenchment the distance between source and drain is reduced and hence short channel effects starts demeaning the performance of the devices [4]. Channel starts losing its control on the carriers and hence dual gate MOS, Gate all around devices

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have been introduced. During retrenchment of the devices the process of aligning the deep-shallow source and drain junctions are becoming very hard. So an advanced research has found a magnificent technology in which there is no need to form any source and drain junctions called junctionless transistor technology (JLT) [3], [4].

This has become a favorable type of transistor which is capable of condensing different trouble and is present in inversion mode MOSFET during scaling. This type of device has a steady doping all the way from source to channel to drain. There is a zero concentration gradient in the entire device. N-type junctionless transistor (NJLT) and P-type junctionless transistor (PJLT) are devices with n channel/n-type substrate and p channel/p-type substrate respectively. The operation of such device depends highly on work function of gate material. Work function of such devices is very significant to Off and On the device. JLT devices follow a conduction in the entire device called bulk conduction [5], [7], [8], [9]. In this article we have demonstrated P channel and N channel dual gate Junctionless transistor at various technology nodes. Various specifications are considered while simulating the structures in TCAD simulator [13].

2 DEVICE STRUCTURE

The P-type DGJLT and N-type DGJLT are drawn using technology computer aided design software (TCAD) [13].

2.1 P-Type and N-type Dual gate junctionless transistor

The material distribution in P-type dual gate junctionless transistor consists of acceptor type doping and p-type substrate. The work function of junctionless transistor is taken opposite to conventional type MOSFET. The substrate and channel is same for such junctionless devices.

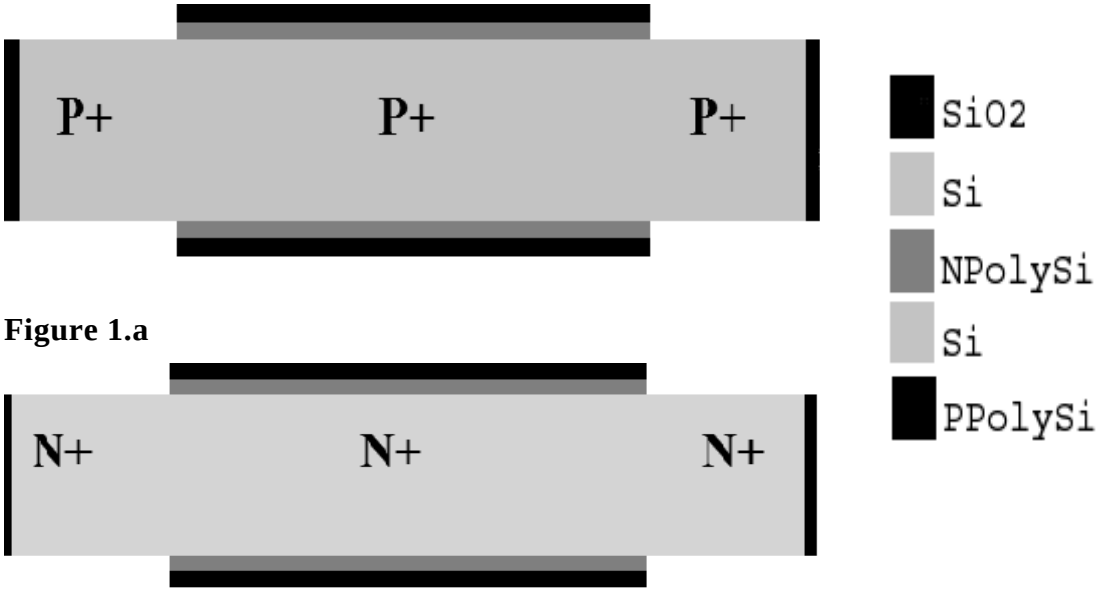

Figure 1.a

Figure 1.b

Figure 1. Material Distribution of N and P channel Double Gate Junctionless transistor.

The design has zero acceptor and donor type concentration gradient. The value of doping is taken as 1.5e+19cm^{-3}. The high doping of such devices is due to reason that there is only single doping which is responsible for current to flow in the device and channel formed is in the bulk. Fig. 1.a and Fig. 1.b shows the material distribution of p-type and n-type dual gate junctionless

transistor respectively. The N-type DGJLT has both n channel and n substrate. The structures shown in Fig. 1 are drawn at different technology nodes 10nm, 20nm, 30nm and 40nm and all parameters are evaluated for each channel length. Values used in entire simulation are given in Table 1.

Table 1
Values used in drawing and simulating the junctionless structures [6][13].

S.No	*Parameter Name*	*Notation*	*P-DGJLT*	*N-DGJLT*
1	Doping	N_d, N_a	1.5e+19cm-3	1.5e+19cm-3
2	Work function	Φ	4.1eV	5.3eV
3	Oxide thickness	t_{ox}	1nm	1nm
4	Channel length	L	10, 20, 30, 40nm	10, 20, 30, 40nm

The simulated structures of N and P channel double gate junctionless transistor at channel length 20nm are drawn using VisualTCAD are shown in Figure 2.a and 2.b respectively.

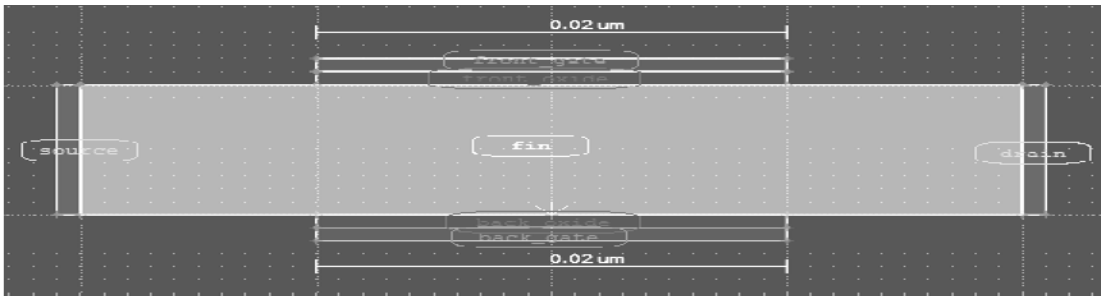

Figure 2.a

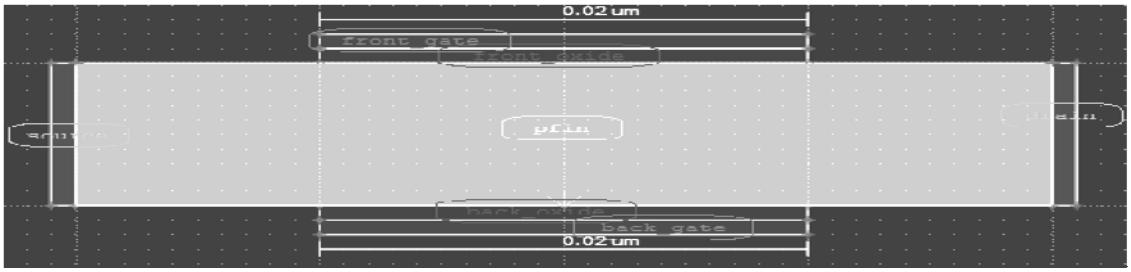

Figure 2. b

Figure 2. Simulated structures of N channel and P channel dual gate junctionless transistor at channel length 20nm is shown in Figure 2.a and Figure 2.b respectively.

The entire simulations of these structures are performed using different work functions and other parametric values. The simulations performed at various channel lengths also include Lombardi as mobility model, basic drift-diffusion equations for calculating the results. Impact ionization effect is not taken in entire simulation for both the structures as due to this effect carrier density increases and as a result current increases rapidly and creates an impact on the results.

3. RESULTS AND DISCUSSION

The performance parameters and short channel effects such as Subthreshold slope (SS), Drain induced barrier lowering (DIBL), Threshold voltage (V_{th}), On current, Off current and On/Off

current ratio have been calculated and compared for both P-type and N-type dual gate JLT at various technology nodes.

3.1 Subthreshold slope (SS) and Drain Induced Barrier Lowering (DIBL)

Subthreshold slope is defined as slope of subthreshold region. This region represents the (on to off) or (off to on) switching of the transistor. DIBL is a short channel effect which refers to the reduction in threshold voltage at higher voltages. Figure 2.a and Figure 2.b depicts the variation of subthreshold slope and DIBL at different channel lengths for both P and N-type dual gate junctionless transistor. P-type and N-type structure follows the same fashion of decreasing SS and DIBL with channel length. The reason for decrease in SS is due to decrease in drain current with channel length. For N-type SS at 10nm is 100.0 mV/decade and at 40nm is 62.50 mV/decade where for P-type at 10nm is 112.3 mV/decade and at 40nm is 86.9 mV/decade. The lesser value of SS expose that switching will happen faster. The different values of SS and DIBL for both P and N–type transistors are due to the nature and property of carriers. DIBL is calculated at V_{ds}=50mV and at 1V. DIBL is found to have a larger values at L=10nm for both type of DGJLT. The probable reason for decrease in DIBL is lesser off current with increase in length of the channel [8], [10], [11], [12].

3.2 Threshold Voltage (V_{th}), ON current (I_{on}), OFF current (I_{off}) and I_{on}/ I_{off} current ratio

Threshold voltage is a gate voltage which acts as a benchmark for the conduction in the device. Threshold voltage for N and P-type DGJLT is positive and negative respectively due to the nature of carriers involved. Threshold voltage for both junctionless P-type DGMOS and N-type DGMOS increases with the increase in channel length. Threshold voltage is calculated by keeping drain voltage at 50mV for JLT-DGNMOS and at -50mV for JLT- DGPMOS. If the gate voltage is below the threshold voltage, the transistor is turned off and ideally there is no current from the drain to the source of the transistor. In fact, there is a current even for gate biases below the threshold (leakage) current, although it is small and varies exponentially with gate bias. Figure 2.c illustrates the variation of threshold voltage for both types of transistors [12].

On current is the drain current which drives the circuit and OFF current degrades the performance of the device [11], [12]. OFF current keeps the device ON even if switch is off. Figure 2.d and Figure 2.e depicts the ON current and OFF current for both P-type and N-type DGJLT at various technology nodes respectively. Due to this current, large power dissipiation takes place as there will always be a current flowing in the device [1], [5], [12]. Therefore power consumption increases. ON current and OFF current for both P-type and N-type DGJLT is observed to be decreasing with the increase in channel length. The reason for decrease in ON current is the inverse dependence of channel length and current [3] and for decrease in OFF current is the increase in area from 10nm to 40nm. The difference between the ON current and OFF current in both the devices is the negative value of current in P-type which represents the direction of the flow of holes. The values of ON current of N-DGJLT at 10nm is 1.29e-05A, at 20nm is 9.06e-06A, at 30nm it is 7.02e-06A and at 40nm it is 5.78e-06A. Similarly OFF current also decreases, at 10nm it is 9.25e-09A, at 20nm is 2.52e-12A, at 30nm is 1.15e-13A and at 40nm it is 5.78e-14A. ON current needs to be higher and off current has to be lesser for an efficient working of the device. ON/OFF current ratio is also shown for both P and N-type DGJLT in Figure 2.f.

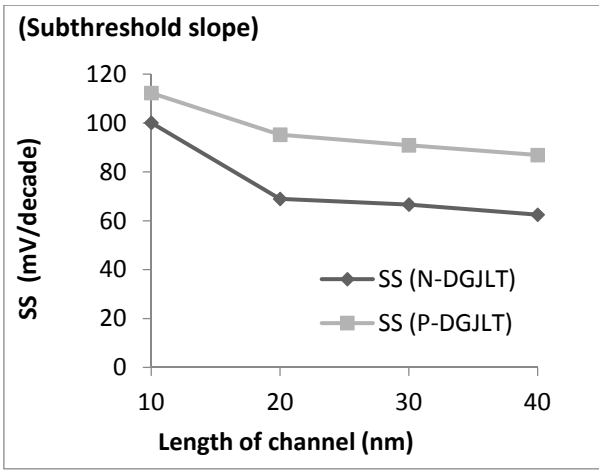

Figure 2.a

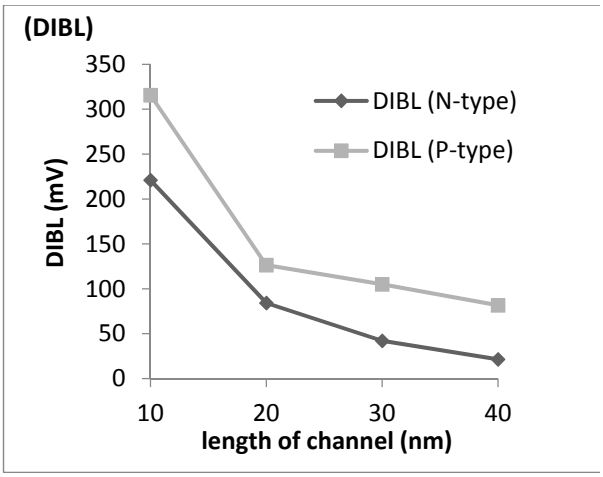

Figure 2.b

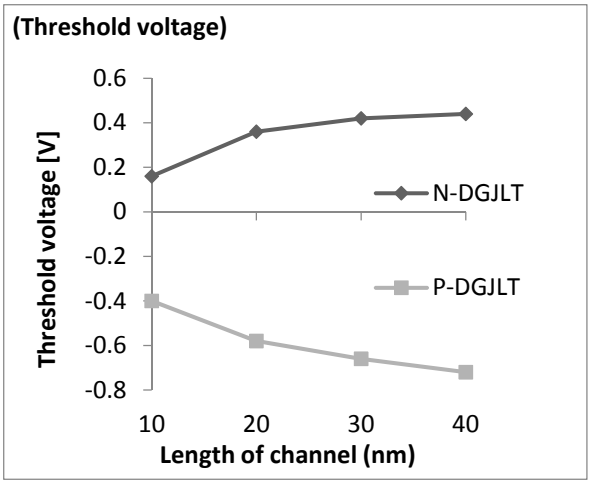

Figure 2.c

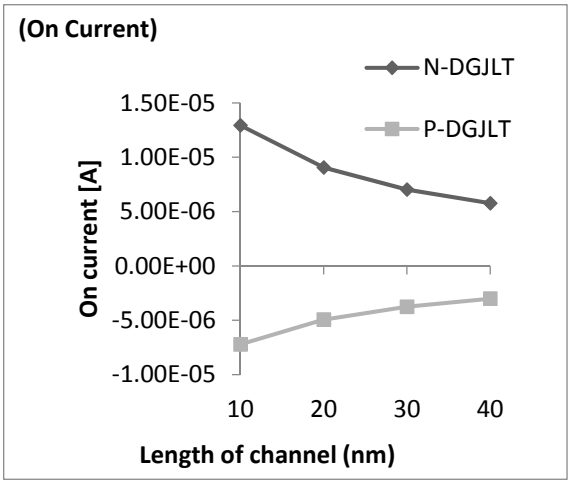

Figure 2.d

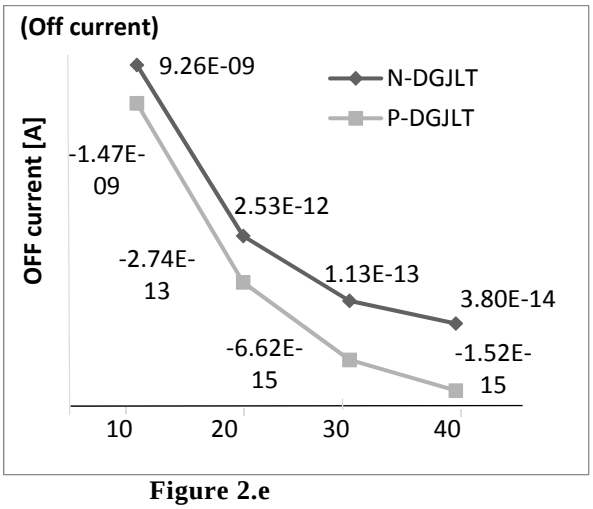

Figure 2.e

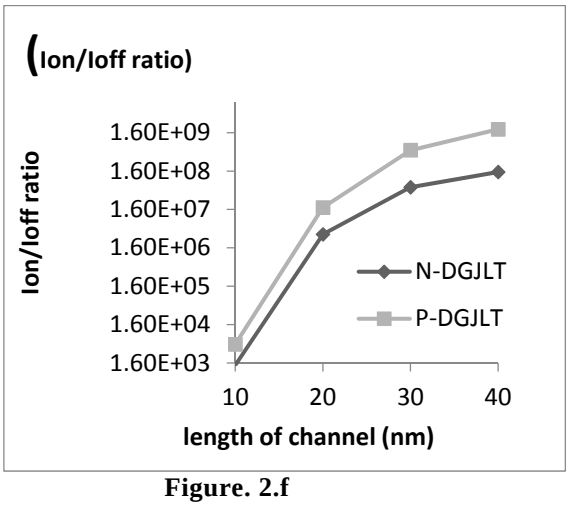

Figure. 2.f

Figure 2.a-f. Showing various short channel effects and performance parameters of P-DGJLT at work function 4.1eV and N-DGJLT at work function 5.3eV. All results are obtained at V_{ds}= 50mV for N-type and V_{ds} = -50mV for P-type.

In this article, we have discussed about the short channel effects and various parameters which enhance or degrade the performance of DGJLT's. All such parameters are compared at different technology nodes. P and N type channel DGJLT's almost follows the same fashion in all parameters varying along the length of the channel. However the difference occurs in applying the voltages and mobilities of both the devices. As mobility of electrons is higher than holes, N-DGJLT is preferred over P-DGJLT. DIBL and SS are found to be higher for P-DGJLT than N-DGJLT. The probable reason is the nature and direction of carriers flowing in P-type than N-type. The value of current in P- DGJLT is found to be negative which represents the direction of the current in the device. The physics of both the devices is same however due to flowing nature of holes and electrons we can observe the effect in various parameters varying along length of the channel. The devices with this technology are getting its pace due to ease of construction at smaller scales.

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